The conducted immunity of SPI EEPROM memories

Mohamed Amellal, Mohamed Ramdani, Richard Perdriau, Mathieu Médina, M'Hamed Drissi, Ali Ahaitouf

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Mohamed AMELLAL
Mohamed RAMDANI
Richard PERDRIAU
ESEO-EMC, ESEO Angers
10, Bd Jeanneteau
49107 Angers- France
www.eseo-emc.fr
Email: mohamed.amellal@eseo.fr
mohamed.ramdani@eseo.fr
richard.perdriau@eseo.fr

Mathieu MEDINA
SERMA TECHNOLOGIES
30, avenue Gustave Eiffel
33608 Pessac- France
Email: m.medina@serma.com

Mhamed DRISSI
National Institute
of Applied Sciences of Rennes
20, Avenue des Buttes de Cosmes
35708 Rennes- France
Email: mhamed.drissi@insa-rennes.fr

Ali AHAITOUF
Faculty of Sciences and Technology of Fez
DGE, FSTF, B.P. 2202 Fez- Morocco
Email: ali_ahitouf@yahoo.fr

***Abstract*—This paper focus on the conducted immunity measurement of non-volatile memories up to 1 GHz. A specific measurement flow is introduced, which makes possible to compare the EMC performances in different test cases. Trough measurements and simulation, this study gives a real view on the immunity difference of this integrated circuits (IC).**

I. Introduction

Currently, the memory market reaches almost half of the production of integrated circuits. This evolution is mainly due to the improvement of the manufacturing and the design process of memories. Therefore, the significant growth experienced by industrial applications requiring permanent storage of information, helped to focus on the study and improvement of the performance of non-volatile memories. Based on the fact that electromagnetic disturbances can trigger modifications in memory zones, the impact on systems incorporating these circuits can be enough to make them unusable.

In addition, modern ICs suffer from high susceptibility to radio frequency interference up to 5 GHz [1] [2]. Consequently, the study of the conducted susceptibility of various memories is becoming compulsory as far as each supplier has its own technologies. Many efforts have been done in the development of tools, methodology [3] [4] [5] and models [6] for the prediction of parasitic emission of ICs. However susceptibility modeling has not followed the same evolution and few dedicated simulation methodologies or models [7] have been proposed yet, particularly for memories. This paper describes measurement technique based on direct power injection (DPI) test [8] specially dedicated to Serial Peripheral Interface (SPI) memories, which proposes three different test modes and set a digital immunity criterion. The main objective of this study is to compare the conducted immunity of two SPI EEPROM memories.

The paper is organized as follows. Sect. II describes the structure and validity conditions of the test. Then, Sect. III provides the obtained results and discuses the validation of this technique and also a simulation model is presented and explained, before giving some statement about new perspectives.

II. Structure and test set-up of the SPI memories

A. Description of the tested memories

The choice of tested memories was based on the principle of obsolescence, in other words, the selected memories size may be different, with different technologies and produced by different manufactures, however, they must share three characteristics :

- SPI communication interface.
- SOIC8 package.
- 3.3Vpower supply voltage.

Based on these parameters, and in order to assess the impact of manufacturing and design process, we chose to conduct our study on two memories whose characteristics are presented in Table I.

TABLE I
Characteristics of used memories

Characteristics	**AT25512**	**25LC512**
Manufacturer	ATMEL	MICROCHIP
Technology	EEPROM	EEPROM
Memory size	512 Kbits	512 Kbits
Max Frequency	20 MHz	20 MHz
Endurance in Erase/write cycle	1 Million	1 Million

B. Test set-up for SPI memories

The suggested test is dedicated to the prediction of the immunity behavior for continuous wave (CW) disturbances, in the 1MHz–1GHz frequency range, and up to 30 dBm incident power in the DPI test.
As shown in the Figure 1, the measurement system consists of two different board:

- **Test PCB**: it is a generic SOIC DPI measurement board [9]. Thanks to it, both S-parameter and DPI measurements can be performed on the same PCB.

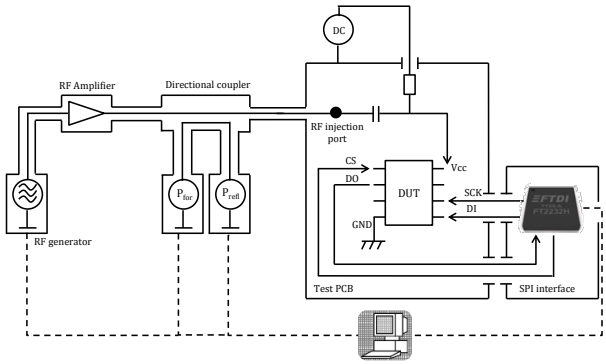


Fig. 1. General diagram of DPI measurement system for SPI memories

- **SPI interface**:This board is specifically developed for the study of SPI memories with a module *FTDI2232H* that plays the role of the SPI communication interface. In fact, this component will allow the implementation of our susceptibility criteria for the different test mode.

It should be noted that in addition to being mounted on two separate boards, the FTDI module and the DUT have also two different power supplies. The purpose of this is to reduce as much as possible coupling of RF aggression to the SPI power supply board and, consequently,the disturbance of the FTDI module.

C. Definition of an immunity criterion

The definition of immunity criteria for integrated circuits is still a prominent issue, due to the very wide range of IC functionalities. For memories, the accuracy of its returned data is the essential information, therefore our criterion is based on this assertion. The circuit is considered perturbed if:

- **Criterion 1**: The value of the status register has changed after the RF perturbation.
- **Criterion 2**: The percentage of wrong read data is higher than the error rate threshold (10%).

Based on the fact that in an industrial application, electromagnetic disturbances can occur at random instants, the SPI-memory test includes three kinds of investigation, a flowchart of one of them is shown in Figure 2 :

- **Test mode 1**: Disturbed write, undisturbed read.
- **Test mode 2**: Undisturbed write, disturbed read.
- **Test mode 3**: Undisturbed write, 2-second disturbance, undisturbed read.

In all tests, two different data are written in two the different addresses and then, read 100 times each to ensure the measurement reproducibility.

III. Results and discussion

A. DPI measurements

For validation purposes, different experiments were performed for each memory using the same immunity criterion.

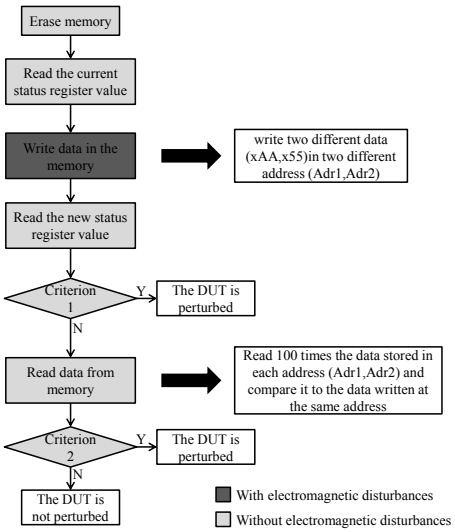


Fig. 2. Test mode 1 : Disturbed write, undisturbed read flowchart

1) Immunity vs technology: In order to compare the immunity of the selected memories, each of them have been subject to the the various tests but with the same criterion and running with the same SPI frequency (4.26 MHz).

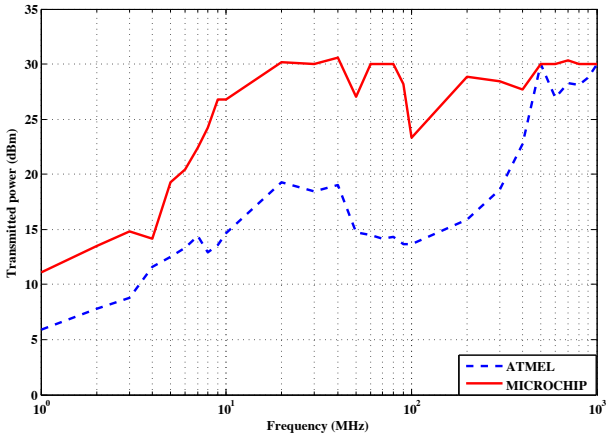
As we can see in Figure 3, even if the memories are functionally equivalent and therefore interchangeable, their susceptibility is far from being the same. The difference between the two memories immunity can be more than 10 dB at some frequencies for the same test mode. This result is fundamental for the suggested methodology since, at first glance, the *AT25512* and the *25LC512* are a priori two equivalent EEPROMs, this proves that manufacturing and design process have a big impact on the electromagnetic character of ICs.

B. simulation model

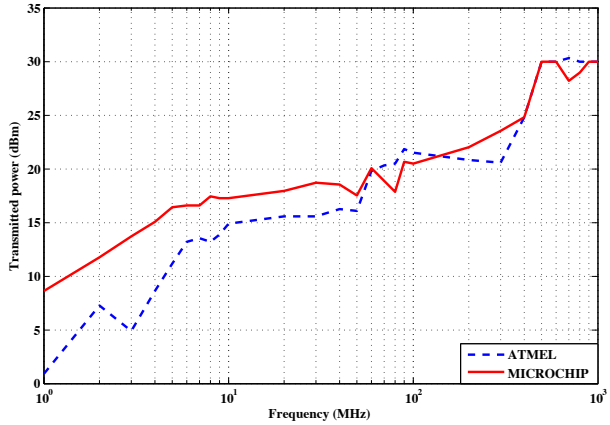
In order to confirm the measurements results, a simulation model based on the ICIM-CI standard [10] was performed on the two memories. The main objective is, the immunity prediction and validation of DPI measurements.

1) S parameters and PDN model: Lumped elements modeling of the input impedance of each component will identify the influence of PDN (*Passive Distribution Network*) on the immunity difference. The extraction of the S-parameters, by considering each pin as a port referenced to the ground pin of the IC (port 1 is the V_{dd} pin), was done with the same PCB as in DPI measurements, and a direct calibration is performed in the reference plane of the IC thanks to a custom calibration kit.

As showed in Figure 4 the MICROCHIP memory has the lowest S_{11}, it means that, if both devices have the same manufacturing and design process, more RF power is needed to disturb the ATMEL memory. To prove that same active parameters can affect the memories susceptibility, we try to evaluate the MOS capacitance of each device by measuring



(a) DPI measurement Test1



(b) DPI measurement Test2

Fig. 3. Immunity difference between both memories

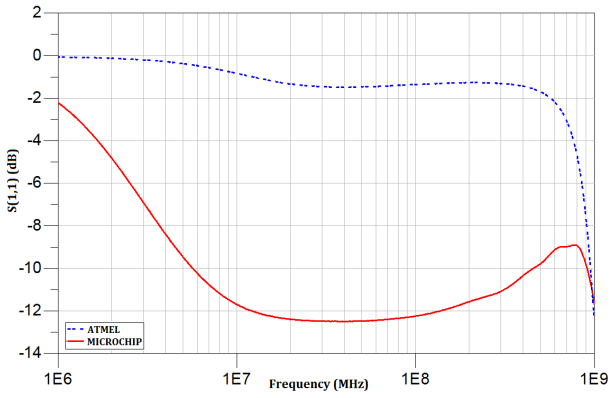
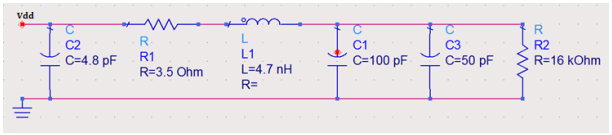
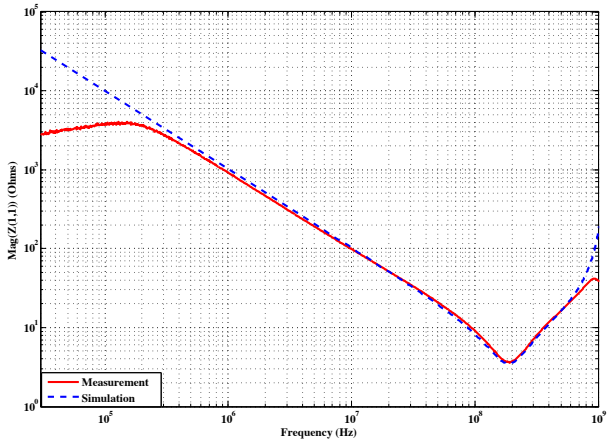


Fig. 4. S_{11} difference between ATMEL and MICROCHIP memories

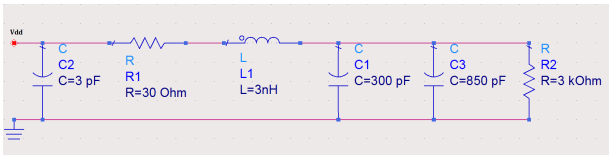


(a) Input impedance model

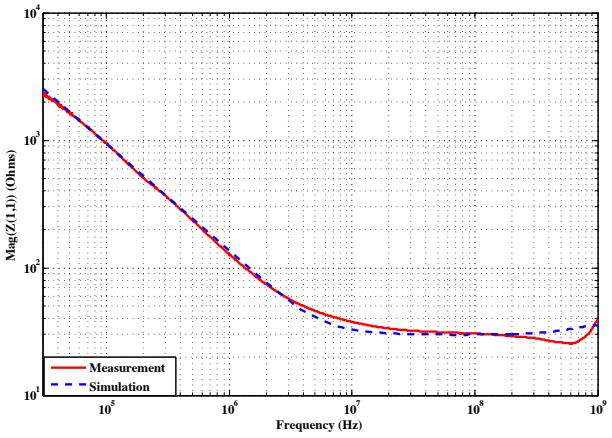


(b) Simulation of the model

Fig. 5. Measurement of the ATMEL MOS capacitance



(a) Input impedance model



(b) Simulation of the model

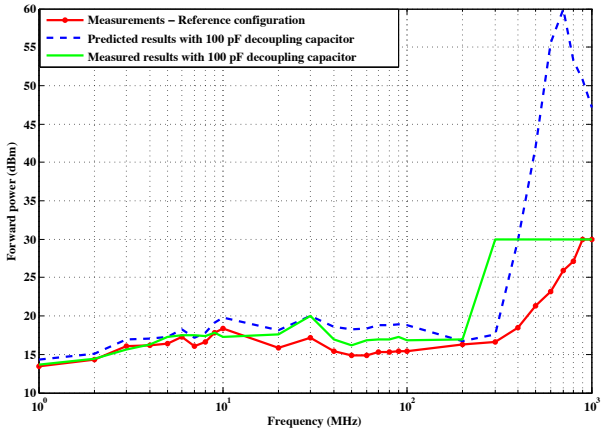
Fig. 6. Measurement of the MICROCHIP MOS capacitance

the input impedance. In fact, this capacitance can be extracted from the difference between the input impedance with and without power supply.

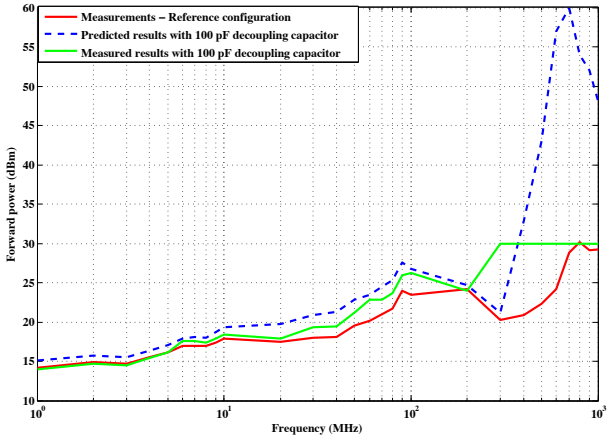
As we can see in the result showed in figure 5(a) and 6(a), the MOS capacitance *C3* is higher on the MICROCHIP memory (about 17 times).This result indicates that, the manufacturing and design process of both devices are actually different.

2) Model structure: The model structure corresponds to the current IEC standard proposal for the Integrated Circuit Immunity Model (ICIM). The first part of the model is based on a PDN structure. The second part of the model consists of a table indicating the transmitted power triggering a failure as a function of frequency.

To estimate the power transmitted to the IC, a simulation based on the modeling of a complete DPI set-up was used [11], the only difference is that, in this paper, we use an ADS simulation witch allows use of measured S-parameters. Figure 7 display the model corresponds to the SPI memories test on the V_{dd} pin in predict configuration. In the fact, the 100 pFdecoupling capacitor is added to the simulation model to predict the device immunity in other configuration and then validate the model. A significant correlation between



(a) Test 1 results



(b) Test 2 results

Fig. 8. Immunity prediction compared with DPI measurement results on the AT25512.

simulation and measurement can be noticed (Figure 8), seeing that, the DPI measurements artifacts. Based on this, we can assert that DPI measurement are correct.

It can be noted that 30 dBm corresponds to the maximum incident power fixed during the tests.

IV. Conclusion

In this paper, we described a measurement methodology of conducted immunity for SPI memories. Throughout our analysis, we made the susceptibility comparison of two EEPROM memories from different suppliers.

The measurement results showed firstly that, although the selected memories are in the same technology and also functionally equivalent, is no proof that their conducted immunity should be the same. Secondly, the S-parameters are not the best way, in this case, to find and explain the source of the immunity difference. However, modeling the input impedance was useful to prove the impact of manufacturing and design process on the conducted immunity of EEPROM SPI Memories.

Moreover, a detailed technological analysis confirmed that, manufacturing and design process of the two device is very different.

These observations must be confirmed with other technologies of non-volatile memories but, nevertheless, provide interesting perspectives for obsolescence management in EMC study.

References

[1] G. Barber and D. Herke, "Conducted susceptibility measurements on integrated circuits," in *Electromagnetic Hazards to Active Electronic Components, IEE Colloquium on*, jan 1994, pp. 4/1 –4/9.

[2] T. Sketoe, J. G.; Clark, "Integrated circuit electromagnetic immunity handbook," *NASA/CR-2000-210017, M-968, NAS 1.26:210017*, August 2000.

[3] H. Chen and J. Neely, "Interconnect and circuit modeling techniques for full-chip power supply noise analysis," *Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on*, vol. 21, no. 3, pp. 209 –215, aug 1998.

[4] W. Cui, B. Aspnes, P. Parmar, and M. Suryakumar, "Power delivery design and analysis on a network processor board," in *Electromagnetic Compatibility, 2004. EMC 2004. 2004 InternationalSymposium on*, vol. 1, aug. 2004, pp. 231 – 236 vol.1.

[5] T. Steinecke, M. Goekcen, D. Hesidenz, and A. Gstoettner, "High-accuracy emission simulation models for vlsi chips including package and printed circuit board," in *Electromagnetic Compatibility, 2007. EMC 2007. IEEE International Symposium on*, july 2007, pp. 1 –6.

[6] *IEC 62014-3: Models of integrated circuits for EMI behavioural simulation*, www.iec.ch Std., 2004.

[7] J.-L. Levant, M. Ramdani, R. Perdriau, and M. Drissi, "Emc assessment at chip and pcb level: Use of the icem model for jitter analysis in an integrated pll," *Electromagnetic Compatibility, IEEE Transactions on*, vol. 49, no. 1, pp. 182 –191, feb. 2007.

[8] *IEC 62132-4 - Integrated Circuits Measurement of Electromagnetic Immunity 150 kHz to 1 GHz Part 4: Direct RF Power Injection Method*, www.iec.ch Std., 2006.

[9] Frédéric LAFON, "Développement de techniques et de méthodologies pour la prise en compte des contraintes CEM dans la conception d'équipements du domaine automobile. Etude de l'immunité, du composant l'équipement," Ph.D. dissertation, INSA Rennes, 2011.

[10] *(Proposal) Integrated Circuit EMC modeling Part 4: ICIM-CI (Integrated Circuit Immunity Model, Conducted Immunity)*, IEC Std. 62 433-4, 2011.

[11] F. Lafon, F. de Daran, M. Ramdani, R. Perdriau, and M. Drissi, "Immunity Modeling of Integrated Circuits: an Industrial Case," vol. E93-B, no. 7, July 2010, pp. 1723–1730.

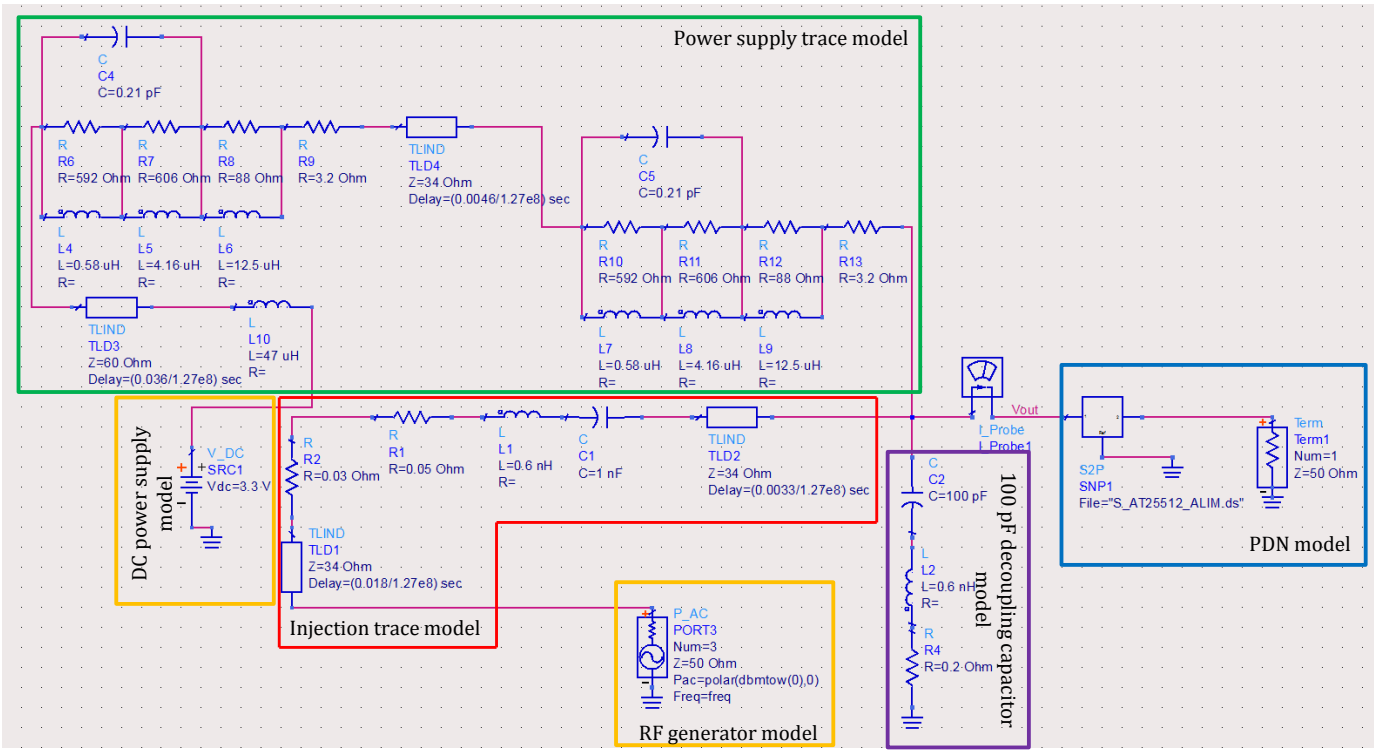


Fig. 7. Modeling of SPI memories test set-up.