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3D Multi-layer Copper Interconnects for High Performance Monolithic Devices and Passives

Ayad Ghannam, David Bourrier, Lamine Ourak, Christophe Viallon, and Thierry Parra

Abstract—This paper presents a new and efficient low-cost multi-layer 3D copper interconnect process for monolithic devices and passives. It relies on the BPN and SU-8 photoresists, associated with an optimized electroplating process to form multi-level 3D interconnects in a single metallization step. The SU-8 is used as a permanent thick dielectric layer which is patterned underneath specific locations to create the desired 3D interconnect shape. A 3D seed layer is deposited above the SU-8 and the substrate to insure 3D electroplating current flow. The BPN is used as a thick mold for copper electroplating with an aspect ratio as high as 16:1. An optimized 3D copper electroplating process is later used to grow 3D interconnects, insuring transition between all metallic layers. Finally, high-Q (55 @ 5 GHz) power inductors have been designed and integrated above a 50 W RF power LDMOS device, using this process.

Index Terms— Above-IC, BPN, Copper, Electroplating, High-Q, Inductor, Interconnect, MMIC, Process, Photoresist, SU8

I. INTRODUCTION

WITH the increasing demand for miniaturized, efficient and low-cost integrated microwave systems, manufacturers are constantly seeking new powerful low-cost integration technologies. The most demanding requirement for these technologies is the capability of integrating low-loss interconnects and passive devices, especially inductors, taking into account the nature of the substrate (resistivity and dielectric properties). Furthermore, complexity, compatibility with MMIC and process cost are major requirements for a technology, as well.

Many proposed technologies focus mainly on passive device loss enhancement. This is the case for approaches that use high resistivity silicon HRS [1], SOI [2] or organic laminates [3][4]. These technologies provide high-Q passive devices but fail to meet low-cost requirements and often need extra packaging steps for use. Silicon etching [5], ground shield patterning [6][7], spacers [8] and micromachining for

suspended planar or 3D structures [9]-[12] are other technologies that enable direct above-IC integration of high-Q inductors. However, these approaches are either complex and expensive or incompatible with standard silicon technologies which use low resistivity substrate. Therefore, they fail to fulfill current industrial demands. Alternative technologies, like 3D-MMIC [13]-[16], look promising especially because they address both miniaturization and passive device performance enhancement. However, their complexity, cost and processing time increase rapidly with each additional dielectric or metallic layer, thus hindering their large scale usage. Moreover, as the performance of passive devices is severely limited by relatively thin dielectric layers, stacks of several dielectric layers are required to compensate. This stacking often induces a high residual stress on the wafer, which can be problematic if the substrate is later thinned. Furthermore, the presence of seed layer at the interface between interconnects could reduce the reliability of the device under mechanical stress (resulting from backside wafer thinning, for example). In specific cases, these technologies require mechanical polishing steps in order to planarize the dielectric layer and prevent thickness homogeneity-related problems.

This paper presents an efficient multi-layer 3D copper interconnect process that overcomes all previous drawbacks. Low-cost and compatible with standard lithography and electroplating techniques, the industrial implementation of this process is easy and straightforward. The process relies on dielectric patterning, 3D seed layer deposit and 3D copper electroplating to form 3D interconnects or 3D passive devices in a single metallization step. As a result, the process offers the following advantages:

- Reduced number of technological steps
- Reduced manufacturing time and cost
- Dielectric mechanical polishing eliminate (if previously present)
- Reduced residual stress
- Enhanced reliability

In addition to technological advantages, High-Q and high inductance density interconnects and inductive devices can be fabricated using this new approach (§ IV).

The process technological steps are presented in the following section. An example of implementation of this process is then described in the third section, which deals with high-Q 3D interconnected pre-matching inductors integration

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above a 50 W RF LDMOS transistor. Finally, the process capability for integrating high-Q 3D inductors is discussed in the fourth section.

This paper complements previously published results [17] as it further discusses the technological steps and adds new material regarding inductor Q-factor enhancement. It also introduces new capabilities of the process.

II. 3D INTERCONNECT PROCESS

A. Process Overview

The key benefit of the here proposed process is based on growing multi-level 3D copper interconnects using a single metal electroplating step. Interconnects and vias are grown at the same time ensuring electrical connection with underlying metallic layers. Vias are Through Polymer Vias (TPV) since they are integrated through a polymer layer deposited on top of the substrate.

Electroplating 3D multi-level interconnects requires four main steps, compared to a minimum of 10 in other similar approaches, which are: 1/ the deposit and the selective patterning under specific locations of a dielectric polymer on top of the substrate; 2/ the deposit of a void-free 3D seed layer; 3/ the deposit and the patterning of a high aspect ratio thick photoresist mold; and 4/ 3D single step copper electroplating. Fig. 1 illustrates a process flow for integrating a 3D interconnected inductor.

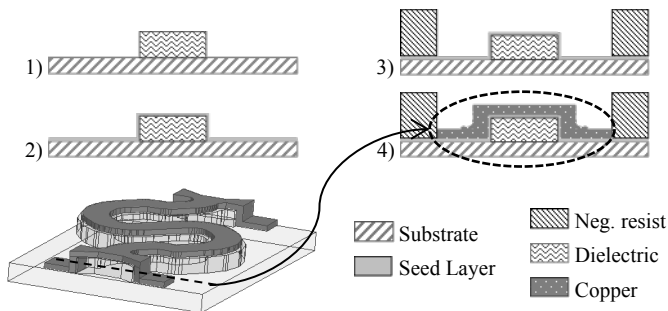


Fig. 1. 3D interconnected inductor integration steps using the proposed process.

B. Dielectric Layer

The dielectric layer represents a principal feature of the process. As illustrated in Fig. 2a, the dielectric can be patterned and kept only under metallic strips allowing their elevation from the substrate while enabling direct access to the underlying metallic patterns.

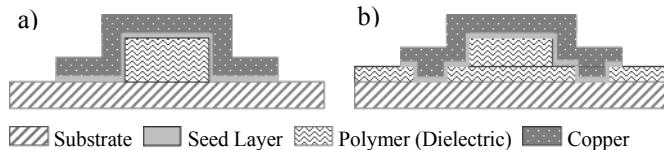


Fig. 2. Methods of forming 3D interconnects: a) with a single dielectric layer. b) with two dielectric layers.

The process is not limited to a single dielectric layer. If needed, by simply adding additional dielectric layers, metallic patterns can be grown at different distances from the substrate and interconnected together in a single electroplating step, as

shown on Fig. 2b. The example depicted in this figure uses two dielectric layers: the first is deposited on the entire wafer surface and is combined with via openings to allow connections with the bottom metallic level, while the second is located only under the required upper metallic pattern and can be simply connected to lower levels, as previously described. This kind of topology is challenging for seed layer deposit as highlighted in the next paragraph.

If compared with 2.5D interconnect technologies where vias are electroplated before the deposition of the dielectric layer, this process offers the following advantages:

- Elimination of the mechanical polishing step used for dielectric surface planarization. This step is often required since the presence of metallic pillars generates waves during the polymer (dielectric) spin-coating.
- Reduction of mechanical strain applied to the substrate by means of the dielectric patterning. Depending on density and shape of interconnects, the ratio between dielectric and substrate surfaces can be often widely reduced. It can be even decreased to nearly 2% in many cases.

The material used as a dielectric layer can be any photosensitive spin-coated or laminated dry-film polymer (BCB, polyimide, SU-8...). For this work, the SU-8 negative photoresist has been chosen as a result of its attractive technological properties and its good electrical characteristics for frequencies up to 7 GHz [18]. Furthermore, this resist, spun or spread over thicknesses ranging from a few to several hundreds of micrometers, can achieve high aspect ratio features (above 10:1) with vertical sidewalls, and still be processed with standard contact lithography. Vertical sidewalls make the SU-8 choice challenging for 3D seed layer deposit, especially for thicknesses greater than 50 μm . Once this challenge is overcome, any other polymer can be used regardless of its sidewall profile.

TABLE I
SU-8 PROCESS FOR TWO THICKNESSES

Step	Thickness	45 μm	90 μm
	Coating		SU-8 3025 3000 RPM 30s
Pre-exposure bake		1 min at 65 $^{\circ}\text{C}$ 30 min at 95 $^{\circ}\text{C}$	1 min at 65 $^{\circ}\text{C}$ 44 min at 95 $^{\circ}\text{C}$
Exposure (UV)		220 mJ/cm^2	360 mJ/cm^2
Post-exposure bake		1 min at 65 $^{\circ}\text{C}$ 3 min at 95 $^{\circ}\text{C}$ Ramp down to 25 $^{\circ}\text{C}$	1 min at 65 $^{\circ}\text{C}$ 3 min at 95 $^{\circ}\text{C}$ Ramp down to 25 $^{\circ}\text{C}$
Development		PGMEA 12 min	PGMEA 15 min
Hard bake		1 min at 65 $^{\circ}\text{C}$ 2 min at 125 $^{\circ}\text{C}$	1 min at 65 $^{\circ}\text{C}$ 2 min at 125 $^{\circ}\text{C}$

The SU-8 lithography process includes six steps : 1/ spin-coating, 2/ pre-exposure bake, 3/ exposure, 4/ post-exposure bake (PEB), 5/ development and 6/ hard bake. In order to reduce the tensile stress of the SU-8 and to avoid cracks, the

temperature must be ramped down to 25 °C at the end of the PEB cycle.

Table I summarizes details of the process used to spin-coat 45 μ m or 90 μ m thick SU-8 layer.

C. 3D Seed Layer

For single step 3D copper electroplating, a 3D seed layer must be deposited to ensure the electrical continuity all the metallic layers to be connected, from the substrate to the upper dielectric surface (Fig. 2). As already mentioned, this step translates into a great challenge because of the vertical SU8 sidewalls. Furthermore, depending on the pattern nature (pillars or hollows), size and density, as well as the equipment used (evaporation, sputtering), the ease of seed layer deposit can vary widely. In fact, if an evaporation technique is used, the presence of a high vertical sidewall might create a shadow effect. The result is a locally thinned or even deleted (void) seed layer (left part of Fig. 3) that fuses when applying the electroplating current. A sputtering technique can enhance the homogeneity of seed layer thickness. However, in some severe cases, like the presence of narrow hollows (Fig. 2b), seed layer enhancement (SLE) [19] approaches must be used. SLE, typically used in Through Silicon Vias (TSV) applications [20]-[23], is prepared using a chemical solution for deposition of a thin 3D conductive layer on all surfaces. While originally dedicated to silicon substrates, this technique has now been extended to polymer substrates.

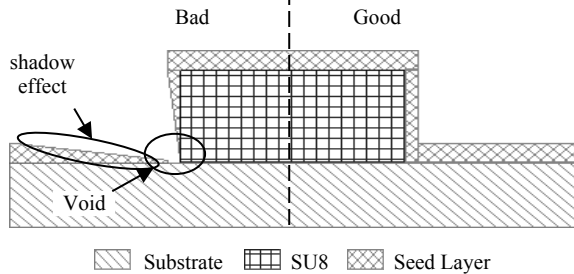


Fig. 3. Cross-sectional view illustrating 3D seed layer deposit difficulties

When the seed layer is homogenous (right part of Fig. 3), electroplating currents flow in a 3D way allowing copper to grow on all exposed surfaces and sidewalls which are bound into the electroplating mold.

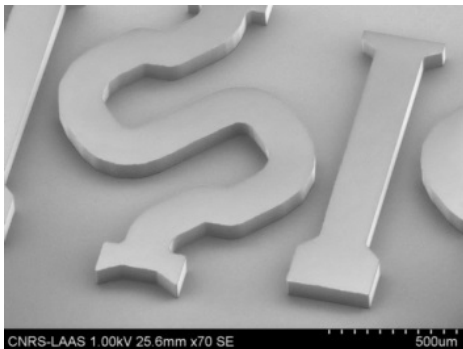


Fig. 4. 3D Ti/Cu seed layer deposited over a single SU-8 layer.

During process development, several metals and pieces of

equipment were used to find the best result. Experiments employing Titanium, Tantalum, Copper and Gold were performed using electron cannon evaporation (Varian 3616) and physical vapor deposition sputtering cluster (Univex 450C). For this test, two SU-8 layers with a total thickness of 90 μ m have been used. The results (Table II) show that a thickness of 1000/2000 Å of either titanium/copper (Ti/Cu) or titanium/gold (Ti/Au) produces a uniform, void-free 3D seed layer (Fig. 4). This result is valid for both evaporation and sputtering techniques. However, sputtering may be preferred when via holes are implemented in the dielectric layer since it yields a good 3D coverage in hollow features. This is due to the higher energy of deposited metal atoms as compared to evaporation technique.

Fig. 5a shows a 500/1000 Å thick evaporated Ti/Cu seed layer before SLE and after SLE (Fig. 5b & c). Note that the thin seed layer on the SU-8 sidewalls is corrected after SLE thus enhancing its uniformity.

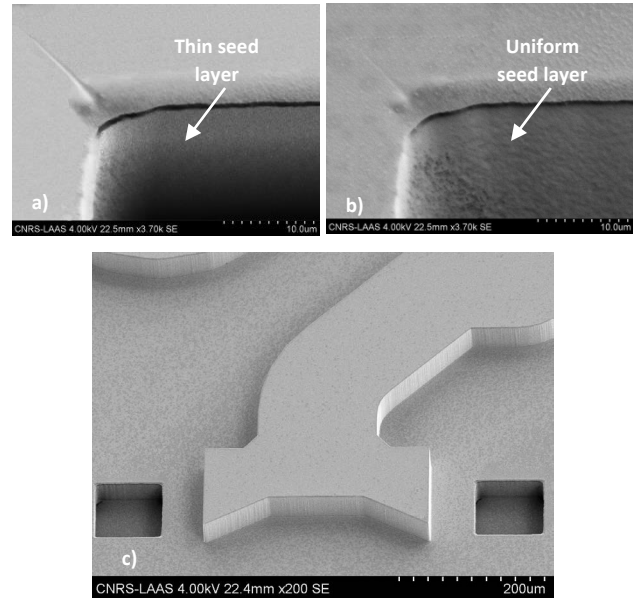


Fig. 5. SEM micrograph of a 500/1000 Å thick evaporated Ti/Cu seed layer: a) before SLE, b and c) after SLE.

TABLE II
RESULT OF DIFFERENT SEED LAYER TESTS ACCORDING TO METAL TYPE, THICKNESS AND USED EQUIPMENT

Seed layer	Thickness	Evaporation	Sputtering	Result
Ti/Cu	500/500 Å	X		Thin + Voids
Ti/Cu	500/1000 Å	X		Voids
Ti/Cu	1000/2000 Å	X		Good coverage
Ta/Cu	500/1000 Å		X	Cracked
Ti/Au	1000/2000 Å		X	Excellent coverage
Ti/Au	1000/2000 Å	X		Good coverage

D. Photoresist for thick molds

Since the patterned dielectric (SU-8) remains only in specific locations, the photoresist used for mold formation

must present the following abilities:

- high thicknesses: the thickness of photoresist must be larger than the sum of the dielectric and copper thicknesses. For example, if the dielectric is $90\ \mu\text{m}$ thick and the required copper thickness is $10\ \mu\text{m}$, the depth of the mold must be greater than $100\ \mu\text{m}$.
- high resolution: the photoresist must reach a high aspect ratio, because this ratio determines the minimum width which can be integrated for interconnects.

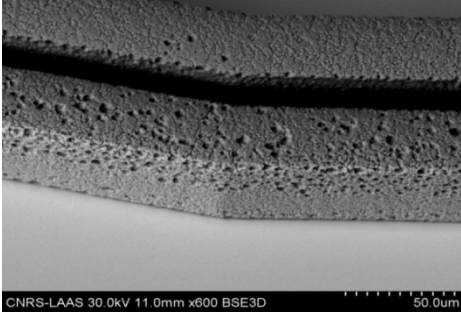


Fig. 6. Damaged copper surface after plasma etch of $90\ \mu\text{m}$ thick SU-8.

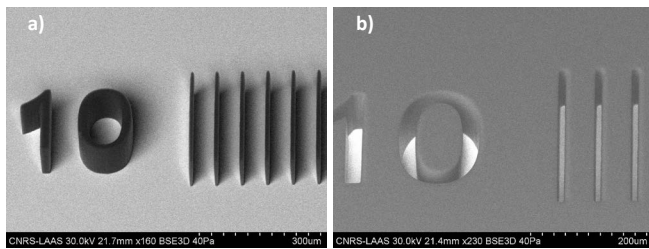


Fig. 7. SEM micrograph showing the BPN high aspect ratio, achieved after optimization. a) lines, b) openings.

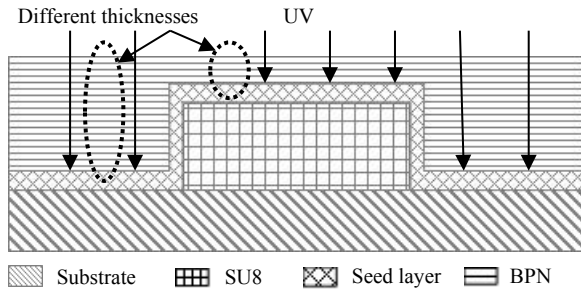


Fig. 8. Illustration of BPN lithography process challenge.

Unfortunately, since the process is intended to be used for a wide range of dielectric thicknesses (from $10\ \mu\text{m}$ up to $150\ \mu\text{m}$), few photoresists are able to fulfill these requirements. Of available possibilities, SU-8 and BPN photoresists appear to be the best candidates. The use of SU-8 as a mold was quickly discarded since etching this photoresist is difficult and cannot be performed without damaging surrounding metallizations (Fig. 6). The BPN photoresist offers a better alternative since it can be easily stripped using an *N*-methyl pyrrolidinone (NMP) based stripper [24]. The stripper, heated at $50\ ^\circ\text{C}$, selectively dissolves the BPN without damaging surrounding materials. Though this photoresist is commercialized with a low aspect ratio (2:1) compared to the SU-8, optimization of the BPN-based process

yielded an aspect ratio as high as 16:1 [25], permitting its adoption for this process (Fig. 7).

The BPN lithography process includes four steps: 1/ spin-coating of the resist, 2/ pre-exposure bake, 3/ UV exposure, 4/ development. The main challenge consists in finding all proper values for annealing temperature and time, for UV dose and for development time, taking into account the difference in thickness caused by the presence of SU-8 pillars and hollows inside the BPN layer. Fig. 8 shows that the BPN is thinner when it is located on top of an SU-8 pattern. Given the fact that both thicknesses receive the same UV dose, the thinner BPN layer is over-exposed. This effect has been studied by integrating metallic ribbons of $25\ \mu\text{m}$ width which step over the $45\ \mu\text{m}$ thick SU-8 pillar. A $100\ \mu\text{m}$ thick BPN layer is deposited and insulated with a UV dose of $1350\ \text{mJ}/\text{cm}^2$. After copper electroplating, the measured widths of these ribbons are $22.5\ \mu\text{m}$ and $25.5\ \mu\text{m}$ at the top and bottom, respectively (Fig. 9a). However, since the BPN sensitivity is low, the impact of the over-exposure on the width of the top metallic strips is low as shown (Fig. 9a). This phenomenon can be predicted using a simplified exposure model [26] for vertical UV lithography (Fig. 9b) and if needed, optical proximity correction (OPC) [27] can be applied. Fig. 9b shows the predicted wall profile of BPN and the change in offset of the feature edge. For the bottom level (BPN over substrate), the offset of the feature shifted $-0.2\ \mu\text{m}$ on each side, resulting in an increase of the line width of $0.4\ \mu\text{m}$ since the BPN is a negative photoresist (Fig. 9c). For the top level (BPN over SU-8), the offset of the feature shifted $1.25\ \mu\text{m}$ on each side, resulting in a decrease of the line width of $2.5\ \mu\text{m}$ (Fig. 9c), in a good agreement with measured line widths.

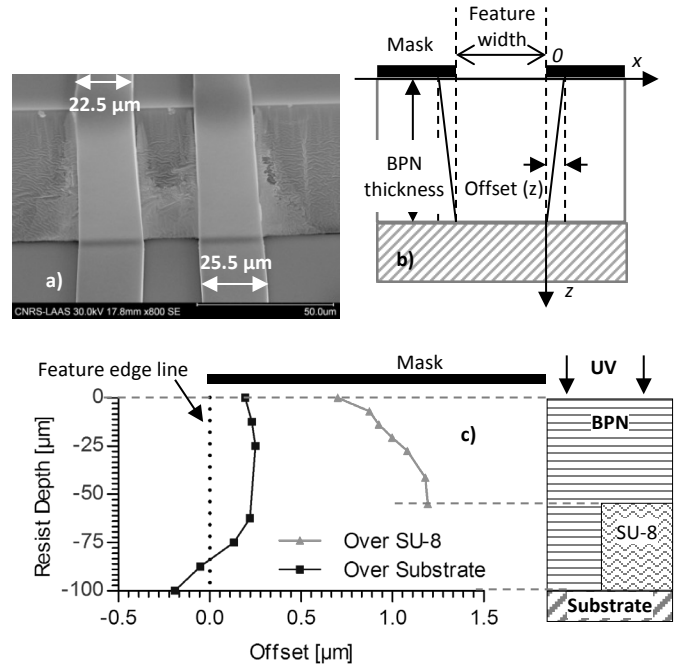


Fig. 9. a) Effect of UV exposure on strip width, b) schematic drawing of vertical UV lithography c) offset as a function of resist depth and insulated BPN thickness.

Table III summarizes process details used to spin-coat a $100\ \mu\text{m}$ or $160\ \mu\text{m}$ thick BPN layer.

TABLE III
BPN PROCESSES FOR DIFFERENT THICKNESSES

Step	100 μm	160 μm
Coating	BPN 65A 750 RPM 30s	BPN 100A 500 RPM 30s
Pre-exposure bake	3 min at 65 °C 3 min 30 at 120 °C	3 min at 60 °C 5 min at 120 °C
Exposure (UV)	1350 mj/cm ²	2500 mj/cm ²
Development	TMAH 6 min	TMAH 10 min

E. Copper electroplating process

The aim of this work is the development of a 3D interconnect process based on a single copper electroplating step. Although previous process steps are crucial to obtain the 3D shape, the electroplating process itself is of equal importance, since it must be capable of properly filling the vias and forming interconnects, simultaneously. The electroplating requirements are similar to those of TSV technologies. Therefore, extensive work has been done to properly set all electroplating parameters, including electrolytic bath concentration, current density and electroplating temperature.

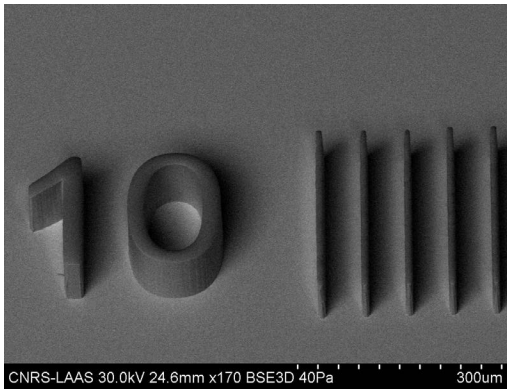


Fig. 10. SEM micrograph of copper patterns after electroplating inside 100 μm thick BPN molds.

During this study, electroplating was carried out using an RENA deposition reactor. Electroplating tests, from a bath containing 25 g/L copper, have been carried out at 25 °C with current densities ranging from 0.5 to 6 A/dm². Fig. 10 shows that the current density of 2 A/dm² yields the best results since the BPN molds are not damaged during copper electroplating. Once the current density is set, the required copper thickness is reached by adjusting electroplating time.

III. EXPERIMENTAL RESULTS

A. Process validation

After validation of each technological step, two-level 3D test interconnects are fabricated using the proposed process. The fabricated structures involve two 45 μm thick SU-8 layers (total thickness 90 μm) and 20 μm thick copper lines, with interconnections between both levels (Fig. 11). This implementation is performed using the following

technological sequence:

1. Deposition and patterning of the first 45 μm thick SU-8 layer on the entire wafer to create via openings for connections to metallic pads on the substrate
2. Deposition and patterning of the second 45 μm thick SU-8 layer
3. Evaporation of a 1000/2000 Å thick Ti/Cu seed layer
4. Deposition and patterning of a 160 μm thick BPN layer to create molds for copper electroplating
5. Electroplating of 20 μm thick copper
6. Dissolving of BPN and etching of seed layer

Fig. 11 shows the good continuity of metallization among all levels, from substrate to the upper metal level while stepping over a dielectric vertical wall, validating thus the developed process.

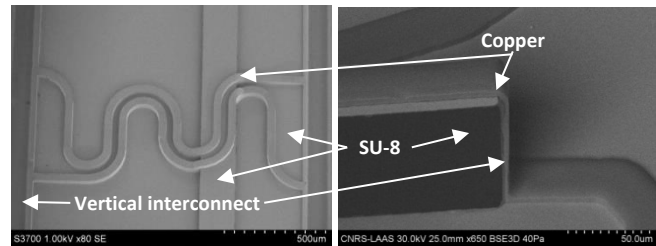


Fig. 11. SEM micrographs of two-level 3D interconnects fabricated using the process.

B. Interconnected inductors above a 50 W RF LDMOS

After process validation, 3D interconnected high-Q inductors are designed and integrated above 50 W RF LDMOS transistors as pre-matching network elements. Because of its high levels, the current must be distributed along the power transistor's drain electrode. For this purpose, several inductors are implemented in parallel, and each connection is distributed between two accesses (Fig. 12- Fig. 13). Two versions are fabricated: the first involves a 90 μm thick SU-8 layer located only under inductors; the second is based on two SU-8 layers (for a 90 μm total thickness) with the first layer kept on the entire wafer surface (pillar/hollow combination). The aim of the second version is to demonstrate the process capability of managing 3D transitions, since in this second version, copper electroplates with currents in upward and downward directions, simultaneously.

Inductors integrated over a single SU-8 layer require only two lithography masks whereas the second variation requires an additional mask for vias. The integration process outlined previously in § III.A is applied, except for the first step which is irrelevant in the single SU-8 layer version.

Fig. 12a shows the BPN molds whereas Fig. 12b shows cross-sections of the single step 3D electroplated copper for both versions. One can observe the excellent metallic structure continuity in both cases, as well as good filling of the vias in the version based on two SU-8 layers. Fig. 13 presents the inductors as applied above the 50 W RF LDMOS transistor and the cross-sectional view of the electrical connection between inductors and transistors.

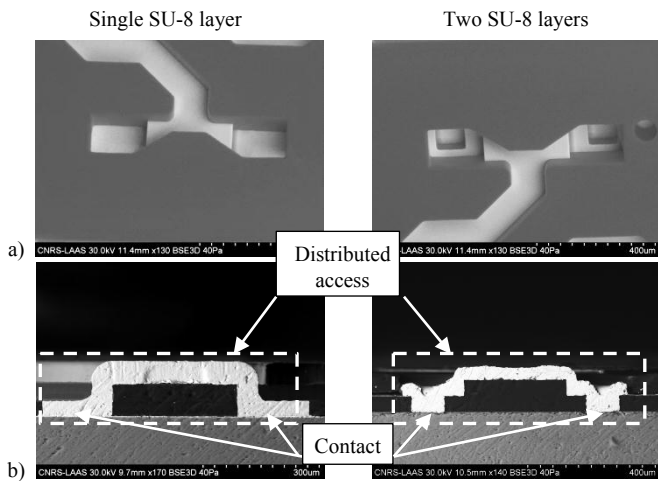


Fig. 12. SEM micrographs of: a) BPN molds, b) 3D electroplated copper cross-sectional view in contact plane.

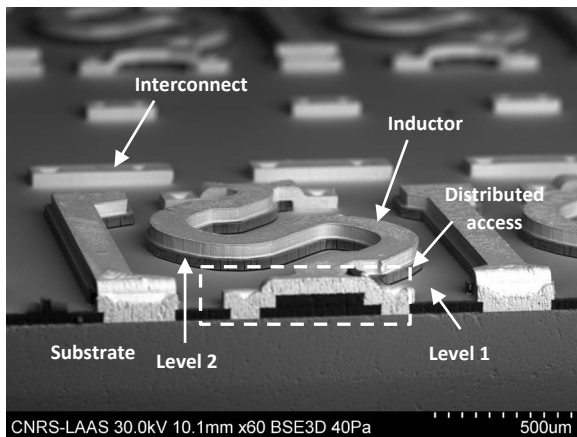


Fig. 13. 3D interconnected inductors integrated above a 50 W LDMOS transistor.

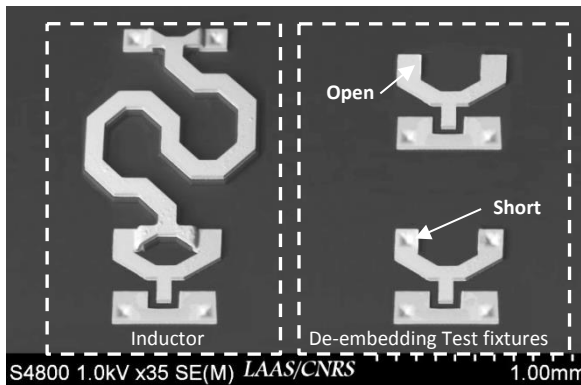


Fig. 14. SEM micrograph of DUT (inductor with distributed access) and test fixtures required for de-embedding.

Stand-alone RF performances of inductors are assessed from structures including CPW probe pads, which are designed and integrated above a low resistivity silicon substrate ($8 \text{ m}\Omega\cdot\text{cm}$) simulating the LDMOS's environment (Fig. 14). For such a resistivity value, a solid ground shield, integrated on top of the substrate, is required in order to limit bulk electromagnetic losses. A vector network analyzer (Anritsu 37397C) and a probe station are used for microwave

on-wafer S-parameter measurements up to 20 GHz. A SOLT calibration is performed to locate reference planes at probe tips and on-wafer open/short test fixtures are used to deembed the probing pads.

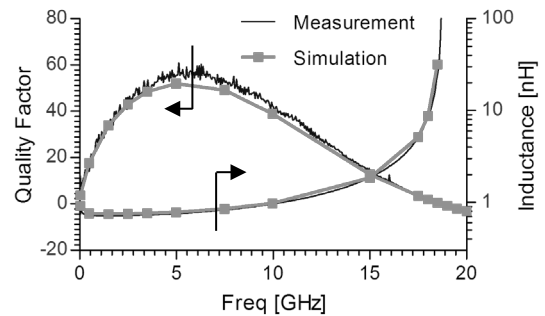


Fig. 15. Q-factor and inductance measured and simulated values versus frequency of an inductor on low resistivity silicon substrate ($8 \text{ m}\Omega\cdot\text{cm}$).

One-port measurements of these inductors exhibit a maximum Q (Q_{\max}) value of 55 at 5 GHz for a total inductance value of 0.8 nH (Fig. 15). The good agreement between measurements and simulations must be pointed out, which validates both inductor optimization and the technological process control.

Load-pull measurements of the pre-matched RF LDMOS transistor at 1.85 GHz yield a maximum output power ($P_{\text{out, max}}$) of 48.5 dBm, a maximum gain ($G_{T, \text{max}}$) of 14.75 dB and a maximum efficiency (η_{\max}) of 54%. An efficiency only 5% lower than the bond-wired version of the transistor is noticed. This small decrease has been traced and appears to be caused by a higher source resistance due to back-side metal processing. Therefore, one can conclude that the proposed process results in integrated planar inductors which can compete with bond-wires.

IV. PROCESS INTEGRATION

To further demonstrate process capabilities, electromagnetic simulations (EM) with Ansoft HFSS software are carried out when the previously presented inductor is integrated on a silicon high resistivity substrate (HRS). In this case, the ground plane implemented as a shielding between the inductor and the low resistivity substrate is no longer required (Fig. 16), whereas the SU-8 layer is still useful to keep the self-resonant frequency as high as possible (because its relative dielectric constant value is about 4, parasitic capacitances are lowered). Fig. 17 demonstrates that on a silicon HRS and by removing the ground shield, Q_{\max} increases from 55 to 112 while the inductance also increases from 0.8 nH to 1.6 nH . Using this process, a 3D solenoid inductor of 4 turns has been fabricated. Results in Table IV are compared to published values of Q_{\max} , self resonant frequency (SRF) and inductance density. Even though Q_{\max} values must be compared with caution, since they greatly depend on the inductance value, the here proposed low-cost process appears very attractive for high-Q inductor fabrication, since it gives the best Q_{\max} and inductance density.

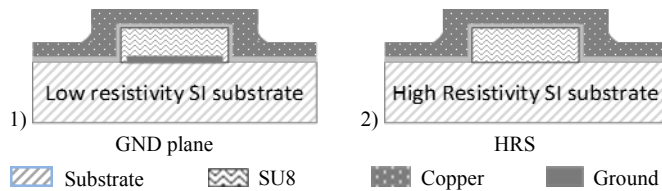


Fig. 16. Structure setup for EM simulation.

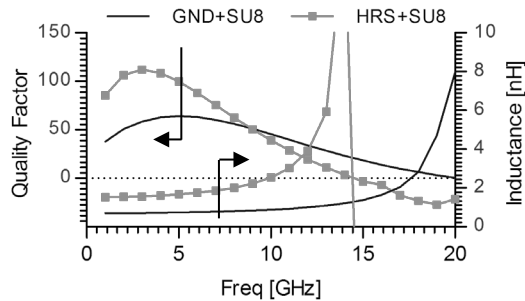


Fig. 17. Evolution of Q-factor and inductance values when a silicon HRS (5 kΩ.cm) is used and the ground shield is removed.

TABLE IV
SUMMARY OF 3D INTEGRATED INDUCTORS

	L (nH)	Q_{max}	SRF (GHz)	Dimensions: X x Y x Z (μm)	L density (nH/mm^3)
This work	1.1	70	31	170 x 225 x 90	320
[8]	34	10	1.96	820 x 820 x 200	250
[10]	2.58	36	17.84	390 x 390 x 70	235
[28]	2.6	20.5	-	400 x 600 x 50	215
[12]	0.84	52	31.8	140 x 450 x 70	190
[3]	17.7	65	2.56	1525 x 1550 x 760	9.9

This process is also suited for system in package (SiP) applications. Several MMIC chips, which have been mounted on a blank substrate, can be interconnected together while high-Q passives are integrated on the substrate or above IC (Fig. 18). This solution, which requires few operations and technological steps, simplifies chip to chip RF connections, and enhances miniaturization while reducing costs, is thus a good alternative to current bond-wires or flip-chip solutions.

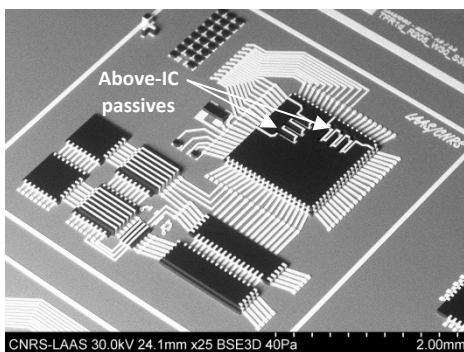


Fig. 18. Illustration of chip to chip interconnection using the proposed process.

V. CONCLUSION

A low-cost multi-level copper interconnect process is presented in this paper. This process relies mainly on the patterning of SU8-based dielectric and on single step 3D copper electroplating inside thick BPN photoresist molds. It features a reduced number of technological steps which allow integration of high performance low-cost 3D interconnects for microwave and/or power applications. This technology has been validated by integrating 3D interconnected inductors on a 90 μm thick SU-8 dielectric layer deposited over a very low resistivity silicon substrate. An excellent electroforming of 3D copper ribbons was observed, and inductor measurements revealed a Q of 55 at 5 GHz for an inductance of 0.8 nH. These inductors have been successfully integrated above a 50 W RF LDMOS whose characterization demonstrates that the 3D interconnected planar inductors can compete with bond-wires. Additional results show that inductor performances can be enhanced, as well, if a high resistivity substrate is used, since in this case the same inductors exhibit a value of 1.6 nH and a maximum Q of 112. Finally, this process is applied for the interconnection of MMIC chips.

Thus, the proposed technology appears to be a very promising integration solution for many applications, including on-chip antenna, 3D inductor or balun/transformer solenoids, as well as for SiP packaging. It is also fully compatible with standard IC manufacturing equipment.

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