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Fixed-Point Implementation of an Efficient Low-Complexity Turbo-Equalization Scheme

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Abstract: *This paper investigates the realization of an efficient low-complexity turbo-equalizer under fixed-point data representation and computation constraints. We address the quantization issues that arise in the receiver design, and expose a simple computation procedure for the equalizer coefficients. The proposed solution is well-suited for a DSP implementation on low cost 16 bits fixed-point devices such as Texas Instrument next generation C55x platform. The simulation results show a performance loss of 0.2 dB in comparison with the ideal unquantized receiver on a specific channel model.*¹

Keywords: turbo-equalization, fixed-point implementation, DSP, ISI channels

1. INTRODUCTION

Following the growing interest in iterative “turbo” processing techniques, turbo-equalization pioneered in [1] has emerged as an attractive solution to combat intersymbol interference (ISI) over frequency selective channels. The optimal turbo-equalizer uses the BCJR-MAP Soft-In/Soft-Out (SISO) equalizer [2], whose complexity prohibits a practical implementation when considering multilevel signaling over long delay spread channels. Research efforts have thus been devoted to the design of efficient low-complexity SISO equalizers, which either employ reduced-states trellis-based algorithms (see *e.g.* [3]) or linear filtering operations [4]. Among the latter class, the minimum mean-square error *Interference Canceller - Linear Equalizer* (MMSE IC-LE) proposed in [5] realizes an attractive receiver for single-carrier wireless broadband transmissions in severe multipaths environments. Building upon the respective works of [6] and [7], the MMSE IC-LE generalizes the classical MMSE linear equalizer by exploiting the reliability of *a priori* information to modify the equalization strategy accordingly. The overall complexity of the MMSE IC-LE is essentially linear with the length of the channel impulse response and the constellation size.

We focus in this paper on the fixed-point realization of a turbo-equalization scheme relying on the MMSE IC-LE. Data quantization issues and algorithmic choices are emphasized in the framework of a simple transmission

scheme. This work constitutes the preliminary step towards a DSP implementation of this receiver. The envisioned target is Texas Instrument TMS320C55x device, a low cost and low power consumption 16 bits fixed-point platform, optimized for embedded communications systems such as GPRS receivers for example.

2. SYSTEM DESCRIPTION

2.1. Transmission scheme

We will consider in the following a bit-interleaved coded modulation (BICM) scheme. Frames of information bits b_k are encoded by a rate $1/2$ recursive systematic convolutional (RSC) encoder with memory 2 and octal generator polynomials $(1, 5/7)_8$. Tailbits are appended to ensure zero-state trellis termination. The coded bits c_k are interleaved according to a pseudo-random permutation function, grouped and mapped onto discrete complex symbols x_n with zero mean and variance σ_x^2 . We shall focus on a BPSK signal set in this example, although higher-order PSK or QAM modulation schemes may be considered as well [8]. The resulting symbols are then modulated and transmitted over a frequency selective channel on a burst-by-burst basis. The channel is assumed invariant along the burst duration. An appropriate guard interval is inserted between successive bursts to prevent inter-block interference at the receiver side.

We assume a coherent receiver front-end and perfect synchronization, such that the cascade of the transmit filter, the transmission over the channel, the receiver filter and of the symbol-rate sampling device may be represented by an equivalent discrete-time baseband channel, modelled as a FIR filter with L complex coefficients h_k . Following this convention, the observation received at time n may be written as :

$$y_n = \sum_{k=0}^{L-1} h_k x_{n-k} + w_n \quad (1)$$

where w_n denote white gaussian noise samples with zero mean and variance σ_w^2 .

2.2. Iterative receiver

The turbo-equalization scheme is depicted in figure 1. The SISO equalizer delivers extrinsic information $L_e^E(c_n)$

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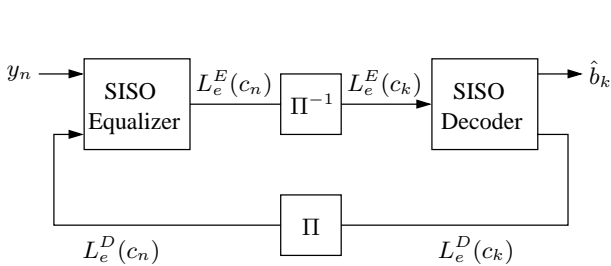


Figure 1: The turbo-equalization scheme

on the coded bits, which are deinterleaved and passed to the channel decoder. This one generates in turn hard decisions \hat{b}_k on the information sequence, as well as updated extrinsic information $L_e^D(c_k)$ on the coded bits. The quantities $L_e^D(c_k)$ are then interleaved and fed back to the equalizer where they are exploited as *a priori* information for a new equalization attempt. Iterating the process a few times usually improves significantly the receiver performance.

2.3. The MMSE IC-LE

The overall structure of the MMSE IC-LE is depicted in figure 2. It comprises a soft symbol mapping module (labelled SoMAP) and an interference cancellation structure composed of two transversal FIR filters with frequency responses $P(\omega)$ and $Q(\omega)$, followed by a SISO symbol demapping function (labelled SoDEM). A full description of the equalizer is provided in [5] and thus omitted here for the sake of brevity. We shall only recall the results pertaining to the implementation.

The SoMAP module generates soft symbol estimates a_n . They are computed as the expected value of the transmitted symbols, with respect to prior probabilities derived from the soft values delivered by the decoder at the previous iteration. In the BPSK case, assuming that $L_e^D(c_n)$ relates to the symbol x_n , we get :

$$a_n = \sigma_x \tanh(L_e^D(c_n)/2) \quad (2)$$

The SoMAP module also computes the normalized variance $\rho = E(|a_n|^2)/\sigma_x^2$, which is used in the computation of the filters coefficients. At the first iteration, no prior information is available and thus $L_e^D(c_n) = 0$, $a_n = 0$ and $\rho = 0$. As the reliability of the soft values increases across the iterative process, $a_n \rightarrow x_n$ and $\rho \rightarrow 1$.

The core of the MMSE IC-LE lies in the interference cancellation structure. The equalized sample at time n is given by :

$$z_n = \sum_k p_k y_{n-k} - \sum_l q_l a_{n-l} \quad (3)$$

where we impose the condition $q_0 = 0$ to prevent the subtraction of the desired signal. The filters coefficients

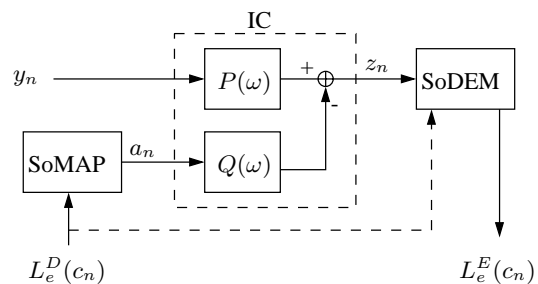


Figure 2: Structure of the MMSE IC-LE

are optimized according to the minimization of the mean-square error $E(|z_n - x_n|^2)$. The computation exploits the knowledge of the normalized variance ρ of the soft symbol estimates. Define $\text{SNR} = \sigma_x^2 \|h\|^2 / \sigma_w^2$ with $\|h\|^2 = \sum_{k=0}^{L-1} |h_k|^2$. Introducing the Fourier transform $H(\omega)$ of the channel impulse response, we finally obtain :

$$P(\omega) = \frac{1}{1 + \beta\rho} \frac{H^*(\omega)}{(1 - \rho)|H(\omega)|^2 + 1/\text{SNR}} \quad (4)$$

with

$$\beta = \frac{1}{2\pi} \int_{-\pi}^{+\pi} \frac{|H(\omega)|^2}{(1 - \rho)|H(\omega)|^2 + 1/\text{SNR}} d\omega \quad (5)$$

and, defining $G(\omega) = P(\omega)H(\omega)$,

$$Q(\omega) = G(\omega) - g_0, \quad g_0 \triangleq \frac{1}{2\pi} \int_{-\pi}^{+\pi} G(\omega) d\omega \quad (6)$$

The optimum filters have infinite-length and must be approximated in a practical implementation. A low complexity computation procedure for the filters coefficients will be exposed in the next section. Note that when $\rho \rightarrow 0$, the IC-LE reduces to the classical MMSE linear equalizer. In contrast, it converges towards the ideal MMSE interference canceller which achieves the matched-filter bound when $\rho \rightarrow 1$.

The SoDEM module finally delivers extrinsic information $L_e^E(c_n)$ computed both from the knowledge of the equalized sample z_n and (for high-order modulation schemes) from the prior soft values $L_e^E(c_n)$. Let us decompose the equalized sample as :

$$z_n = g_0 x_n + \nu_n \quad (7)$$

where ν_n denote the residual noise + interference term at the canceller output. The SoDEM module implements a SISO symbol demapping function under the assumption that ν_n is gaussian with variance σ_ν^2 [8]. It can be shown that $\sigma_\nu^2 = \sigma_x^2 g_0 (1 - g_0)$. $L_e^E(c_n)$ may thus be expressed in the BPSK case as :

$$L_e^E(c_n) = \frac{4g_0}{\sigma_\nu^2} \text{Re}(z_n) = \frac{4}{\sigma_x^2 (1 - g_0)} \text{Re}(z_n) \quad (8)$$

Note that the extension of this receiver to higher-order modulations only affects the complexity of the mapping

and demapping functions. On the ideal AWGN channel, the MMSE IC-LE turbo-equalizer reduces to a simple iterative demapping and decoding scheme.

3. IMPLEMENTATION ISSUES

3.1. Receiver design

Our implementation is targeted towards a 16 bits fixed-point DSP device with two-complement arithmetic. Special care should be taken to properly quantize the data in order to maintain the highest possible precision while avoiding underflows/overflows resulting from finite precision computations.

The proposed implementation relies on two hypothesis : the average power of the received samples is less than unity, and the receiver has knowledge of the channel taps h_k and parameters σ_x^2 and σ_w^2 . The first condition may be realized in practice by means of a convenient automatic gain control device inserted in front of the ADC. The second assumption relates to the insertion of a proper channel parameters estimator at the turbo-equalizer front-end and will not be addressed here. The observations y_n and channel taps h_k are quantized on 16 bits following the common DSP Q15 representation. The receiver is designed to operate with SNR values ranging from 0 up to 20 dB.

Regarding the realization of the SoMAP module, soft estimates a_n are computed according to (2), without the scaling factor σ_x which is applied after the computation of ρ . The $\tanh(\lambda/2)$ function is precomputed and stored in a look-up table. Quantization range is limited to $\lambda \in [-8, +8]$ with a quantization step of $1/64$, thus resulting in 1024 entries. This value has been chosen to match the range of the input soft values delivered by the decoder (see below). The normalized variance ρ is computed using the sample variance estimator and assuming $E(a_n) = 0$, yielding :

$$\rho \approx \frac{1}{N_s} \sum_{n=0}^{N_s-1} |a_n|^2 \quad (9)$$

where N_s refers to the number of symbols in a burst.

The equalizer coefficients are computed once a burst and then applied to the whole received frame. The optimum filters under finite-length constraints may be derived from matrix algebra in a similar way as in [6] and [8]. We rather focused on a less complex but sub-optimal alternative relying on the Fast Fourier Transform (FFT). Simulations did not show significant performance loss when using this solution with respect to exact computations. The resulting procedure is summarized in table 1. Parameter N_p denotes the number of taps of the feedforward filter $P(\omega)$. Note that the feedback filter $Q(\omega)$ has length $N_q = N_p + L - 1$. Filtering in (3) is realized in the time-domain.

The SoDEM function consists in a direct implementation of equation (8). The output soft values $L_e^E(c_n)$

-
1. Compute the FFT H_n of h_n on N_p points
 2. Compute $D_n = (1 - \rho)|H_n|^2 + 1/\text{SNR}$ and $P'_n = H_n^*/D_n$ for $n = 0..N_p - 1$
 3. Compute $\beta = \frac{1}{N_p} \sum_{n=0}^{N_p-1} H_n P'_n$ and $g_0 = \beta/(1 + \beta\rho)$
 4. Compute $P_n = P'_n/(1 + \beta\rho)$ and take the IFFT of P_n on N_p points to get p_n
 5. Compute q_n as the convolution of p_n with h_n and set $q_0 = 0$
-

Table 1: Coefficients computation procedure

are quantized on 10 bits. The interleaving permutation is stored in RAM and used both by the interleaving and deinterleaving functions.

The SISO decoder implements the Max-Log-Map algorithm. One-shot decoding is performed on the whole coded sequence, thus maximizing the computation efficiency at the expense of higher storage requirements with respect to a sliding-window implementation. Decoding proceeds in 3 steps. The backward recursion is performed first, and the resulting backward state metrics are stored in an array. The decoder then simultaneously performs the forward recursion and delivers *a posteriori* soft values $L^D(c_n)$ on the code bits, quantized on 10 bits. In the final step, both extrinsic information on coded bits (also quantized on 10 bits) and hard decisions on information bits are extracted from the $L^D(c_n)$ quantities, thanks to the systematic property of the code. No additional storage is required for the transitions metrics which are recomputed when needed. State metrics accumulation remains the critical issue in the decoder implementation as it may overflow. We retained the solution advocated in [9] which is particularly suited for software implementation. The metric growth problem is solved by subtracting the metric of the zero state to the other state metrics at each stage in the trellis. This strategy is applied both for the forward and backward recursions. Note that this solution reduces the storage requirements since metrics for the zero state are now identically 0 and need not be stored anymore.

3.2. Complexity and storage

Preliminary estimations show that the overall complexity of the receiver is essentially dominated by the filtering and decoding operations with respect to the coefficients computation procedure. The storage requirements are fully compatible with the average on-chip RAM size available on current DSP.

4. SYSTEM PERFORMANCE

Simulations have been conducted over the time invariant ‘‘Porat’’ channel model, with impulse response $h = \{2 - 0.4j, 1.5 + 1.8j, 1, 1.2 - 1.3j, 0.8 + 1.6j\}$ [4] in

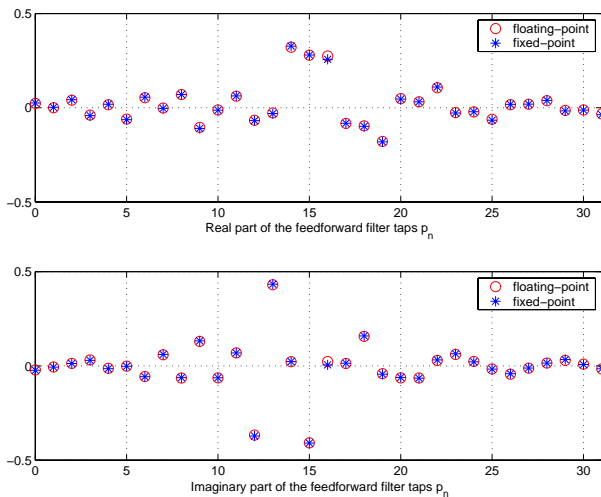


Figure 3: Feedforward filter coefficients for SNR = 5 dB and $\rho = 0$ on the Porat channel model

order to assess the performance of the proposed implementation. Bursts of $N_s = 1024$ symbols were considered, with $N_p = 32$ taps for the feedforward filter. Figure 3 compares the coefficients p_n computed both with our fixed-point implementation and with the ideal unquantized receiver, for parameters SNR = 5 dB and $\rho = 0$. We notice the good accuracy of the fixed-point computation procedure within the 16 bits data representation constraint. BER simulation results are presented in figure 4 respectively at the first and fifth iteration. The fixed-point implementation only suffers a 0.2 dB loss with respect to the floating-point turbo-equalizer at iteration 5 on this channel model. Additional simulations have shown that the degradation is less than 0.5 dB on a wide range of channels. Interestingly, the performance gap is all the more smaller that the channel is harder to equalize. Note that better overall system performance may be achieved with larger interleaver sizes in combination with stronger coding schemes (e.g. turbo-codes), and by considering (sometimes) more iterations.

5. CONCLUSIONS

The fixed-point realization of a low complexity and efficient turbo-equalization scheme was exposed. Simulation results show that the proposed implementation performs at worst within 0.5 dB from the ideal unquantized receiver. A DSP implementation on TI TMS320C5509 device, as well as the extension to QPSK and 16-QAM modulations are currently under development. Investigation of the receiver performance over block-fading channels is also planned.

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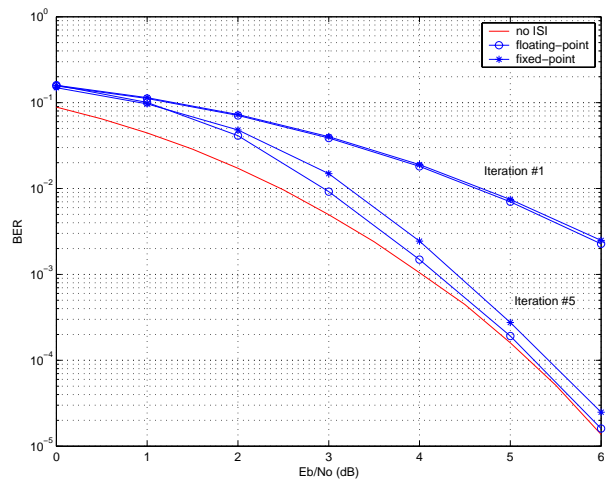


Figure 4: BER simulation results with 5 iterations on the Porat channel model

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