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Multi-scale analysis of the mobility in high-k UTBB-FDSOI Devices and comparison to split-CV measurements.

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Abstract—A rigorous study of the mobility in high-k metal gate Ultra-Thin Body and Box Fully Depleted SOI (UTBB-FDSOI) devices is done by means of split C-V measurements and advanced simulations. Measurements have been performed for various Interfacial Layer (IL) Equivalent Oxide Thickness (EOT) allowing an investigation of the physical mechanisms responsible for the mobility degradation at high-k/IL interface. The impact of the back bias on transport properties is investigated and mobility enhancement in the forward regime (back gate inversion) is demonstrated. A multi-scale simulation approach is performed and we compared simulated mobility using quantum Non-Equilibrium Green's Functions (NEGF) to semi-classical solvers results using the Kubo Greenwood (KG) approach. We demonstrated good correlations between these solvers comparing phonon and remote Coulomb-limited mobility. However, a clear overestimation of the surface roughness-limited mobility determined using semi-classical solvers is shown compared to NEGF results. These advanced solvers have been used to reproduce mobility measurements allowing us to calibrate Technology computer aided design (TCAD) mobility models.

Keywords: *UTBB-FDSOI devices, split C-V mobility measurements, back bias, NEGF, semi-classical solvers, TCAD.*

I. INTRODUCTION

UTBB-FDSOI is considered as one of the best solution to overcome conventional planar Bulk CMOS limitations [1-3]. Thanks to an excellent electrostatic control and transport properties, this architecture is suitable to reach ITRS requirements for 28 nm technology node and beyond [4]. The threshold voltage can be easily adjusted by applying back biases (VB) and it has recently been demonstrated that the mobility can be enhanced in the forward regime (VB > 0 V for nMOS and VB < 0 V for pMOS) [5]. However, the presence of high-k dielectrics can induce mobility degradations when the Interfacial

Layer (IL) Equivalent Oxide Thickness (EOT) is decreased [6-8].

The modeling of the transport in this technology is essential to predict device performances and to identify mechanisms responsible for the mobility degradation. Many solvers have been developed to investigate the transport in UTBB-FDSOI devices but their direct comparison remains difficult because of the use of different models parameters or structures. In this paper, an investigation of the mobility in high-k UTBB-FDSOI is performed thanks to “multi-scale” simulations: quantum Non-Equilibrium Green's Functions (NEGF) solvers, semi-classical solvers and calibrated empirical TCAD mobility models are compared to split-CV measurements.

In the first part of the paper we briefly described solvers, mobility models and parameters used for the simulations. In the second part, we investigate the effect of the back bias on the electrostatic behaviors and on the transport properties, thanks to effective mobility measurements (split-CV method). These measurements have been performed for n- and p-MOS high-k UTBB-FDSOI devices with various EOT ranging from 1 to 3.7 nm in order to study the effect of the gate oxide scaling. The third part is a comparison of the mobility simulated using widely used semi-classical approaches such as the Kubo-Greenwood (KG) to NEGF results. Three main scattering mechanisms responsible for the mobility degradation in high-k UTBB-FDSOI device have been investigated: 1/Phonon, 2/ surface roughness (SR) and 3/ remote coulomb scattering (RCS). Finally, a full set of parameters is determined for TCAD mobility models to reproduce mobility measurements.

II. MULTI-SCALE SIMULATION APPROACH: NEGF, SEMI-CLASSICAL AND TCAD SOLVERS.

A. Semi-classical approach

The software UTOX, developed at STMicroelectronics [9], and Sentaurus Band Structure (SBAND) [10] from Synopsys are both self-consistent Poisson k.p Schrödinger solvers. They compute the mobility in a 2D electron/hole gas within the momentum relaxation time (MRT) approximation, using the Kubo-Greenwood formalism. The Multi-subband Monte Carlo (MSMC) solver of the University of Udine [11] give similar results as KG and is not shown here [12]. These solvers treat acoustic phonons as an isotropic, elastic mechanism and inter-valley phonons as isotropic with fixed phonon energies. Surface roughness is treated as elastic, anisotropic mechanism within the Prange-Nee approximation [13], the generalized Prange-Nee model [14], or the Gamiz numerical approach [15]. Coulomb scattering is treated as an intra-valley, elastic scattering mechanism. The matrix elements are screened using the scalar Lindhard approach.

B. NEGF

NEGF mobility calculations have been performed with the TB_SIM solver from CEA [16]. We generated random samples of disorder with width $W = 20$ nm and length $L = 30$ nm. We then built devices made of these units repeated once, twice ($L = 60$ nm), and up to three times ($L = 90$ nm). One nanometer of SiO₂ is included in the effective mass Hamiltonians on both sides of the film. We next computed the resistance of the devices in a mode space approach, including electron-phonon scattering. As expected, the resistance of the devices is proportional to their length, allowing for an accurate extraction of the resistance of the disordered sample. We finally computed the phonon-limited mobility μ_{PH} in smooth films and extracted an "effective" mobility $\mu_{SR}^{-1} = \mu_{SR+PH}^{-1} - \mu_{PH}^{-1}$ (surface roughness) or $\mu_{RCS}^{-1} = \mu_{RCS+PH}^{-1} - \mu_{PH}^{-1}$ (remote Coulomb scattering). We stress that a direct NEGF calculation (no phonons) for SR or RCS might not give a very accurate picture, as the absence of inelastic pathways for electron scattering strengthens localization.

C. TCAD

Mobility in TCAD is determined using empirical models which depend on a series of parameters that have to be calibrated on measurements or on more advanced solvers (NEGF, MSMC, KG). Mobility simulations have been performed using Sdevice solver from SYNOPSIS [10].

Bulk phonon-limited mobility is treated using:

$$\mu = \mu_0 \left(\frac{T}{300K} \right)^{-\theta} \quad \text{Eq.1}$$

with μ_0 the mobility at 300 K, T the temperature and θ a fitting parameter.

The remote Coulomb-limited mobility is given by:

$$\mu_c = \frac{\mu_0 \left(\frac{T}{300K} \right)^k \left\{ 1 + \left[\frac{c}{c_{trans} \left(\frac{N_{A,D}}{10^{18} \text{cm}^{-3}} \right)^{\gamma_1} \left(\frac{N_c}{N_0} \right)^{\gamma_2}} \right]^{\nu} \right\}}{\left(\frac{N_{A,D}}{10^{18} \text{cm}^{-3}} \right)^{\gamma_2} \left(\frac{N_c}{N_0} \right)^{\gamma_2} \cdot D \cdot f(F_{\perp})} \quad \text{Eq.2}$$

$$D = \exp\left(-\frac{x}{l_{crit}}\right)$$

With

$f(F_{\perp}) = 1 - \exp[-(F_{\perp}/E_{10})^{\gamma}]$. x is the distance from interface, N_c is the negative or positive interface charge density, $N_{A,D}$ is the charge density for the Coulomb 2D component and c is the carrier concentration in the channel. F_{\perp} is the perpendicular electric field and the other terms are fitting parameters.

ThinLayer mobility model is used to take accounts for the mobility degradation in thin channel. The calibration has previously been done in [10,17,18] and is used for our study. The only modified term is the one accounting for surface roughness to fit experimental data:

$$\mu_{SR} = \left(\frac{\left(\frac{F_{\perp}}{F_{ref}} \right)^{A^*}}{\delta} + \frac{F_{\perp}^3}{\eta} \right)^{-1} \quad \text{Eq.3}$$

With F_{ref} a reference field equal to 1MV/cm. δ , η and A^* are fitting parameters. The distance from the considered interface is directly introduced in the Matthiessen rule through the factor D (see D in eq. 2):

$$\frac{1}{\mu_{tot}} = \frac{D}{\mu_{SR}} + \dots \quad \text{Eq.4}$$

Previously, it has been observed in [19] that the surface roughness can be degraded by high-k oxides and it was expected that rugosity parameters had to be modified.

III. EXPERIMENTAL OBSERVATIONS AND ELECTROSTATIC CALIBRATION

Devices were processed on 300 mm SOI wafers with a 25 nm thick BOX. The oxide stack is made of a 1.8 nm thick layer of high-k oxide (HfSiON) deposited on top of a SiON IL with various EOT. The final channel

thickness is 7.5 nm and the effective mobility was extracted using split-CV method on $10 \times 10 \mu\text{m}^2$ devices

A. Impact of the Back bias

The impact of VB on the gate capacitance is shown on figure 1 for n- and p-MOS. The dependence on the back bias is strong and, as previously demonstrated in [20], in the forward regime ($V_B > 0$ V for nMOS and $V_B < 0$ V for pMOS) the capacitance reaches a first level with an amplitude of $C_{inv} // C_{Si}$. The inversion charge thickness (T_{inv}) of the front gate capacitance is 2.65 nm which is consistent with an EOT of 2.35 nm. Consequently, the extracted electrical Silicon thickness (following formula in figure 1) is consistent with ellipsometric measurements ($T_{Si} = 7.5$ nm).

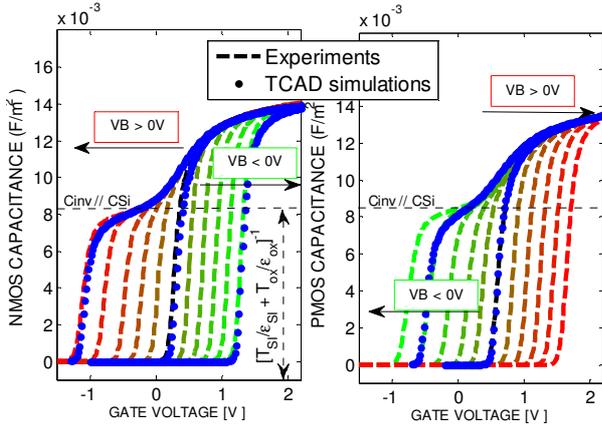


Figure 1: Gate capacitance as a function of the Gate voltage for various back biases (V_B) ranging from -10V to 10V per steps of 2V in nMOS devices (fig 2a) and pMOS devices (fig 2b). $T_{inv} = 2.65$ nm; $T_{Si} = 7.5$ nm; $T = 300$ K.

The threshold voltage can be significantly shifted by -1.5 V to 1 V for V_B ranging from -10 V to 10 V (figure 2) while the sub-threshold slope remains unchanged for both n- and p-MOS: see drain current characteristics on figure 3.

An electrostatic calibration has been performed for all simulations shown in this paper (NEGF, KG and TCAD). $V_T(V_B)$ and the variation of the capacitance with V_B is shown for TCAD (figures 1 and 2) and all solvers present very good agreements using identical geometrical parameters: $T_{inv} = 2.65$ nm, $T_{Si} = 7.5$ nm and $T_{BOX} = 25$ nm.

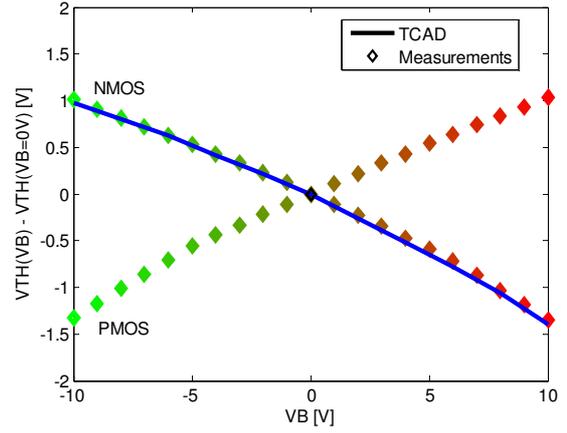


Figure 2: Threshold voltage variation (reference at $V_B = 0$ V) as a function of the back bias in nMOS devices (fig 3a) and pMOS devices (fig 3b). $T_{inv} = 2.65$ nm; $T_{Si} = 7.5$ nm; $T = 300$ K.

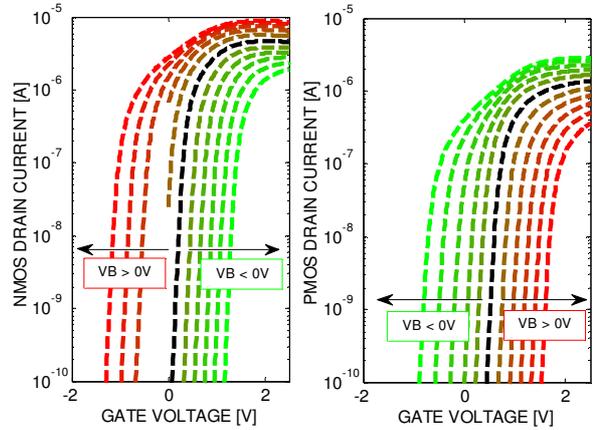


Figure 3: Drain current as a function of the Gate voltage for various back biases (V_B) ranging from -10V to 10V per steps of 2V in nMOS devices (fig 4a) and pMOS devices (fig 4b). $T_{inv} = 2.65$ nm; $T_{Si} = 7.5$ nm; $T = 300$ K.

Figure 4 represents the profile of the potential and the electron density in the channel simulated using KG solvers. It is demonstrated that the inversion charges is moved from the front to the back interface by applying a back bias. The “volume” inversion regime is however not completely reached as the majority of carriers are confined at front and back interfaces. At the same time, the silicon channel is too thick ($T_{Si} = 7$ nm) to reach this regime [21].

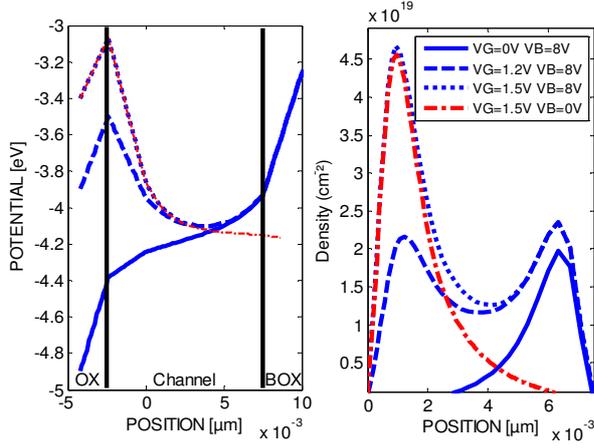


Figure 4: Simulated profile of the potential and the electron density in the channel for various biases conditions. nMOS, $T_{inv}=2.65$ nm; $T_{si}=7.5$ nm; $T=300$ K.

Figure 5 shows the dependence of the mobility on inversion charge for various back biases for n- and p-MOS. For a given field, an increase of the mobility is observed for $VB>0$ V in nMOS and for $VB<0$ V in pMOS devices. This improvement of mobility is discussed in details later.

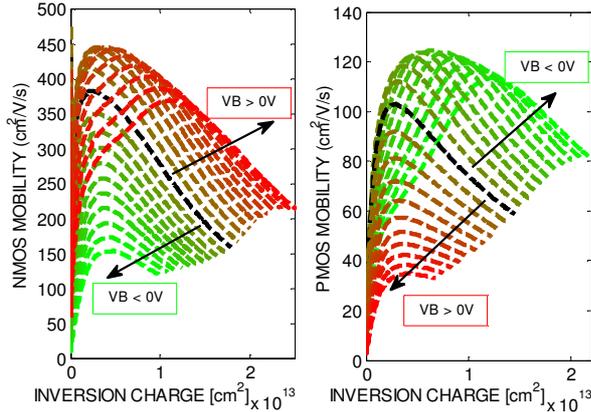


Figure 5: Effective experimental mobility as a function of the inversion charge for various back biases (VB) ranging from -10 V to 10 V in nMOS devices (fig 5a) and pMOS devices (fig 5b). $T_{inv}=2.65$ nm; $T_{si}=7.5$ nm; $T=300$ K.

B. Discussions about the definition of the effective field and the universality of the mobility

Many issues have been reported concerning the universal behavior of the mobility [22] and the definition of the effective field in FDSOI devices [23].

The theoretical effective field expression can be defined as:

$$E_{eff}^{th} = \frac{\int_0^{T_{si}} E_z(x) n(x) dx}{\int_0^{T_{si}} n(x) dx} \quad Eq.5$$

With $E_z(x)$ the transversal electric field and $n(x)$ the carrier density which depend on the position in the SOI. This definition works well for Bulk devices but it has recently been mentioned [22] that it cannot be applied for double gate device since its value is always equal to 0. We still used it for UTBB-FDSOI device simulation since the electrodes and consequently the carrier distributions are dissymmetric.

The experimental effective field was calculated using:

$$E_{eff}^{exp} = \frac{Q_d + \eta Q_i}{\epsilon_{si}} - \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{VB}{T_{BOX}^{eff}} \quad Eq.6$$

With $T_{BOX}^{eff} = \frac{C_{si} + C_{BOX}}{C_{si}} T_{BOX}$, Q_i the inversion charge and Q_d the depletion charge ($Q_d = q N_A T_{si}$). Values for η parameters have historically been fixed to 0.5 for nMOS and 0.33 for pMOS to make the mobility variation with respect to the effective field “universal” [24]. However, from the electrostatic standpoint, it is demonstrated that η should be equal to 0.5 for both devices [25]. Moreover, we demonstrated in this paper that the mobility is not universal since it depends both on the inversion charge and the effective field: for a given effective field, many values of mobility can be obtained depending on the position of the carriers and consequently on front and back gate voltages.

In figure 6, we compared the experimental effective field (extracted from Eq.6) to the theoretical one (Eq.5) obtained by simulation for n- (fig. 6a) and p-MOS (fig. 6b) devices. Really good agreements are observed for both devices when using $\eta = 0.5$.

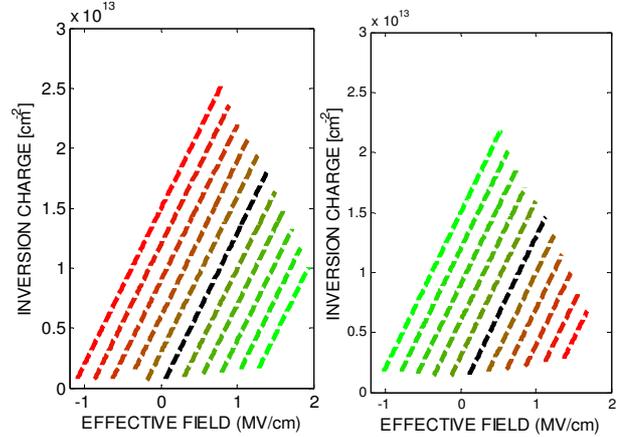


Figure 6: n- and p-MOS experimental effective field (Eq.6) assuming $\eta = 0.5$ compared to the simulated field (Eq.5). VB from -10 V to 10 V per steps of 2 V.

The mobility with respect to the effective field and for various VB is then plotted for n- and p-MOS using $\eta = 0.5$ (figure 7).

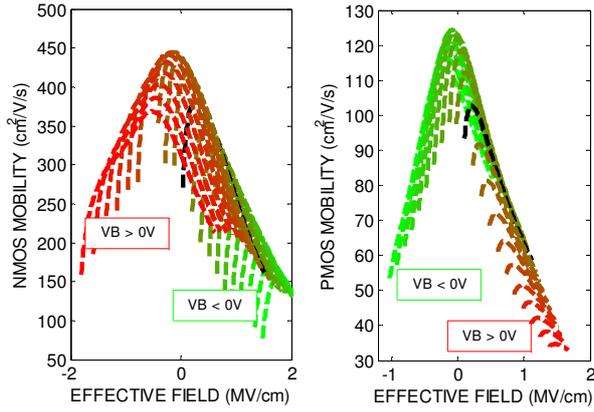


Figure 7: Effective experimental mobility as a function of the effective field for various back biases (VB) ranging from -10V to 10V in nMOS devices (fig 8a) and pMOS devices (fig 8b). $T_{inv}=2.65$ nm; $T_{si}=7.5$ nm; $T=300$ K.

Applying back biases in UTBB-FDSOI device allows to “explore” a larger range of effective field (from -2 to 2 MV/cm). The mobility exhibits a bell-shaped behavior and is limited, at large negative and positive effective field, by surface roughness scattering with the back and the front interface respectively. In figure 8, the mobility is extracted at fixed inversion charge and as a function of VB. An enhancement of the mobility of nearly 45% for nMOS and 60% for PMOS can be observed at $N_{inv}=1e13$ cm⁻². The mobility enhancement can be explained by the shift of the inversion charge centroid away from the interface (the profile of carrier density is shown in figure 8 for three different biases conditions) affecting surface-roughness and remote-Coulomb scattering mechanisms. Moreover, the back interface (Silicon/BOX) seems to be intrinsically smoother than the front interface (Silicon channel/IL) since the mobility is less degraded at high absolute effective field (figure 7). This has been confirmed by NEGF simulations (not shown here) where different rugosity parameters for the front and the back interface have been used to reproduce experiments.

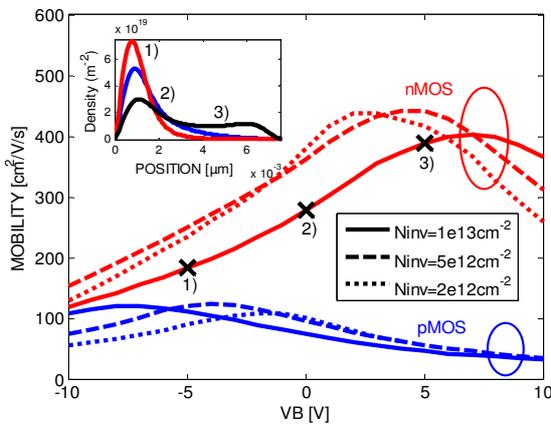


Figure 8: Effective experimental mobility as a function of the back bias for various inversion densities: $N_{inv}=1e13$, $5e12$ and $2e12$ cm⁻². $T_{inv}=2.65$ nm; $T_{si}=7.5$ nm; $T=300$ K. Symbols represent biases conditions where density profiles are extracted (for $N_{inv}=1e13$ cm⁻²): 1/ $VB=-5$ V, $VG=2.0$ V; 2) $VB=0$ V, $VG=1.6$ V; 3) $VB=5$ V, $VG=1.2$ V;

Figure 9 represents the mobility variation versus the effective field sweeping VG at $VB=0$ V and sweeping VB at VG ranging from 1.0 to 2.5V. It demonstrates that the mobility depends on back bias conditions for a given effective field and tends to confirm that the mobility does not follow a unique universal trend. It is also observable in figure 10 where the mobility with respect to the inversion charge is extracted at $E_{eff}=0.35$ MV/cm by adjusting front and back gate voltages. For a given effective field, many values of mobilities can be obtained depending on bias conditions.

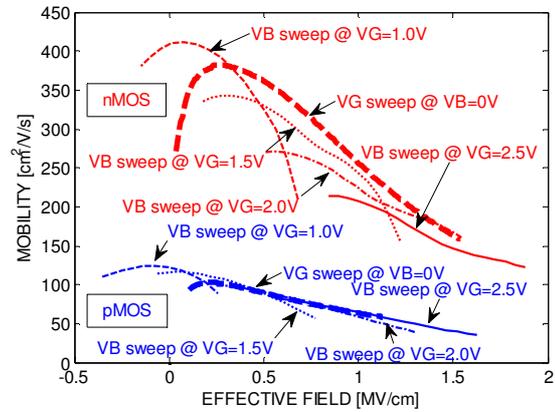


Figure 9: n- and p-MOS experimental effective mobility as a function of the effective field sweeping the back bias for three VG values: 1.5V, 2.0V and 2.5V. Measurements at $VB=0$ V with a VG sweep is also added. $T_{inv}=2.65$ nm; $T_{si}=7.5$ nm; $T=300$ K.

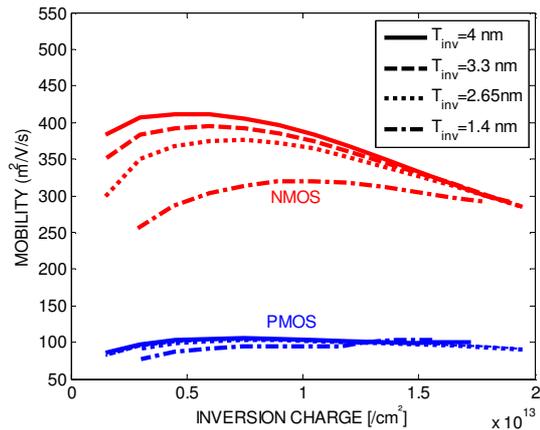


Figure 10: n- and p-MOS experimental effective mobility as a function of the inversion charge and extracted at $E_{eff}=0.35$ MV/cm by sweeping front and back gate voltages.

C. Influence of the IL EOT

The mobility variation with the effective field for two structures with two different IL EOT is shown on figure 11. A significant degradation of the mobility can be observed compared to Takagi measurements and can be attributed to the presence of the high-k oxide. The degradation of the mobility in presence of high-k oxide has been observed and studied by many authors. This degradation is attributed to scattering mechanisms such as remote Coulomb [6,7,26,27], remote phonon [28] or remote surface roughness scattering [29].

In figure 12, we extended our study to T_{inv} varying from 1.4 to 4.0nm (variation of the IL EOT) and for n- and p-MOS. The IL EOT scaling induces strong mobility degradations. Two tendencies for the degradation can be observed (figure 13). The first one, for IL EOT > 1 nm, the mobility degradation can be well captured by simulations (figure 21) and is attributed to remote Coulomb scattering. The second one, for IL EOT < 1 nm, the degradation is attributed to another scattering mechanism. Remote phonon and high-k/SiO₂ interface roughness can be suspected to be responsible for the mobility degradation. In this paper simulations targeted to reproduce devices with IL EOT > 1nm and remote phonon or remote surface roughness will not be investigated.

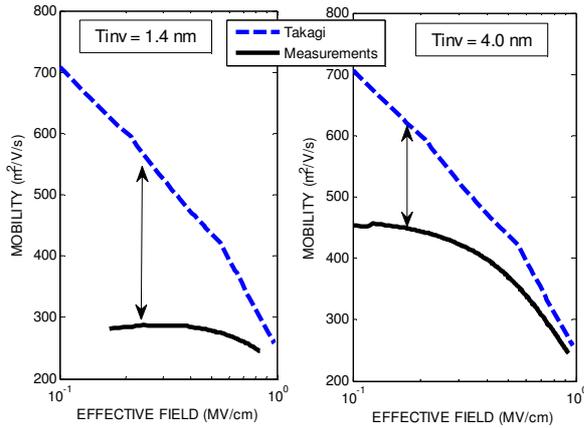


Figure 11: n-MOS Measured effective mobility as a function of the effective field for two structures with different IL EOT: a) $T_{inv}=1.4$ nm b) $T_{inv}=4$ nm. Dashed lines are Takagi measurements.

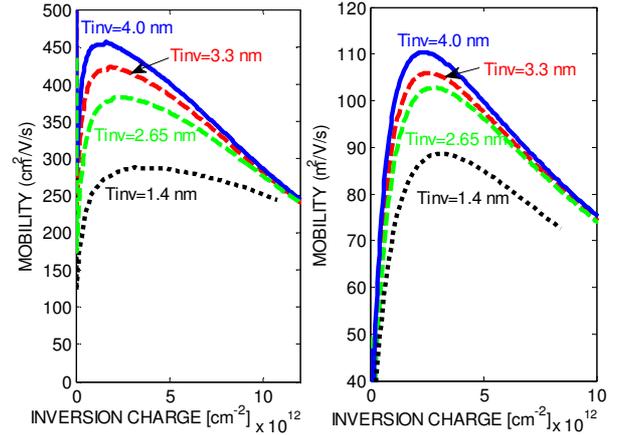


Figure 12: n- and p-MOS measured effective mobility as a function of the inversion charge for structures with various IL EOT: T_{inv} ranging from 1.4 to 4.0 nm.

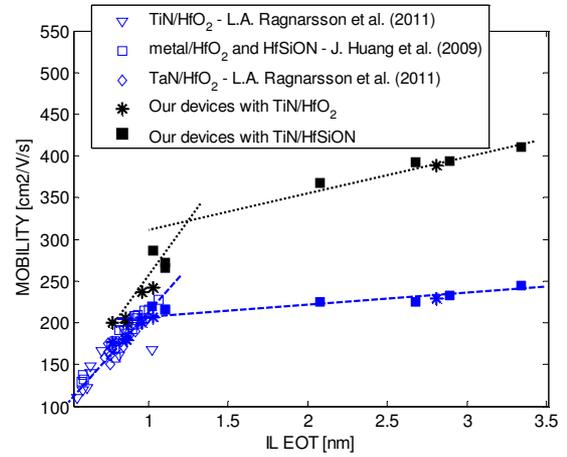


Figure 13: Effective mobility as a function of the IL EOT measured in UTBB-devices and published data compiled in [1].

IV. SOLVER COMPARISON

A. Mobility extraction: Discussion about the Matthiessen rule.

In Monte Carlo and NEGF simulations, the surface roughness or remote Coulomb-limited mobility cannot be extracted directly by turning off the phonon scattering mechanisms. An “effective” mobility μ_M , based on the Matthiessen rule is defined and used for the comparison between the different solvers:

$$\mu_M^{-1} = \mu_{A+PH}^{-1} + \mu_{PH}^{-1} \quad \text{Eq.5}$$

A is the considered scattering mechanism: Surface Roughness Scattering or Remote Coulomb scattering in this paper.

The validity of the Matthiessen rule has been recently questioned and quantitative errors have been evaluated using the following expression [30,31]:

$$E = \frac{\mu_M - \mu_A}{\mu_A} \quad \text{Eq.6}$$

With μ_A the mobility for mechanism A directly calculated using KG simulations.

An error ranging from -20 to -12% is observed (figure 14) when extracting the surface roughness-limited mobility using the Matthiessen rule. This is consistent with simulations in [30]. Concerning Remote Coulomb scattering, the error can reach -80% so it is therefore important, for the solvers comparison, to use the same method to extract the mobility.

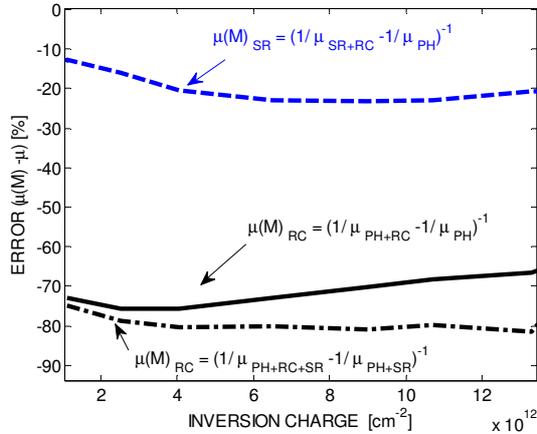


Figure 14: Error E produced by the extraction of mobility components (Surface roughness and remote Coulomb scattering) using the Matthiessen rule.

B. Results

Advanced solvers comparison has been done for electrons using a purely parabolic band structure with a Si/SiO₂ barrier of 3.15 eV and an oxide effective mass of 0.5m₀. The gate stack of the device is made of 2 nm of HfO₂ ($\epsilon = 22$) on top of 2 nm of SiO₂ ($\epsilon = 3.9$). The silicon channel thickness varies from 2 nm to 10 nm and the BOX thickness is 25 nm.

Parameters of [32] have been used for phonon scattering. The phonon-limited mobility with respect to the channel thickness is shown in figure 15 and all solvers are in excellent agreement.

The comparison for the surface roughness scattering use an exponential autocorrelation with $\Delta=0.47$ nm and $\Lambda=1.3$ nm. Figure 15 shows the good agreement between surface roughness-limited mobilities obtained with semi-classical methods (KG) but they clearly overestimate the mobility simulated using TB_SIM. This is further pointed out in figure 16, which shows the SR-mobility as a function of the channel thickness T_{Si} .

The discrepancy between semi-classical methods and NEGF is more important at low T_{Si} (below 5 nm). The validation on experimental data will be done by using higher surface roughness parameters (Δ and Λ) for KG solvers than for NEGF.

Figure 18 shows that the surface roughness limited-mobility calculated using Gamiz approach and results obtained using the usual Prange-Nee-based approach are in good agreement. Jin's results [14], accounting for carrier density fluctuations and image charge effects are also added on figure 17. The introduction of these terms and the comparison to NEGF simulations need to be investigated.

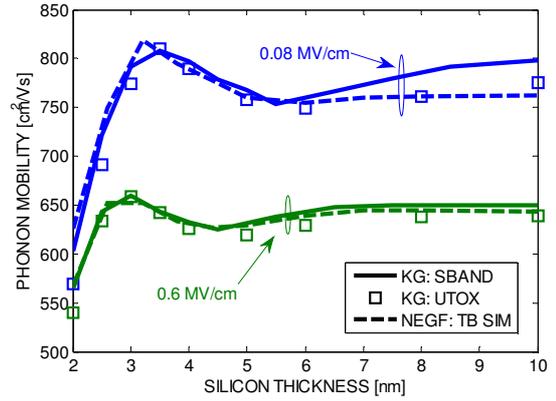


Figure 15: Phonon-limited electron mobility in FDSOI devices as a function of the silicon channel thickness. Phonon parameters from [] are used.

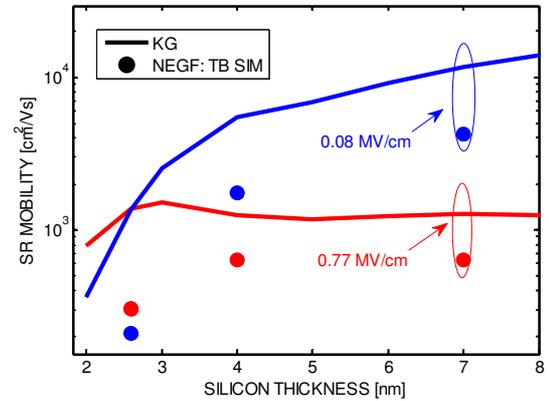


Figure 16: Effective Surface roughness-limited electron mobility in FDSOI devices as a function of the silicon channel thickness. Exponential SR autocorrelation with $\Delta=0.47$ nm and $\Lambda=1.3$ nm.

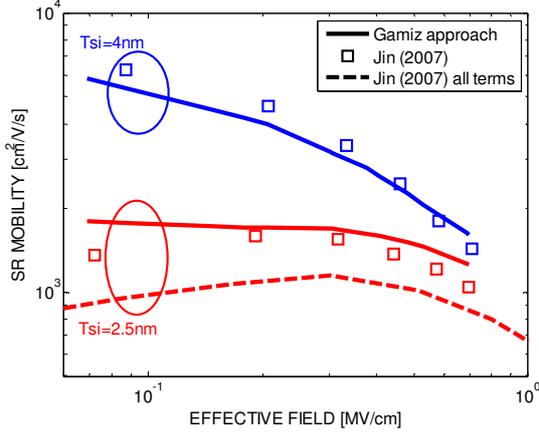


Figure 17: Surface roughness-limited electron mobility as a function of the effective field. Comparison between the Gamiz numerical approach and Jin's results accounting for carrier density fluctuations and image charge effects or neglecting them.

RC-limited mobility obtained with semi-classical methods compare well with NEGF. A low discrepancy is observed and the error is lower when the remote Coulomb scattering mechanism is dominant (with respect to phonon). This error can be due to the use of the Matthiessen rule (in the KG approach) when calculating the total momentum relaxation by adding the relaxation time of each mechanism. A.Paussa [33] demonstrated a new solution to solve the exact solution of the linearized Boltzmann transport equation (BTE).

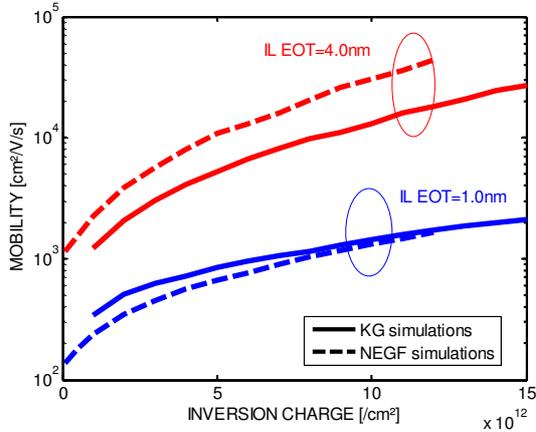


Figure 18: Effective Remote Coulomb-limited electron mobility in FDSOI devices as a function of the inversion charge and for various IL EOT.

Note also that our simulations indicate lower mobility degradations compared to simulations in [barraud casteran].

V. VALIDATION ON EXPERIMENTAL DATA

TCAD remote Coulomb-limited mobility model (Eq. 3) has first been calibrated on advanced solvers (KG).

Figure 19 shows the variation of the remote Coulomb scattering with respect to the inversion charge for various charge concentrations (figure 19a) and for various IL EOT (figure 19b). The empirical model implemented in Sdevice reproduces well the mobility determined with KG solvers. Remote Coulomb-limited mobility calibration has also been investigated and calibrated for pMOS in figure 20.

The total mobility for nMOS is then simulated using Sdevice and KG solvers varying the IL EOT (figure 21). A charge concentration of $3e13 \text{ cm}^{-2}$ at high-k/SiO₂ IL is used to fit experimental data. Excellent agreement for IL EOT > 1 nm is found between simulations and experimental data for n- and p-MOS. The mobility degradation is due to remote Coulomb scattering and is well captured by simulations.

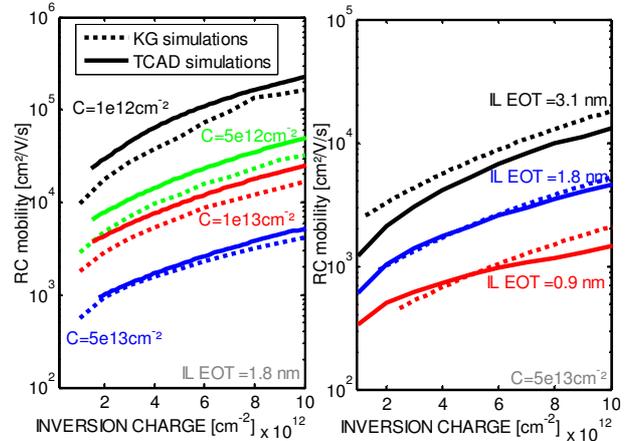


Figure 19: nMOS effective Remote Coulomb-limited electron mobility in FDSOI devices as a function of the inversion charge and for various charge concentration.

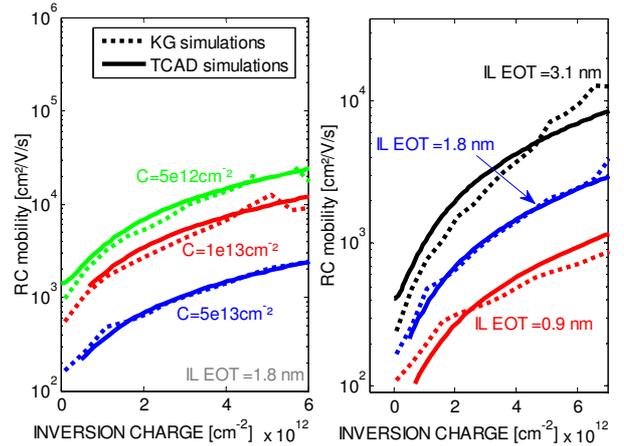


Figure 20: pMOS effective Remote Coulomb-limited electron mobility in FDSOI devices as a function of the inversion charge and for various charge concentration.

Figure 22 is the variation of the mobility with the temperature for various effective fields and for n- and p-MOS. The mobility degradation (due to the increase of phonon scattering) with increasing temperature is well reproduced by simulations.

Figure 23 is a comparison of the simulated mobility as a function of the inversion density varying T_{inv} (figure 23a) and the temperature for nMOS (figure 23b). The fit has also been done for pMOS in figure 24. Excellent agreements between simulations and experiments are found. Tables 1 and 2 are the simulations parameters for KG solvers and Sdevice respectively.

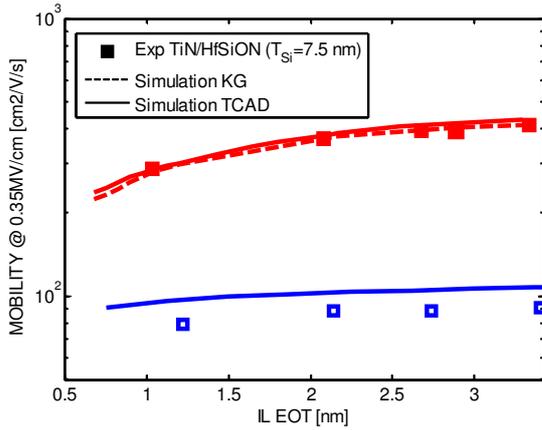


Figure 21: n- and p-MOS mobility extracted at $E_{eff}=0.35\text{MV/cm}$ as a function of the IL EOT for various temperatures: 233, 300 and 450K. Comparison between TCAD, KG solvers and experiments.

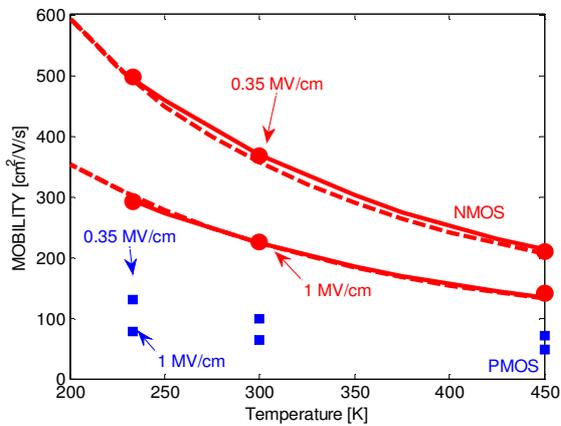


Figure 22: n- and p-MOS mobility as a function of the temperature for various effective fields: 0.35 and 1MV/cm. Comparison between TCAD, KG solvers and experiments. $T_{inv}=2.65\text{ nm}$; $T_{si}=7.5\text{ nm}$; $T=300\text{K}$.

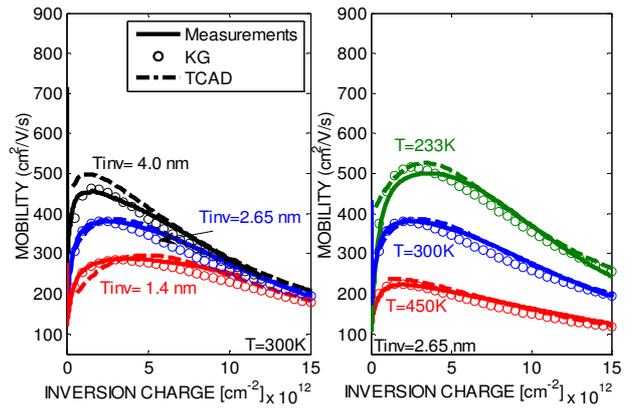


Figure 23: n-MOS mobility as a function of the inversion charge for structures with various IL EOT (fig 23a) and for various temperature (fig 23b). Comparison between Sdevice KG solvers and experiments.

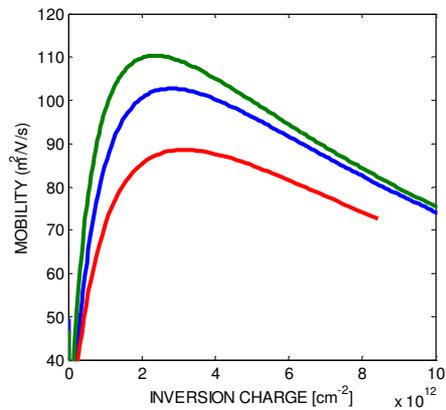


Figure 24: pMOS mobility as a function of the inversion charge for structures with various IL EOT. Comparison between Sdevice KG solvers and experiments.

	Band structure	phonon	Surface roughness	Remote Coulomb
Electron	parabolic band structure	Parameters of []	Exponential Autocorrelation $\Delta=0.62$ nm and $\Lambda=1.0$ nm. Scalar Lindhard screening.	Tensorial Lindhard screening. Charge density at high-k/IL interface: $3e13$ cm ⁻² .
Hole	six-bands k.p model	Parameters of []	Exponential Autocorrelation $\Delta=0.62$ nm and $\Lambda=1.0$ nm. Scalar Lindhard screening.	Tensorial Lindhard screening. Charge density at high-k/IL interface: $3e13$ cm ⁻² .

Table 1: Simulations parameters for KG solvers to fit experimental data

	Phonon (Eq.1)	Surface roughness (Eq.2)	Remote Coulomb (Eq.3)
Electron	Default Parameters. [10]	$A^* = 2$ $\delta = 1.6e18$ $\eta = 1e50$	$\mu_1 = 25$, $c_{trans} = 1e18$, $k = 0$, $k = 1.3$, $\eta1 = 0$, $\eta2 = 1$, $l_{crit} = 1.25e-7$, $\gamma = 0$,
Hole	Default Parameters. [10]	$A^* = 2$ $\delta = 4.10e15$ $\eta = 5.82e31$	$\mu_1 = 23$, $c_{trans} = 1e18$, $k = 0$, $k = 1.6$, $\eta1 = 0$, $\eta2 = 1$, $l_{crit} = 1.5e-7$, $\gamma = 0$,

Table 2: Simulations parameters for Sdevice to fit experimental data

VI. CONCLUSIONS

We extracted the mobility of n-type and p-type UTBB-FDSOI devices ($T_{SI}=7$ nm and $T_{BOX}=25$ nm) using split CV method. We demonstrated a significant mobility enhancement of nearly 45% for NMOS and 60% for PMOS (at $N_{inv} = 1e13$ cm⁻²) in the forward regime ($V_B > 0$ V for NMOS and $V_B < 0$ V for PMOS). The displacement of the inversion charge centroid from the front to the back interface is responsible for the reduction of surface roughness and remote Coulomb scattering mechanisms. A smoother back interface can also explain the enhancement of the mobility. We also demonstrated that the mobility does not follow a universal trend. Indeed, for a given effective field, many values of mobility can be obtained depending on bias conditions (front and back interface)

The comparison of mobilities extracted using semi-classical solvers to NEGF results showed good correlations for phonon and remote Coulomb-limited mobility. However, semi-classical solvers clearly overestimate surface roughness-limited mobility compared to NEGF.

Finally, TCAD Sdevice mobility models have been calibrated to reproduce experimental data. The Multi-scale analyses (from quantum NEGF simulations to empirical models in TCAD) reproduced well the split-CV mobility.

REFERENCES

- [1] Fenouillet-Beranger, C., et al. "Fully-depleted SOI technology using high-k and single-metal gate for 32 nm node LSTP applications featuring 0.179 μ m 2 6T-SRAM bitcell." *Electron Devices Meeting, 2007. IEDM 2007. IEEE International. IEEE*, 2007.

- [2] Fenouillet-Beranger, C., et al. "FDSOI devices with thin BOX and ground plane integration for 32nm node and below." *Solid-State Electronics* 53.7 (2009): 730-734.
- [3] Planes, N., et al. "28nm FDSOI technology platform for high-speed low-voltage digital applications." VLSI Technology (VLSIT), 2012 Symposium on. IEEE, 2012.
- [4] www.itrs.net: International Technology Roadmap for Semiconductors
- [5] Ragnarsson, L-A., et al. "On the origin of the mobility reduction in bulk-Si, UTBOX-FDSOI and SiGe devices with ultrathin-EOT dielectrics." *VLSI Technology, Systems and Applications (VLSI-TSA), 2011 International Symposium on*. IEEE, 2011.
- [6] Esseni, David, and Antonio Abramo. "Modeling of electron mobility degradation by remote Coulomb scattering in ultrathin oxide MOSFETs." *Electron Devices, IEEE Transactions on* 50.7 (2003): 1665-1674.
- [7] Ragnarsson, L. A., et al. "The impact of sub monolayers of HfO₂ on the device performance of high-k based transistors." *2003 IEEE International Electron Devices Meeting, Technical Digest*. 2003.
- [8] Cassé, Mikaël, et al. "Carrier transport in HfO₂/metal gate MOSFETs: physical insight into critical parameters." *Electron Devices, IEEE Transactions on* 53.4 (2006): 759-768.
- [9] UTOX regroups a series of k.p-Schrodinger-based tools including a KG solver. D. Garetto et al., Proc. Nanotech Conference (2010)
- [10] <http://www.synopsys.com/Tools/TCAD/>
- [11] D. Esseni, et al., « Nanoscale MOS Transistors: Semi-Classical Transport and Applications », Cambridge Univ. Press (2011).
- [12] Rideau, D., et al. "Mobility in FDSOI Devices: Monte Carlo and Kubo Greenwood Approaches Compared to NEGF Simulations."
- [13] Esseni, David. "On the modeling of surface roughness limited mobility in SOI MOSFETs and its correlation to the transistor effective field." *Electron Devices, IEEE Transactions on* 51.3 (2004): 394-401.
- [14] Jin, Seonghoon, Massimo V. Fischetti, and Ting-Wei Tang. "Modeling of surface-roughness scattering in ultrathin-body SOI MOSFETs." *Electron Devices, IEEE Transactions on* 54.9 (2007): 2191-2203.
- [15] Gamiz, F., et al. "Role of surface-roughness scattering in double gate silicon-on-insulator inversion layers." *Journal of Applied Physics* 89.3 (2001): 1764-1770.
- [16] http://inac.cea.fr/L_Sim/TB_Sim/
- [17] Silvestri, Luca, et al. "A low-field mobility model for bulk, ultrathin body SOI and double-gate n-MOSFETs with different surface and channel orientations—Part I: Fundamental principles." *Electron Devices, IEEE Transactions on* 57.7 (2010): 1567-1574.
- [18] Silvestri, Luca, et al. "A Low-Field Mobility Model for Bulk, Ultrathin Body SOI and Double-Gate n-MOSFETs With Different Surface and Channel Orientations—Part II: Ultrathin Silicon Films." *Electron Devices, IEEE Transactions on* 57.7 (2010): 1575-1582.
- [19] Cassé
- [20] Esseni, David, and Enrico Sangiorgi. "Low field electron mobility in ultra-thin SOI MOSFETs: experimental characterization and theoretical investigation." *Solid-State Electronics* 48.6 (2004): 927-936.
- [21] Ernst, Thomas, et al. "Ultimately thin double-gate SOI MOSFETs." *Electron Devices, IEEE Transactions on* 50.3 (2003): 830-838.
- [22] Cristoloveanu, Sorin, Noel Rodriguez, and Francisco Gamiz. "Why the universal mobility is not." *Electron Devices, IEEE Transactions on* 57.6 (2010): 1327-1333.
- [23] Ohata, A., et al. "Impact of back-gate biasing on effective field and mobility in ultrathin silicon-on-insulator metal-oxide-semiconductor field-effect-transistors." *Journal of Applied Physics* 113.14 (2013): 144514-144514.
- [24] Taka
- [25] Clerc, Raphael. Not published.
- [26] Barraud, Sylvain, Olivier Bonno, and Mikaël Cassé. "The influence of Coulomb centers located in HfO₂/SiO₂ gate stacks on the effective electron mobility." *Journal of Applied Physics* 104 (2008): 073725.
- [27] Casterman, D., and M. M. De Souza. "Evaluation of the Coulomb-limited mobility in high-κ dielectric metal oxide semiconductor field effect transistors." *Journal of Applied Physics* 107.6 (2010): 063706-063706.
- [28] Toniutti/rem ph
- [29] Gamiz, F., and J. B. Roldan. "Scattering of electrons in silicon inversion layers by remote surface roughness." *Journal of applied physics* 94.1 (2003): 392-399.
- [30] Esseni, David, and Francesco Driussi. "A quantitative error analysis of the mobility extraction according to the Matthiessen rule in advanced MOS transistors." *Electron Devices, IEEE Transactions on* 58.8 (2011): 2415-2422.
- [31] Chen, M-J., W-H. Lee, and Y-H. Huang. "Error-Free Matthiessen's Rule in the MOSFET Universal Mobility Region." (2013): 1-6.
- [32] Param phonon
- [33] Pausa, A., and D. Esseni. "An exact solution of the linearized Boltzmann transport equation and its application to mobility calculations in graphene bilayers." *Journal of Applied Physics* 113 (2013): 093702.