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# Redundancy Method to assess Electromigration Lifetime in power grid design

Boukary OUATTARA <sup>1,2</sup>, Lise DOYEN <sup>1</sup>, David NEY <sup>1</sup>, Habib MEHREZ <sup>2</sup>, Pirouz BAZARGAN-SABET <sup>2</sup> and Franck Lionel BANA <sup>1</sup>

<sup>1</sup>: STMicroelectronics;850, rue Jean Monnet, 38926 CROLLES Cedex France

<sup>2</sup>: Laboratory of Computer Sciences, Paris 6 (LIP6), Systems On Chips department. UPMC university  
4 place Jussieu, 75252 PARIS CEDEX 05

Phone : 0033(0)476925140 ; E-mails: boukary.ouattara@lip6.fr; lise.doyen@st.com

## Abstract

The tendency of semiconductor market to increase component density in small chip leads to reliability issues such as Electromigration (EM). This phenomenon becomes critical in deep submicron design technology. In this paper we assess chip power grid lifetimes by taking into account redundant paths contribution in case of EM degradation. The application of this method for wire lifetime validation of a 32nm microprocessor has reduced significantly wires susceptible to EM given by simulation tools.

## Introduction

Electromigration (EM) is a metallic atom movement in interconnection induced by high current density and temperatures, resulting in the creation of voids or hillocks. EM phenomenon is known since several decades, but become critical because of the increase of chips power consumption. Indeed high average currents flowing in thin interconnections make complex for designers to insure chip EM resistance. Ongoing research axes are done in order to anticipate or solve EM degradation in high density chips.

Some of contributions are mainly focused at design level on EM assessment methodology [1] and simulation tools [2]. The goal is to get accuracy in the EM degradation mechanism prediction.

In this paper we analyze the impact of EM degradation in power grid on a chip functionalities. We developed an innovative method to assess the lifetime of power grid redundant paths used to supply standard cell in case of EM failure. Finally we evaluate a chip operation lifetime with our method.

## Electromigration degradation mechanism in power grid

We identify two main interconnection networks in chip design: the power (vdd)/ground (gnd) network used for power supply and the signal network used for signal transmission. Due to currents flowing in both directions inside signal wires, the current average is null. Therefore signal network is assumed relatively safe toward EM phenomenon [4, 5].

Because of high unidirectional current (DC) densities flowing through power/ground network, they are considered highly susceptible to EM. In this work we will focus on the power/ground network.

### A. Chip power grid structure

The figure Fig.1 represents an example of chip power grid. We have M3 metal wires (vertical lines) connected to M2 (the horizontal lines) by  $V_2$  via matrix.  $V_1$  via matrix are used to connect the power grid to standard cells.

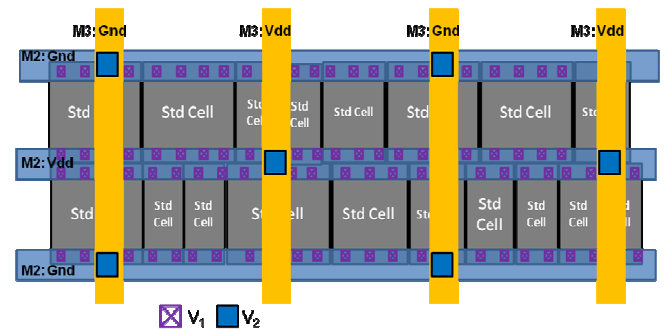


Fig. 1: Standard cells placement in chip power grid design

### B. EM-induced void locations

EM degradations are located in the wire segment around via [6]. With respect to electron ( $e^-$ ) flow direction, we expected EM void in M2 under via  $V_2$  (Fig.3a) for gnd wires and in M3 upper via  $V_2$  (Fig.3b) for vdd wires.

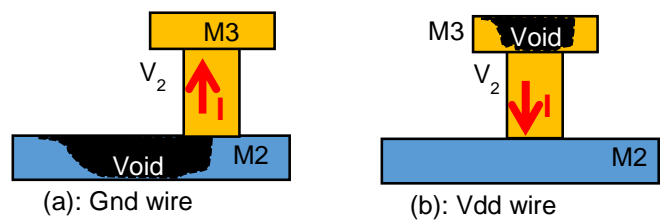


Fig. 2: Sectional overview of EM-induced voids in power grid wires.

EM void size depends on the current density flowing in considered wires for a given time.

### Interconnection lifetime assessment

Interconnect lifetime can be defined as the time to reach a void spanning over the entire wire section.

At design level, EM is assessed by comparing the local average current ( $I_{local}$ ) to a given current limit ( $I_{DRM}$ ) defined in the Design Rule Manual (DRM).  $I_{DRM}$  corresponds to a specified target in operation time to failure ( $TTF_{OP}$ ).  $I_{local}$  is evaluated in each interconnection segment for a given activities (test vectors) through a simulation [7].

#### A. Standard method

With the standard method any wire segments or vias driving more current than the limit  $I_{DRM}$  is susceptible to EM degradation (EM-susceptible). A wire TTF is evaluated with (1).

$$TTF = \frac{I_{DRM} * TTF_{OP}}{I_{local}} \quad (1)$$

Equation 1: Wire time to failure

This approach evaluates the EM lifetime of each wire or vias. However a failure in a wire will not stop supplying nearest standard cells. Indeed considering the structure of the power grid (Fig.1), once an EM failure occurs below a  $V_2$ , a second path exists to supply the devices. We want to evaluate the lifetime gain provided by this redundant path.

#### B. Redundancy method

The principle of this method is to evaluate redundant paths lifetime. The latter is a system composed by a wire and two vias as shown the figure Fig.3.

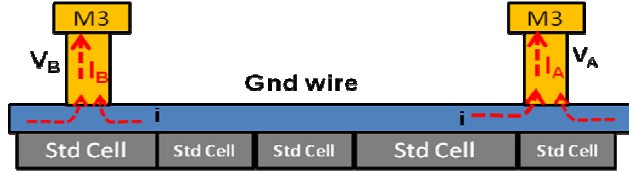


Fig. 3: Gnd wire system structure sectional view

Since EM voids appear below vias, the system lifetime will be the sum of the two via lifetimes ( $TTF_{VA}$  and  $TTF_{VB}$ ). For these calculations, we will assume that EM failure occurs once the void has reached a given critical void ( $V_C$ ) volume and that current in  $V_A$  is higher than  $V_B$ .

##### a) Time to failure of via $V_A$ ( $TTF_{VA}$ )

$V_A$  lifetime is calculated according to local current ( $I_A$ ) flowing in Via  $V_A$  with (1). At  $TTF_{VA}$ , the  $V_C$  is created by  $I_A$  below  $V_A$  as shown in Fig.4.

At the same time a non critical void ( $V_{OB}$ ) has been created by current ( $I_B$ ) near via  $V_B$ .

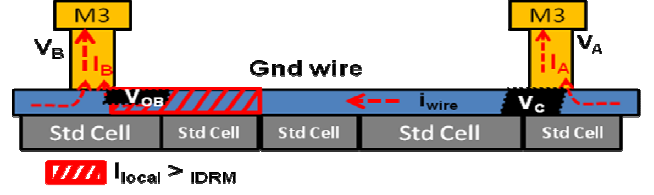


Fig. 4: Sectional view of a critical void in gnd wire after  $TTF_{VA}$

Due to a complete open in wire section near  $V_A$ , the current provided by  $V_A$  will flow through via  $V_B$ . The initial current in  $V_B$  will change from  $I_B$  to  $I_B + I_{wire}$ .

##### b) Time to failure of redundant via $V_B$ ( $TTF_{VB}$ )

Now the goal is to calculate the necessary time to create fatal void below  $V_B$ .

This lifetime is evaluated by taking into account the wear state of wire section that is the void volume  $V_{OB}$ .  $TTF_{VB}$  is expressed as function of  $I_A$ ,  $I_B$ , and  $I_{DRM}$  by (2)

$$TTF_{VB} = \left(1 - \frac{I_B}{I_A}\right) * \frac{I_{DRM} * TTF_{OP}}{I_{wire} + I_B} \quad (2)$$

Equation 2: Redundant path Time to failure

##### c) System lifetime ( $TTF_S$ )

The  $TTF_S$  is evaluated from the sum of all path lifetimes ( $TTF_{VA}$  and  $TTF_{VB}$ ) used to supply standard cells. Equation (3) is used to assess this  $TTF_S$  by summing (1) and (2).

$$TTF_S = \frac{I_{DRM} * TTF_{OP}}{I_A} + \left(1 - \frac{I_B}{I_A}\right) * \frac{I_{DRM} * TTF_{OP}}{I_{wire} + I_B} \quad (3)$$

Equation 3: sSystem lifetime assessment equation

This equation also applies for vdd net.

### Experiments and results

We assess the power grid lifetimes of a microprocessor designed in 32nm node operating at a frequency of 1 Ghz and voltage equal to 1.3V. We used an arbitrary current limit ( $I_{DRM}$ ) to guarantee a  $TTF_{OP}$  of ten years (10 years) assuming a non-stop circuit operation.

$I_{DRM}$  violations concerned M2 wire segments (vdd and gnd) supplying standard cells with high power consumption (High power cells), mainly clock tree cells with high activities (typically 200% toggle rate). For our analyses we focus on gnd network composed of about 400,000 M2 wire segments.

First analysis with standard method has computed about 1,900  $TTF_S$  under  $TTF_{OP}$  (EM-violations).

We have developed an algorithm to detect and compute redundant paths on these EM violations.

After analysis we observe that about 200 segments have no or too worn physical redundant path.

For the about 1700 remaining segments, we have applied the redundancy method.

The TTF distributions obtained with both methods (standard method and redundancy method) are plotted in figure Fig.5.

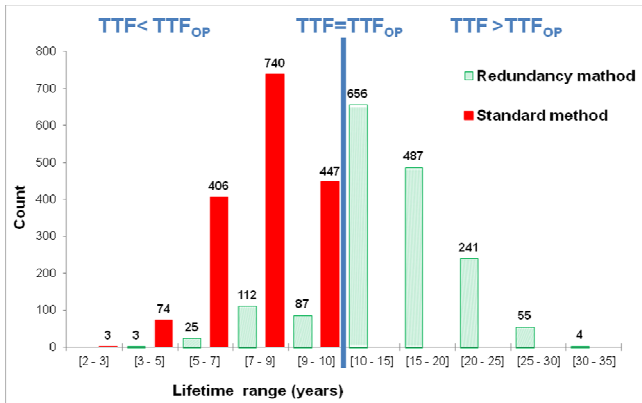


Fig. 5: Comparison of lifetime according the EM risk assessment method

We observe through these results that with the redundancy method, we reduce significantly the number of EM-violation from about 1900 to about 400. There are 200 violations with no redundant paths and 200 EM-violations where redundancy is not sufficient to reach the target of 10 years lifetime.

### Discussions

In order to fix the remaining EM violations, we can either improve chip design or relax current limits.

First physical redundant paths must be insured by optimizing placement to avoid such high power cells at the power grid border.

Second, we need to make sure that the redundant path actually provides a lifetime gain. In other words, via  $V_B$  (Fig.3) should not initially drive too much current. This can be achieved by optimizing high power cells placement with respect to power grid pitch. This is a reasonable action for designer since a dedicated placement is done for clock tree cells, the main contributors of high power cells.

The alternative or complementary solution is to relax the current limits  $I_{DRM}$ .

First the definition of  $TTF_{OP}$  must be in accordance with the chip mission profiles. Let's assume a product switched-off half the time. To guarantee 10 years of operation, we can tolerate twice more current.

Second it is well known that increasing via number matrix improves EM lifetime. By optimizing via connection between M3 and M2 we can allow higher current in interconnection.

We can use this to improve chip power grid robustness towards EM degradation.

### Conclusion

The redundant paths given by power grid structures ensure the chip operation in case of EM degraded interconnections. In this paper we have evaluated the lifetime of these redundant paths according to their wear states. We take into account these additional lifetimes in chip operating time prediction. The results obtained on a 32nm microprocessor design with our redundancy method have shown a significant reduction of the EM-susceptible interconnections. In addition we have proposed design and process solutions to further reduce EM violations and increase chip robustness.

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