Radio-frequency and low noise characteristics of SOI technology on plastic for flexible electronics

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A B S T R A C T

In this work, we report on the HF performance and noise characteristics of 65 nm SOI-CMOS technology transferred onto plastic films. After transfer-bonding onto a thin flexible substrate, RF-SOI-MOSFETs are shown to feature high unity-current-gain cutoff and maximum oscillation frequencies f_T/f_{MAX} amounting to 150/160 GHz for n-type and 100/130 GHz for p-type, respectively. Minimal noise figure and associated gain NF_{min}/G_{ass} of 0.57 dB/17.8 dB and 0.57 dB/17.0 dB are measured at 10 GHz for n- and p-MOSFETs, respectively.

1. Introduction

High frequency transistors from mature 65 nm SOI-CMOS technology node are recognized for delivering a performance level suitable for high frequency, low noise, and low power applications [1]. In parallel to the development of rigid conventional technologies on thick silicon wafer handler (>800 μm), a growing interest is being devoted to the field of large area and bendable electronics also referred to as "macro-electronics" [2]. Adding mechanical bendability to electronic circuits and systems is currently opening the way to promising applications in domains as diverse as biomedical, wireless sensors networks (WSNs), or structure health monitoring. A large number of these prospective applications require, in addition to bendability, low power consumption, radio-frequency communication, and low noise signal processing for instance. CMOS technologies in ultra-thin regime have been reported to provide technological solutions for these applications [3] as they combine mechanical flexibility that organic semiconductors intrinsically feature with carrier mobilities several orders of magnitude higher [4] and finer patterning resolution [5]. This leads to the conclusion that flexible electronic components or circuits requiring high performance in terms of frequency, noise, or power consumption would rely on the hybridation of thin inorganic technologies and organic substrate. Transistors on plastic reaching the GHz range have been reported in the literature [6–15], in addition to low noise devices [8,9,16] and high level of bendability [10,11,17], as summarized in Table 1. In this work, we elaborate on the transfer of mature CMOS technology from its initial rigid SOI substrate onto plastic film. A complete set a DC, RF, and noise characteristics is presented to fully demonstrate the potentialities of this technology as a major building block for fully flexible communicating devices.

2. Device fabrication

RF CMOS transistors with 64-gate fingers are first fully processed on initial HR SOI wafers using a conventional fabrication technology. The back side or handling layer of the original SOI wafer is subsequently completely removed, leaving only the topmost layers unaltered, that is, the buried oxide (BOX), the SOI layer, and the back-of-the-line interconnections network (Fig. 1a–c). This ultimately thinned layer system is hereafter referred to as the active die stack. It is finally transfer-bonded onto a plastic film in order to complete this fabrication process resulting in a fully flexible RF CMOS die (Fig. 1d and e).

2.1. Initial substrate removal

Bulk silicon removal is performed after bonding the front side of the initial processed CMOS die (Fig. 1a) onto a temporary sapphire carrier (Fig. 1b). Bonding is here achieved using a temporary – or sacrificial – SPR220 optical photoresist layer deposited on the front side of the processed CMOS die before contacting it with the sapphire wafer. The bonded stack is then annealed in an oven at

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Table 1
Comparison of RF and noise performance of electronic on plastic devices reaching the GHz range.

Reference	f_T/f_{MAX} (GHz)		NF_{min}/G_{ass} (dB)		Material	Device
This work [6,16]	150	160	0.57	17.8	Si	MOSFET
[7]	105	23	–	–	InAs	MOSFET
[8]	103	–	0.89	14.2	Si	MOSFET
[9]	48	–	1.1	12.0	Si	MOSFET
[10,11]	5	–	–	–	CNT	FET, TFT
[12]	3.8	12	–	–	Si	TFT
[13]	2.0	7.8	–	–	Si	TFT
[14]	1.9	3.1	–	–	Si	TFT
[15]	1.6	–	–	–	GaAs	MESFET

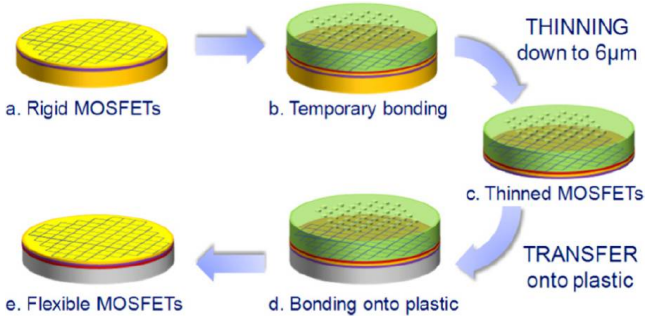

Fig. 1. Fabrication process flow chart. (a) Initial processed rigid CMOS die, (b) bonding of a temporary carrier on the front side of the CMOS die, (c) thinning of the back side of the CMOS die down to about 6 µm thick, (d) bonding of a plastic film on the back side of the thinned CMOS die, and (e) removal of the temporary carrier to achieve the transfer of the thinned CMOS die onto a plastic film.

100 °C during one hour in order to obtain adhesion strength strong enough to withstand the complete removal process of silicon handler, especially the shear stress generated during the chemical–mechanical lapping step. At the end of the transfer process (Fig. 1d and e), the dissolution of this sacrificial layer is enhanced by the fact that the temporary sapphire carrier is drilled with 1 mm diameter holes, enabling homogeneous and quick dissolution of this sacrificial photoresist layer.

After bonding the CMOS die onto its sapphire carrier, the thinning operation (Fig. 1c) is conducted by successively using chemical–mechanical lapping, chemical etching in a HF:HNO_3 solution and Si/SiO_2 selective dry cleaning in xenon difluoride (XeF_2) using the BOX as a stop-layer (Fig. 3), as reported in [6]. We report here on the optimized parameters resulting in large scale (few cm^2) and reliable thinning and transfer process. The first chemical–mechanical lapping step is performed using a *Logitech* PM5 lapping system, applying about 20 N of vertical force on the sample and rotating both the sample holder and the lapping plate at 50 rpm, ensuring a relatively homogeneous lapping. Alumina powder diluted in deionized water (10% w/w) is used as abrasive material. Lapping using a 15 µm diameter alumina powder is first performed to thin the CMOS die from 780 µm down to 200 µm. It is followed by abrasion with a 3 µm diameter powder down to 100 µm in order to increase the fracture strength of thinned dies [18]. Details about this first lapping step can be observed in Fig. 3, where the sample thickness over its complete area is represented after the three successive steps of the thinning process (Fig. 3b). Furthermore, the inhomogeneity associated with the two first steps is highlighted in Fig. 3c by plotting the variations of thickness versus distance from the center of the sample. After this coarse lapping step, a wet etch step in 1:9 HF(50%):HNO_3(65%) solution is applied on the 100 µm thick CMOS die still bonded on its sapphire carrier. In order to protect the edges of the CMOS die and the temporary photoresist in the perforated temporary carrier, a protecting layer of acid resistant wax (W from *Logitech* 10% w/v diluted chloroform) is deposited on the back side of the sapphire carrier and around the 100 µm thick CMOS die before wet etching. This step enables to further thin the CMOS stack down to 20 µm while increasing the fracture strength of the thinned die by removing subsurface damages [19]. At this stage, Fig. 3 also provides information on the resulting surface topography that displays an increased total thickness variation over the considered sample surface (Fig. 3c). Finally, after removing the protecting wax layer in chloroform, the final step devoted to the removal of the initial handling substrate is performed using dry etching of remaining silicon in XeF_2 (Xetch® X3 Series, *XACTIX*) featuring a Si:SiO_2 selectivity greater than 1000:1 [20]. Etching pulses of 10 s at 45 °C and at a pressure of 800 mTorr

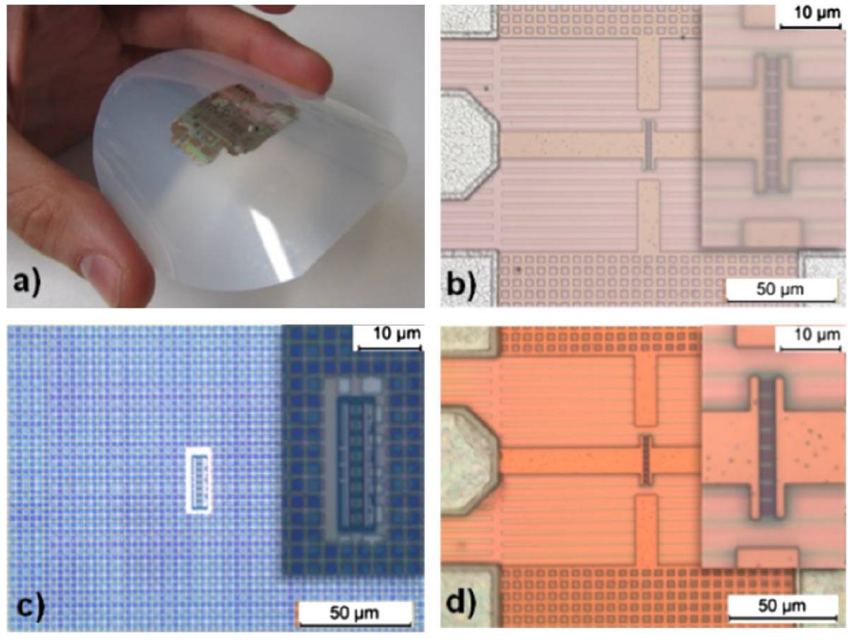

Fig. 2. (a) Fully processed RF-SOI-CMOS die after thinning and transfer onto a plastic film. Images of a transistor (b) on its initial rigid substrate before thinning, (c) after thinning, from the back side, and (d) after transfer on a plastic film.

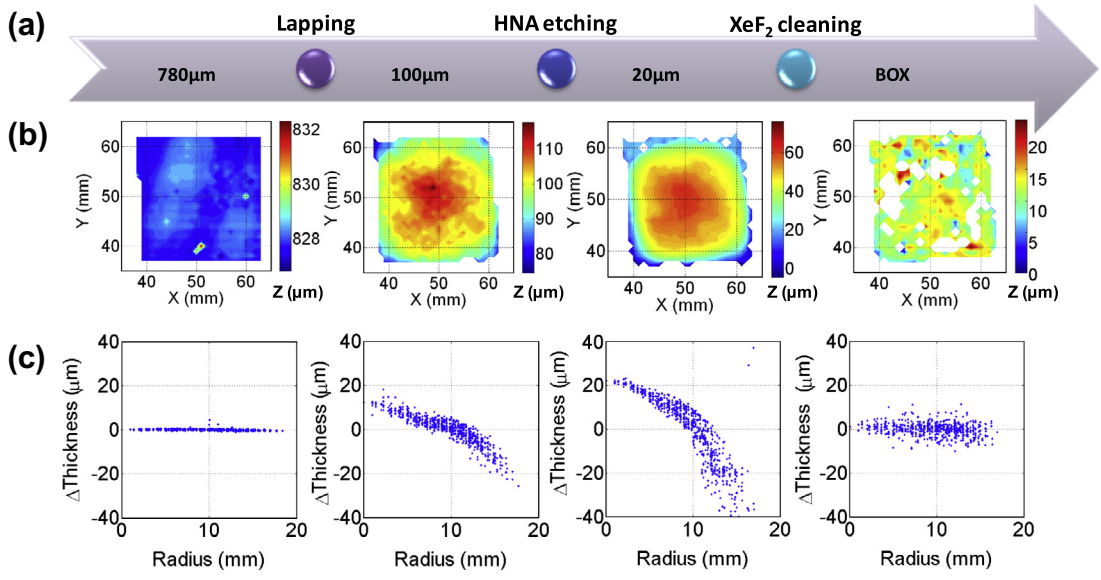

Fig. 3. (a) Description of the three-steps thinning process, (b) thickness measured along the CMOS die surface plotted before and after each etching step, and (c) thickness difference between measurement and least squares fitted plane, as a function of sample radius before and after each etching step.

during etching (and 3 Torr in the expansion chambers) are repeated until complete cleaning of the silicon handler. This method allows the gentle elimination of remaining silicon using the BOX as a stopping layer resulting in a much better thickness homogeneity as shown in Fig. 3. After complete removal of the initial silicon handler, the thinned active die stack only comprises a 5.5 µm thick interconnection network, the 60 nm thick active SOI layer, and the 145 nm thick BOX layer (Fig. 4).

2.2. Thinned processed die transfer

After completing the thinning procedure, the active die stack is transferred from the temporary carrier onto a plastic film using an epoxy-based resist (SU-8). This step is performed by thermo-compression for 30 min at 110 °C, that is, above the glass transition temperature of the unpolymerized photoresist, for 30 min, with 500 mbar of external pressure on both sides of the stack, using a SB6e wafer bonding system from *SÜSS MicroTech* (Fig. 1d). Performing this bonding step under vacuum prevents any air or gas to be trapped at the interface between the plastic film and the back side of the active die stack. Furthermore, a controlled cooling of the bonded stack with a 1 °C/min temperature ramp while still maintaining pressure on both sides of the stack limits bending due to thermal mismatch. The fabrication process is finalized with the release of the active die stack bonded onto the plastic film from the sapphire carrier by selective dissolution of the temporary adhesive layer in acetone. The perforated sapphire carrier allows a quick and homogeneous dissolution of the temporary adhesive photoresist layer without damaging the permanent epoxy adhesive layer and the organic film. Fig. 2a shows a picture of 65 nm CMOS circuit die after transfer-bonding onto a 125 µm thick PEN (polyethylene naphthalate) film. Optical microscope images zoomed onto the transistor gate fingers and the surrounding contact pads can be seen in Fig. 2b–d at different steps of the thinning and transfer procedure. These views demonstrate that the proposed thinning and transfer process can be performed at relatively large scale ($\sim 20 \times 30$ mm^2), resulting in a flexible CMOS chip (Fig. 2a). Furthermore, no visible degradation can be seen from optical microscopy characterizations neither after complete thinning on the back side of the BOX layer, nor after transfer on plastic from the front side of the CMOS chip. In particular, Fig. 2c shows the undamaged active area by transparency from the back side, and Fig. 2d presents a front side view of the topmost metal layer with visible contact pads and accesses to the transistor gate fingers. Fig. 4 presents a SEM image of a cross-section prepared by focused ion beam (FIB) of the active die stack after thinning and transfer-bonding onto a plastic substrate. This picture clearly highlights the final stacked layers comprising the six levels of interconnection network, the active SOI layer, the BOX layer, the SU-8 adhesive layer, and the plastic film. No visible degradation, debonding, or cracks can be seen on any of the six levels of interconnection (Fig. 4).

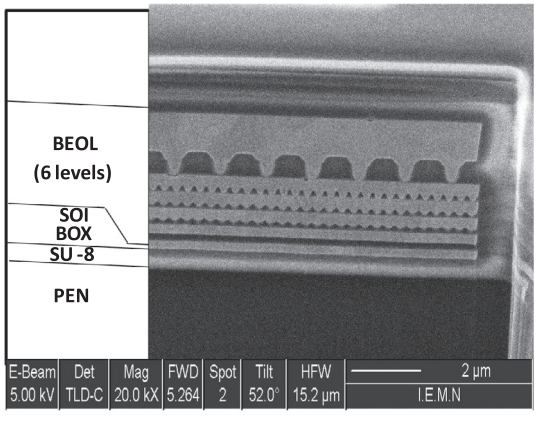

Fig. 4. Scanning Electron Microscope (SEM) image of a Focussed Ion Beam (FIB) cross-section of a fully processed RF-SOI-CMOS die after thinning and transfer onto a plastic film with scheme of the different layers of the imaged stack.

3. Electrical characterizations

Static, radio-frequency and noise measurements have been performed before and after transfer onto plastic films on 64-gate fingers n- and p-MOSFETs, featuring a 65 nm gate length and a unitary finger width of 1 µm.

3.1. DC characterization

Drain currents of almost 30 mA (469 mA/mm) and 15 mA (234 mA/mm) are demonstrated for n- and p-MOSFETs, respec-

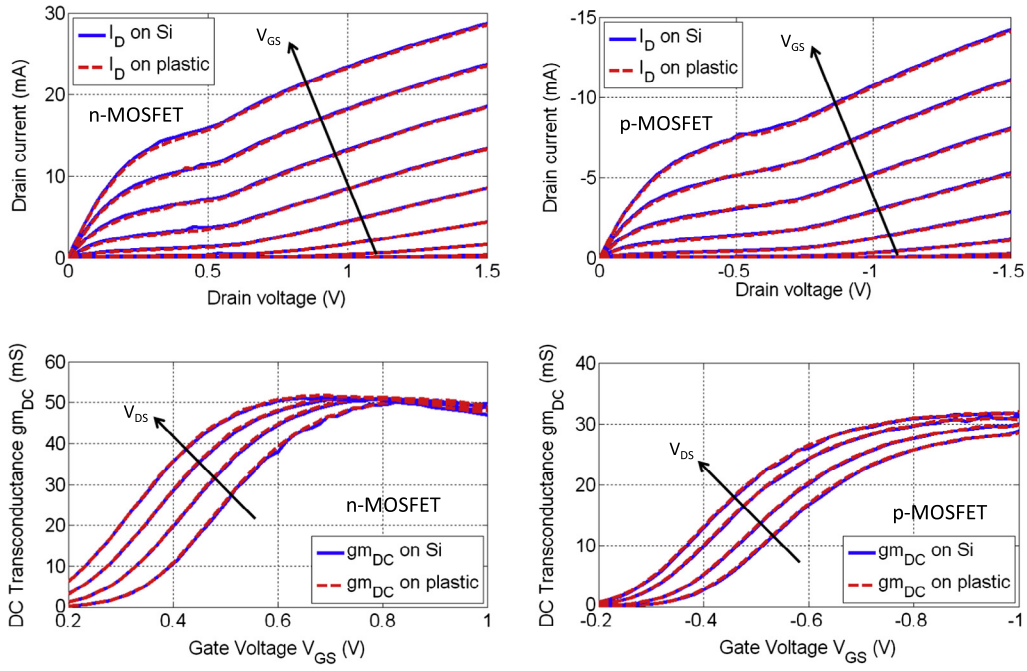

Fig. 5. Comparison of DC characteristic between SOI MOSFETs on their initial rigid substrate (blue lines) and on plastic (red dashed lines) for n- and p-MOSFETs: (a) *I–V* curve for n-MOSFETs, gate voltage V_{GS} varying from 0 V to 1.2 V, (b) *I–V* curves for p-MOSFETs, gate voltage V_{GS} varying from 0 V to −1.2 V, (c) DC transconductance for n-MOSFETs, drain voltage V_{DS} varying from 0.75 V to 1.5 V, and (d) DC transconductance for p-MOSFETs, drain voltage V_{DS} varying from −0.75 V to −1.5 V. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

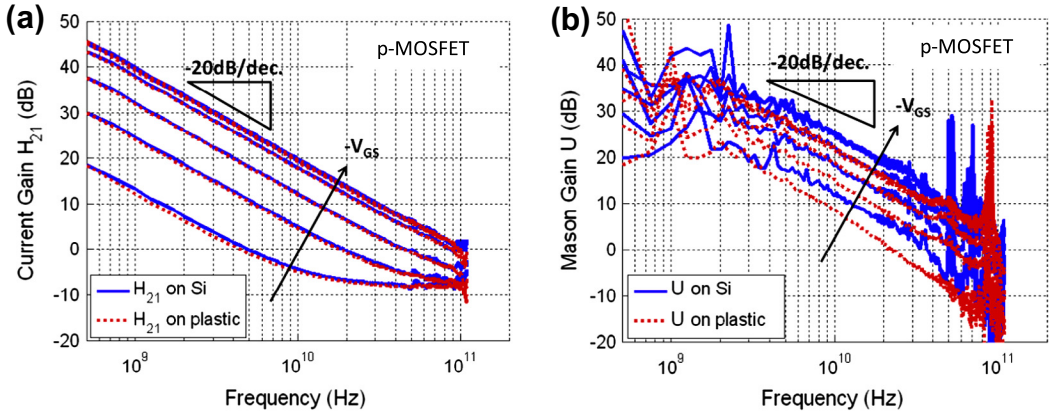

Fig. 6. Comparison of HF characteristic between SOI p-MOSFETs on their initial rigid substrate (blue lines) and on plastic (red dashed lines): (a) Current gain H_{21}, and (b) Mason's gain U as a function of frequency. Gate voltages V_{GS} varying from −200 mV to −1.0 V. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

tively, both on their initial rigid substrate and after transfer-bonding onto a plastic film (Fig. 5a and b). In addition, static transconductance of 50 mS for n-type and 30 mS for p-type devices are reported (Fig. 5c and d). Static characteristics presented in Fig. 5 fully demonstrate that no alteration of DC performance arises from the thinning and transfer process described hereinbefore, neither on n- nor on p-MOSFETs.

3.2. HF characterization

HF measurements presented in Fig. 6 and Ref. [6] have been performed using a Pad-Open-Short-Short (POSS) de-embedding methodology, as presented in [21]. The frequency-dependent current gain H_{21} of RF MOSFETs on their initial rigid HR SOI substrate and after transfer onto a plastic film has been reported for n- and p-type devices in previous work [6], and characteristics of p-MOSFETs are also shown in Fig. 6. Similar electrical behavior has been demonstrated regardless of the nature of the underlying substrate. It can also be observed that the experimental slope follows the theoretical value of −20 dB/decade for a wide range of gate voltages V_{GS}. This allows the extraction of the unity-current-gain cutoff frequencies f_T as a function of V_{GS}, or equivalently, as a function of the drain currents I_{DS}, as presented in Fig. 7a. The first important result that can be inferred from these graphs is that no modification of f_T can be observed after transfer-bonding of ultimately thinned RF-SOI-CMOS dies on a plastic film. Mason's gains U of RF MOSFETs on their initial rigid HR SOI substrate and after transfer onto a plastic film have also been reported for n- and p-type devices in [6] and Fig. 6. Again, similar behaviors and −20 dB/decade slopes have been obtained regardless of the underlying substrate. However, a slight decrease of the Mason's gain after transfer onto a plastic film can be observed for both transistor types. This leads to a decrease of the maximum

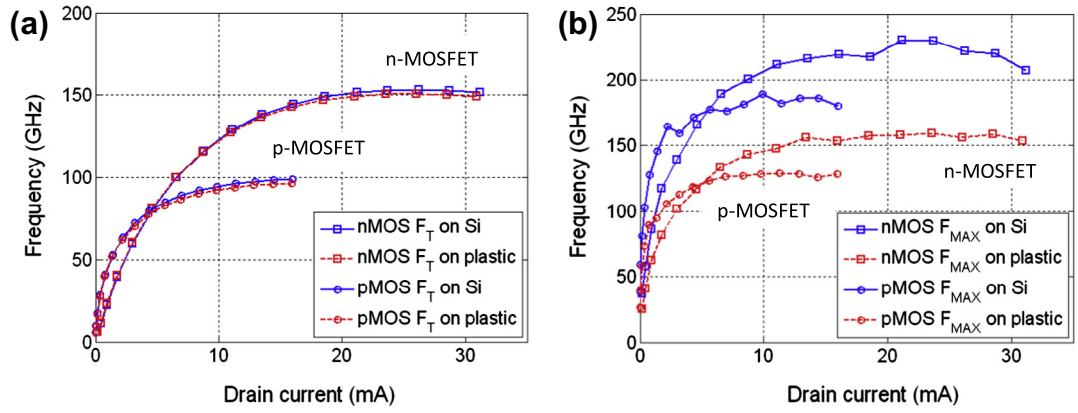

Fig. 7. Comparison of (a) unity-current-gain cutoff frequencies f_T and (b) maximum oscillation frequencies f_{MAX} between SOI MOSFETs on their initial rigid substrate (blue lines) and on plastic (red dashed lines) for n-MOSFETs (squares) and p-MOSFETs (circles) as a function of drain current. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

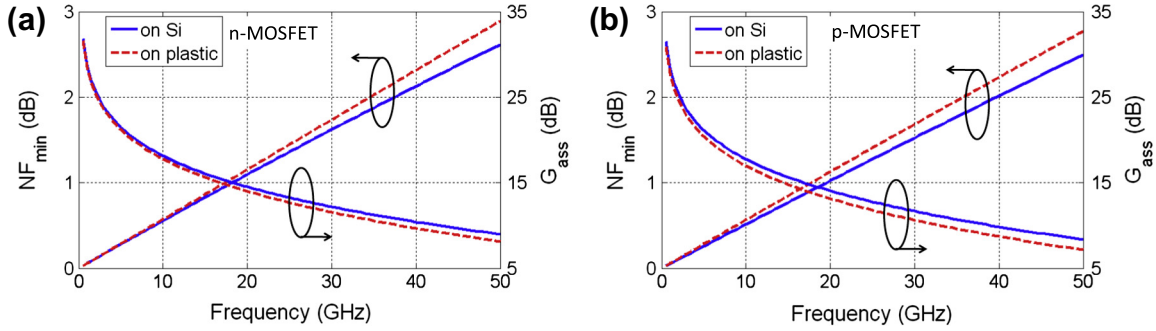

Fig. 8. Noise figures of merit NF_{min} (minimal noise figure) and G_{ass} (associated gain) measured on rigid substrate (blue lines) and on organic film (red dashed lines) for (a) n-MOSFET and (b) p-MOSFET. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

oscillation frequencies f_{MAX}, as presented in Fig. 7b for n- and p-type devices on both rigid and organic substrates as a function of the drain current I_{DS}. Unlike f_T, the f_{MAX} figure-of-merit is reduced by 25–30% at the highest current levels. In an attempt to identify the origin of f_{MAX} degradation, the extraction of the Small Signal Equivalent Circuit (SSEC) has been achieved for both n- and p-MOSFETs according to the strategy described in [21]. A comparison of intrinsic and extrinsic extracted parameters [16] reveals that f_{MAX} performance reduction associated with the plastic substrate can be attributed to an increase of the gate resistance resulting from the fabrication process, as explained in [6]. It is emphasized here that invariant unity-current-gain cutoff frequencies f_T are demonstrated over a large set of bias conditions.

3.3. Noise characterization

In addition to static and radio-frequency measurements, noise characteristics have been measured using the F_{50} method [22]. Noise measurements have been performed in the 6–20 GHz and 20–40 GHz ranges using two different noise setups taking into account the actual noise source impedance (around 50 Ω) as presented in [16]. A modeled NF_{50} is then fitted on the noise measurements using the SSEC described in [21] with the addition of two uncorrelated noise sources, corresponding to input and output temperatures T_{in} and T_{out} [22]. The input temperature is fixed at room temperature and the output temperature fitted to obtain the best agreement with measured data. T_{out} of 1221 K and 1162 K are obtained for the p-MOSFET on its initial substrate and after transfer onto a plastic film, respectively. Similar noise behavior is obtained regardless of the substrate as presented for n-MOSFETs only in [16], where T_{out} of 1412 K and 1372 K were obtained. From these 50 Ω noise figures NF_{50} measurements and the noisy SSEC, the four noise figures of merit can be extracted [22]. Fig. 8 presents the minimal noise figure NF_{min} and the associated gain G_{ass} as a function of frequency for n- and p-MOSFETs on both substrate types. Remarkably, Fig. 8 demonstrates the invariability of noise performance upon thinning and transfer onto the PEN film.

4. Discussion

As summarized in Table 1, present results outperform the previous state-of-the-art reported by Kao et al. for a 130 nm CMOS technology [8]. Figures reported here demonstrate f_T/f_{MAX} = 150/160 GHz for n- and 100/130 GHz for p-MOSFETs on plastic, and NF_{min}/G_{ass} = 0.57/17.8 dB for n- and 0.57/17.0 dB for p-MOSFETs, respectively. Owing to almost invariant RF characteristics, it is anticipated that RF-MOS circuits such as low noise amplifiers (LNAs) are capable to maintain performance levels very close to their counterpart on conventional bulk substrate. Another expected direct benefit of the above analysis is that complex RF integrated functions could be directly implemented on flexible plastic without resorting to a costly and tedious re-design of circuits.

5. Conclusion

In this paper, high frequency and low noise MOSFETs have been reported on a plastic film. The common use of mature 65 nm node SOI-CMOS technology with a new transfer method allows the fabri-

cation of high performance, low noise MOSFETs on plastic foils that opens tremendous perspectives for the development of numerous flexible, nomadic and space, weight, and power (SWAP)-constrained applications. Future investigations will bear on the characterization of CMOS circuits on plastic and electrical performance variation of flexible MOSFETs under external mechanical strain.

References

[1] Raynaud C et al. Advanced SOI technology for RF applications short course. New York: John Wiley & Sons; 1980.
[2] Reuss RH et al. Macroelectronics: perspectives on technology and applications. Proc IEEE 2005;93:1239–56.
[3] Burghartz JN et al. Ultra-thin chips and related applications, a new paradigm in silicon technology. In: Proc solid state device research conference ESSDERC'09; 2009. p. 28–35.
[4] Schön JH et al. On the intrinsic limits of pentacene field-effect transistors. Org Electron 2000;1:57–64.
[5] Halonen E, et al. Evaluation of printed electronics manufacturing line with sensor platform application. In: Proc Eur Microelectron Packag Conf; 2009. p. 1–8.
[6] Lecavelier des Etangs-Levallois A et al. 150-GHz RF SOI-CMOS Technology in ultrathin regime on organic substrate. IEEE Electron Dev Lett 2011;32:1510–2.
[7] Wang C et al. Self-aligned, extremely high frequency III–V metal–oxide–semiconductor field-effect transistors on rigid and flexible substrates. Nano Lett 2012;12:4140–5.
[8] Kao HL et al. Low noise and high gain RF MOSFETs on plastic substrates. Microwave symposium digest. In: 2005 IEEE MTT-S International; 2005. p. 2043–2046.
[9] Kao HL et al. Low noise RF MOSFETs on flexible plastic substrates. IEEE Electron Dev Lett 2005;26:489.
[10] Chimot N et al. Gigahertz frequency flexible carbon nanotube transistors. Appl Phys Lett 2007;91(153):111.
[11] Vaillancourt J et al. All ink-jet-printed carbon nanotube thin-film transistor on a polyimide substrate with an ultrahigh operating frequency of over 5 GHz. Appl Phys Lett 2008;93(243):301.
[12] Sun L et al. 12-GHz thin-film transistors on transferrable silicon nanomembranes for high-performance flexible electronics. Small 2010;6:2553–7.
[13] Yuan H-C et al. 7.8-GHz flexible thin-film transistors on a low-temperature plastic substrate. J Appl Phys 2007;102(034):501.
[14] Yuan H-C et al. Microwave thin-film transistors using Si nanomembranes on flexible polymer substrate. Appl Phys Lett 2006;89(212):105.
[15] Sun Y et al. Gigahertz operation in flexible transistors on plastic substrates. Appl Phys Lett 2006;88(183):509.
[16] Tagro Y et al. High frequency noise potentialities of reported cmos 65 nm soi technology on flexible substrate. In: IEEE 12th topical meeting on silicon monolithic integrated circuits in RF systems; 2012. p. 89–92.
[17] Lesecq M et al. High performance of AlGaN/GaN HEMTs reported on adhesive flexible tape. IEEE Electron Dev Lett 2011;32:143.
[18] Takyu S et al. A Study on chip thinning process for ultra thin memory devices. In: IEEE Elec Comp & Tech Conf Proc; 2008. p. 1511–16.
[19] Burghartz JN et al. A new fabrication and assembly process for ultrathin chips. IEEE Trans Electron Dev 2009;56:312–27.
[20] Ibbotson DE et al. Comparison of XeF_2 and F-atom reactions with Si and SiO_2. Appl Phys Lett 1984;44:1129–31.
[21] Waldhoff N et al. Improved characterization methology for MOSFETs up to 220 GHz. IEEE Trans Microw Theory Technol 2009;57:121237–43.
[22] Dambrine G et al. A new method for on wafer noise measurement. IEEE Trans Microw Theory Technol 1993;41:375–81.