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Change in Admittance of HfO_2 Metal-Insulator-Metal (MIM) Capacitors after dc Bias Stress

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We report on the admittance of Au/HfO_2/TiN MIM capacitors which have been subjected to a dc bias stress (3 V for films with an equivalent oxide thickness of 3.25 nm). Different stress conditions are applied, and the resulting capacitance and ac conductance are measured as a function of frequency. Though charge trapping and dc leakage current are observed under short stress time (1500 s), after bias removal the ac admittance is not affected. This underlies the ability of the capacitor to recover from stress. After longer stress times (10000 s), the capacitance decreases, achieving negative values at very low frequencies. Such a degradation is ascribed to important charge trapping.

Metal-Insulator-Metal (MIM) capacitors are used in integrated circuits for a wide range of applications, such as decoupling, filtering, analog-to-digital conversion, and data storage (Dynamic Random Access Memories, DRAMs). Hence, it is important to study the reliability of MIM devices. During operation, MIM capacitors may be subjected to a dc bias stress. The effect of a dc bias stress on the leakage current in MIM structures is well documented (studies of stress-induced leakage current, SILC). However, less is known about the effect of a bias stress on the capacitance. In the past, a few works have addressed stress-induced modification of the capacitance (C) in dielectrics.[1,2] Upon biasing NaCl crystals, it was observed that there was an initial rapid rise of C, followed by a slow decay of C with time.[1] A similar behavior was reported for anodic Al_2O_3.[2] Renewed attention was recently paid to such effects in MIM capacitors.[3–7] In HfAlO films (17 nm), after bias stressing, C is increased. The longer is the biasing time, the higher is the capacitance increase.[3] A similar behavior is observed for Lu_2O_3 films (10–20 nm)[5] and for Al_2O_3 (2 nm) / HfO_2 (11 nm) / Al_2O_3 (2 nm) stacks.[7] Contrary to these results, C is observed to decrease in $SrTiO_3$ films[4] and SiO_2 (3–9 nm) / Si_3N_4 (12 nm) / SiO_2 (3-4 nm) stacks.[6] Capacitance variations are related to defect creation[3] or to charge trapping.[5,7]

Hafnium oxide (HfO_2) has attracted a great deal of attention as a high-k material for integrated Metal-Insulator-Metal (MIM) capacitors.[8,9] So far, no study has been reported on the bias stress effect on the admittance of HfO_2 capacitors. This is the main point addressed in the present study.

Experimental

HfO_2 films (10 nm thick) are grown by atomic layer deposition (ALD) on TiN. Top gold electrodes (2 mm in diameter) are deposited on the HfO_2 to constitute TiN/HfO_2/Au capacitors. The dielectric constant of the films is around 12. More information on deposition technique and films properties can be found elsewhere.[10] A dc bias stressing is applied at room temperature for different amounts of time. The dc bias (3 V) is applied on the top gold electrode, the TiN electrode being grounded. Current-time (I–t) characteristics are recorded during bias stressing to monitor insulation degradation. After bias removal, impedance spectroscopy is carried out to assess change in the admittance. The admittance ($Y = G + j2\pi Cf$, where G is the conductance and C is the capacitance) of MIM structures is measured with a Novocontrol Analyzer in the 0.1 Hz to 10^4 Hz frequency range (analysis was limited to 10 kHz because of series resistance). Admittance measurements are performed at room temperature with an ac voltage of 0.1 V_{RMS}.

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Results and Discussion

Fig. 1 shows the I-t recorded during bias stressing and the resulting C-f and G–f characteristics. The I-t was discussed in details in previous works.[11,12] Briefly, an absorption current is first observed ($t < 10$ s, I decreases), and then SILC dominates ($t > 10$ s, I increases). The absorption current was related to electron trapping at grain boundaries.[12] The effect of charge trapping on the capacitance will be discussed later. SILC was ascribed to the formation of defect conduction paths extending across the oxide thickness. Upon hot electron injection, oxygen vacancies (V_O^{2+}) are created in the bulk and oxygen ions (O^{2-}) are drifted to the anode. Electronic hopping conduction proceeds via V_O^{2+} defects. As time elapses, more V_O^{2+} are created and consequently hopping conduction rises ($t > 10$ s in Fig. 1a). SILC was modeled taking into account trap creation kinetics and time-dependent trap population.[11]

Applying a bias during 1500 s does not modify the admittance (Fig. 1). The I-t curve shows that the dc current rises up to 5×10^{-6} A at $t = 1500$ s. For a bias of 3 V, this current level corresponds to a dc conductance of about 10^{-6} S. Therefore, one could expect to see a conductance plateau of 10^{-6} S in the G-f characteristics. However, the ac conductance is not modified (see Fig. 1c). To understand this behavior, it must be remembered that admittance measurements are performed *after* bias stress. Conduction paths, which are formed during bias stressing, do not remain permanently. They disappear rapidly enough to show no difference in G. This is consistent with recovery previously observed when performing I-t cycling.[11] As explained above, upon bias application, V_O^{2+} are created and form filamentary conduction paths which short-circuit the dielectric thickness. At the same time, O^{2-} ions are drifted to the anode where they pile up. When the bias is removed, O^{2-} ions back-diffuse from the anode to the bulk where they recombine with V_O^{2+} and annihilate conduction paths. Thus, once the bias is removed, V_O^{2+} conduction paths rapidly disappear (at least the part close to the anode) and the G-f measurements only display the conductance related to the intrinsic dielectric loss ("rapidly" means that the sample recovers in a time shorter than the time necessary to disconnect the dc bias source and to connect the impedancemeter, ~1 min).

Change in admittance appears for more severe stress (10000 s, Fig. 2). In the I-t characteristic, the dc conductance rises up to 2×10^{-4} S (Fig. 2a). In that case, a plateau of the same value is observed in the G-f characteristics during the first seconds of measurements (i.e. at high frequencies, the impedance measurements are carried out starting from 10^4 Hz, see Fig. 2c). As the measurement proceeds (decreasing f) the G-f merges with the intrinsic characteristic. This confirms that the sample recovers after bias removal.

An important modification which emerges after a stress time of 10000 s is capacitance decrease (Fig. 2b). More precisely, the C-f

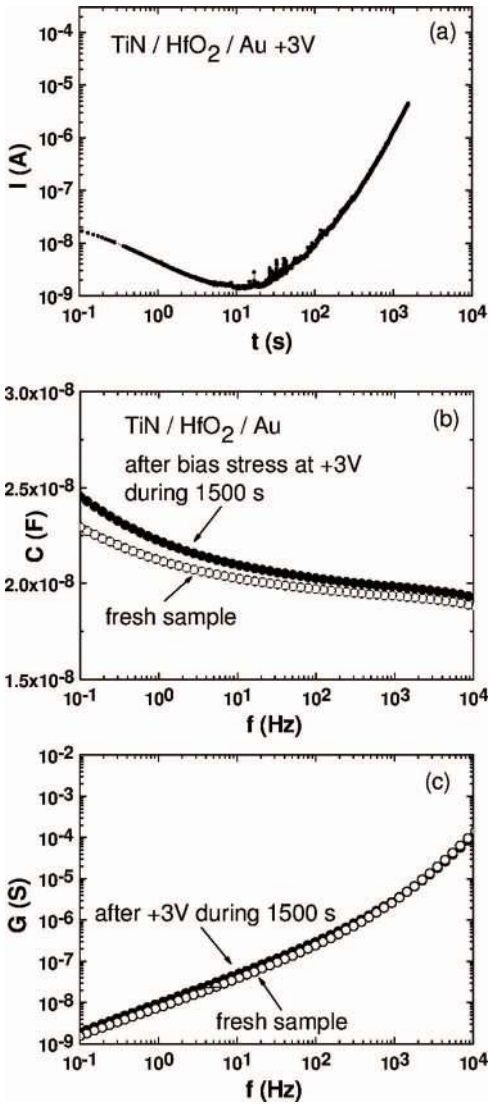

Figure 1. Sample stressed at 3 V during 1500 s. (a) I-t recorded during bias stress. (b) C-f characteristic recorded after bias stress. (c) G-f after stress.

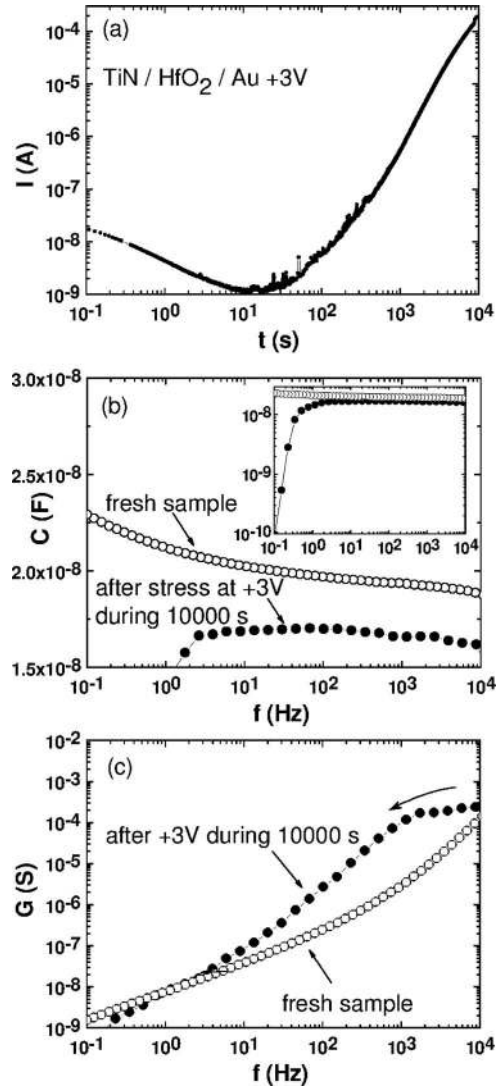

Figure 2. Sample stressed at 3 V during 10000 s. (a) I-t recorded during bias stress. (b) C-f characteristic recorded after bias stress. (c) G-f after stress. As indicated by the arrow, frequency is swept from 10^4 Hz (beginning of measurement) to 10^{-1} Hz.

characteristic displays two distinct behaviors according to the frequency range. For $f > f_c$ (a characteristic frequency) C is divided by a constant factor (A), while for $f < f_c$ there is an abrupt decrease (by two decades). In Fig. 2b, $f_c \approx 2$ Hz and $A \approx 1.15$. For the purpose of comparison, it is interesting to observe C-f and G-f for a sample where hard-breakdown occurred (Fig. 3). Sample in Fig. 3 is a sample which has been subjected to a cumulative stress. Up to 200 s (380 s cumulated stress time), impedance is not modified (similar to sample in Fig. 1). Further 300 s stress leads the sample to breakdown. This is detected as a very high conductance in Fig. 3b (0.01 S). The breakdown field of our sample is 4 V (as deduced from resistance switching studies).[13] Therefore, a bias stress of 3 V sometimes lead to hard-breakdown after a few 100 s (statistical variation from sample to sample). For such samples, no recovery is observed (G remains fixed at 0.01 S after bias removal). It is believed that a large density of V_O^{2+} filaments are formed, leading to a thermal runaway (large damage which cannot be recovered).[11] Still, after breakdown a capacitance can be measured (Fig. 3a), which displays the same behavior as the one observed after a 10000 s stress (Fig. 2b). For the breakdown case, $f_c \approx 20$ Hz and $A \approx 5.8$ (Fig. 3a). When $f < f_c$, C drops toward negative values ($C<0$). It is noted that the C decrease ($A = 1.15$ for a 10000 s stress, $A \approx 5.8$ when breakdown occurred) is not proportional to the dc conductance (10^{-4} S for a 10000 s stress, 10^{-2} S in case of breakdown). Thus, C decrease is not due to an effective area reduction (surface occupied by conducting paths). Moreover, it is noted that the abrupt C drop ($f < f_c$) is not linked to a high conductance state (compare Fig. 2b and Fig. 2c). It is concluded that the C decrease is not correlated to the appearance of conducting paths across the dielectric thickness.

It is proposed that C decreases as a result of charge trapping (see schematic description in Fig. 4). Upon biasing, trapped charge builds up close to the electrodes (this trapped charge is at the origin of the absorption current, Fig. 1a and Fig. 2a). By considering the trapped charge (σ_t), the free charge at electrodes (σ_f), and bulk dielectric polarization (σ_p), the electric field in the sample (E) can be written as (Gauss law):

$$E = (\sigma_f/\varepsilon_0) - (\sigma_p/\varepsilon_0) + (\sigma_t/\varepsilon_0) \quad [1]$$

Using the electric displacement $D = \sigma_f$ and the polarization $P = \sigma_p$, Eq. 1 is rewritten as:

$$D = \varepsilon_0 E + P - \sigma_t \quad [2]$$

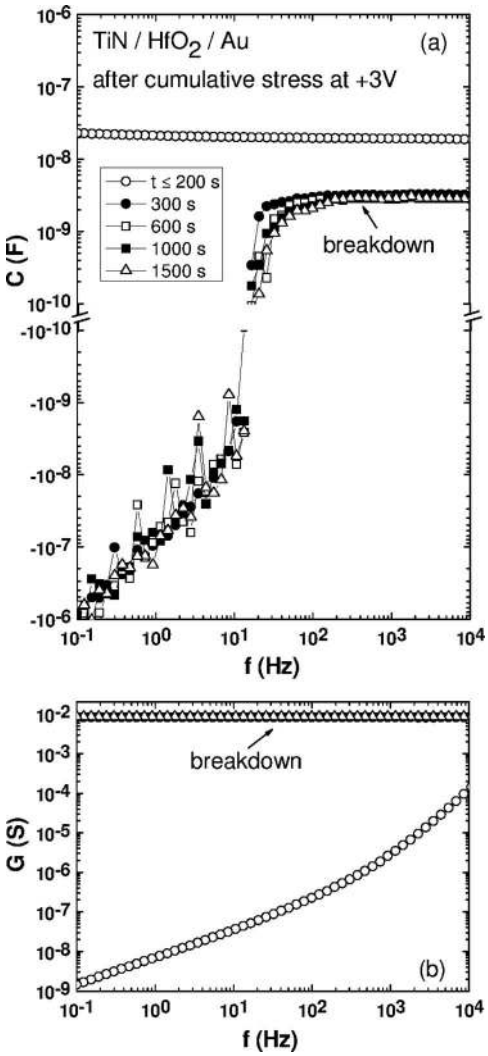

Figure 3. Sample subjected to hard-breakdown. (a) C-f characteristic. (b) G-f characteristic. The sample receives cumulative stresses at 3 V during 10, 20, 50, 100, and 200 s (labeled as " $t \leq 200$ s " in figure). Breakdown occurs for further 300 s stress. Further stresses (600, 1000, 1500 s) do not modify the admittance.

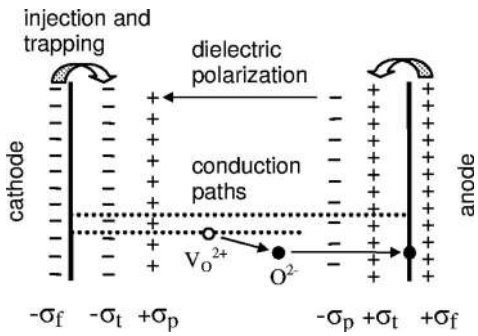

Figure 4. Schematic description of electric phenomena in the MIM capacitors. It shows the free charge at electrodes (σ_f, or D) and dielectric polarization (σ_p, or P). Bias leads to trapped charge at defects close to interfaces (σ_t). At present the origin of these defects is unknown (intrinsic defects). Trapped charge comes from electron injection (hole injection, i.e. positive σ_t is depicted at the anode, but this does not modify conclusions). Bias also gives rise to conduction paths which are made of oxygen vacancies (V_O^{2+}). Such defects are created by hot electron injection (liberating mobile oxygen ions, O^{2-}).

Eq. 2 clearly shows that the existence of trapped charge decreases D, i.e. the capacitance. In other words, the trapped charge (σ_t) compensates dielectric polarization (P), and consequently less free charge (D) is induced at electrodes (capacitance decreases). Trapped charge is observed to vanish rapidly when the bias is removed (desorption current, the traps depopulate).[12] Thus, depending on the initial trapped charge density (related to the bias holding time) and the time given to the sample to recover (traps depopulation), a C decrease can be observed (Fig. 2) or not (Fig. 1). When breakdown occurs (Fig. 3), more defects are created, the trapped charge density is higher, and the C decrease is more important.

Finally, the appearance of negative C is consistent with charge trapping, as suggested in metal-semiconductor interfaces[14] and organic diodes[15] where $C < 0$ is also observed. The ac voltage (0.1 V rms) is too low to inject electrons, but it modulates trap population. Traps respond to ac modulation with delay. If emission from traps is slow, then there is a current (charge emission from traps) which lags behind the ac voltage, giving rise to negative C.[14,15]

Conclusion

A dc bias stress induces leakage currents (SILC) and charge trapping. However, after bias removal the sample is able to recover, and the admittance is left unaffected. It is only for severe stresses (several 1000 s, at a bias close to breakdown voltage) that changes in admittance are observed. The capacitance decreases, to achieve negative values at low frequencies. This is ascribed to trapped charges. There is an obvious time dependence in the observed phenomena (recovery) which needs to be further studied. Future work will address change in capacitance during bias stress, and its time evolution just after bias removal.

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