HAL
open science

# A K-band BiCMOS Low duty-cycle Resistive Mixer

Alessandro Magnani, Christophe Viallon, Ioan Burciu, Thomas Epert, Mattia Borgarino, Thierry Parra

## To cite this version:

Alessandro Magnani, Christophe Viallon, Ioan Burciu, Thomas Epert, Mattia Borgarino, et al.. A K-band BiCMOS Low duty-cycle Resistive Mixer. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF 2014), Jan 2014, Newport Beach, United States. hal-00907835

**HAL Id: hal-00907835**

**https://hal.science/hal-00907835v1**

Submitted on 21 Feb 2014

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# A K-band BiCMOS Low duty-cycle Resistive Mixer

Alessandro Magnani[1,2], Christophe Viallon[1], Ioan Burciu[1], Thomas Epert[1,3], Mattia Borgarino[2] and Thierry Parra[1]

[1]University of Toulouse ; UPS ; LAAS ; Toulouse, France
[2]University of Modena and Reggio Emilia, Modena, Italy
[3]AXESS Europe, Toulouse, France

***Abstract*— This paper presents a double-balanced down-converter based on a low duty-cycle passive mixer that translates a 18.8 GHz RF signal into a 1 GHz IF signal. The resistive mixer is driven by two analog specially designed pulse generators in order to provide very low conversion losses at high frequencies. The chip has been processed using a 0.13 µm BiCMOS technology. With a −1.2 dBm input LO power, the overall measured conversion gain is 13.2 dB with an estimated contribution of only −2.1 dB from the passive mixer. The measured noise figure is 6.3 dB. The input-referred 1 dB compression point, hardly limited by the IF amp, is −25.7 dB, with −5 dBm for the mixer itself. Total power consumption is 109 mW.**

***Index Terms*— Resistive Mixer, Low Duty-cycle Passive Mixer, Sampling Mixer, Pulse Generator.**

## I. Introduction

During the last decade, passive mixer has become a very suitable choice in low or zero-IF receivers thanks to its no inherent 1/f noise and low intermodulation characteristics. More recently, 25% duty-cycle LO driving clock has been introduced [1]. This technique cancels out the crosstalk that is observed in IQ receivers featuring a 50% duty-cycle LO signal and increases the overall receiver's gain by at least 3 dB [2] [3]. Additionnally, when used in a voltage-driven configuration, the resistive mixer operates as a sampler and the conversion losses are almost entirely cancelled theoretically [4]. However, the circuits involved in the generation of a low duty-cycle LO driving signal are frequency-limited and cannot be pushed beyond few GHz [5], which greatly limits the number of applications targeted by such architecture.

The objective of this paper is to demonstrate that a low duty-cycle voltage-conveyor resistive mixer is applicable at higher frequencies using adequate pulse generators to create the required LO driving voltage. A chip operating inside K-band has been designed and processed. The mixer and the pulse generator are described in sections II and measured data are given in the last section.

## II. Circuit description

The chip block diagram is presented in Fig.1a. No LNA has been integrated before the mixer in order to allow a wide range of test frequencies. The resistive mixer (Fig.1b) operates as a sampled voltage conveyor. Its IF side is loaded by the capacitive high input impedance of the IF amplifier ($R_{out}C_{out}$) to hold the IF voltage value during a LO period. This amplifier is optimized to operate at a central frequency of 1 GHz.

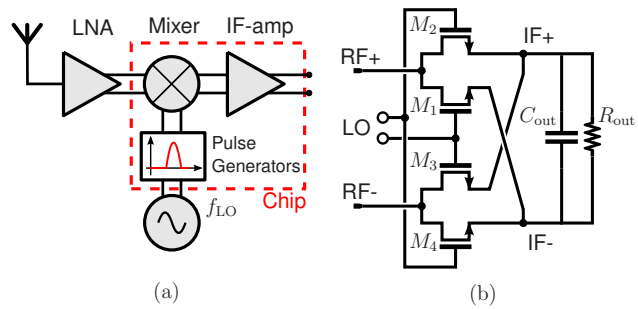


Fig. 1. (a) designed chip, and (b) details of the passive mixer

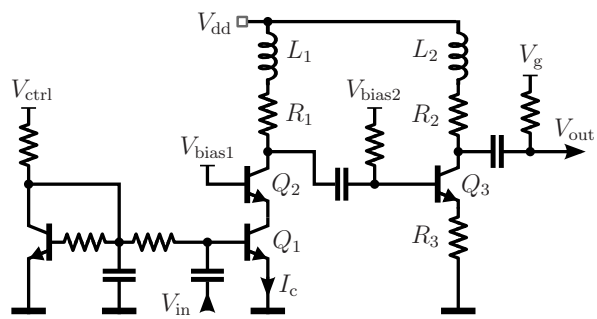


Fig. 2. Schematic of the pulse generator

Both pulse generators are connected to the LO side of the mixer to create the required low duty-cycle voltage waveforms. Common circuits are based on CMOS logic latch and gates [6] and are no longer suitable for pulse generation above approximately 5 GHz [5]. A non-linear analog approach has been preferred. All efforts have been focused on getting a low duty-cycle outgoing rectangular voltage waveform by lowering rise and fall times which are limited by active devices as well interconnects parasitics.

The pulse generator schematic is presented in Fig.2. Heterojunction bipolar transistors (HBT) have been preferred

here instead of NMOS devices thanks to their much higher $f_t$. The circuit involves a class-C cascode amplifier ($Q_1$ & $Q_2$) that creates a high duty-cycle voltage waveform. This signal is then reversed and amplified through a class-A inverting amplifier built around $Q_3$. The duty-cycle and amplitude of the outgoing signal is controlled by the DC voltage applied to $V_{ctrl}$ pin. Inductors $L_1$ and $L_2$ provide some peaking and improve the shape of the impulsion at the highest frequencies.

## III. Experimental Results

The circuit has been processed using a 0.13 µm BiCMOS SiGe technology from IBM. The die photograph is shown in Fig.3. The dimensions of the chip are $1.2 \times 2.4\ mm^2$. The whole system is biased under 2.4 V and consumes 109 mW that splits into 87 mW for both pulse generators and 22 mW for the IF-amp.

The test-bench used for mixer characterization is presented in Fig.4. The chip has been on-wafer measured using RF-probes at RF and IF ports. A VNA Agilent PNA-X N5247A delivers the CW RF differential signal thanks to its ability to accurately control phase and amplitude of its internal sources. This solution is far more flexible, accurate and broadband than using an external balun. The IF balanced outputs are connected to an external 180° hybrid coupler through a GSSG RF-probe. A rat-race balun has been designed on a 5 mils alumina substrate to provide a balanced LO signal to the chip. Its measured center frequency, around 17.8 GHz, has driven the experiments. At this frequency, the output voltage of a pulse generator is around 630 $mV_{pp}$ with a 27% duty-cycle.

Finally, cables, RF-probes and balun are de-embedded from measurements to shift the RF and IF reference planes to the pads of the chip.

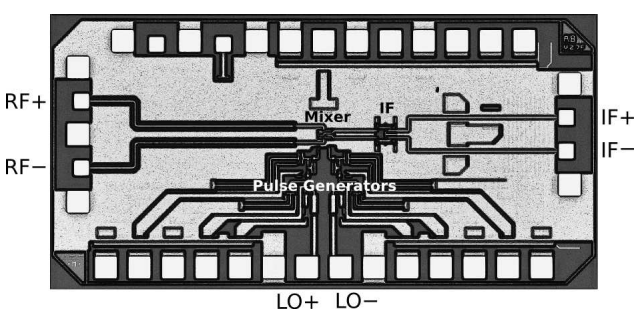


Fig. 3. Die photograph of the fabricated down-converter

### A. Conversion Gain

Fig.5 shows simulated and measured power conversion gains for $f_{RF} = 18.8$ GHz and $f_{LO} = 17.8$ GHz. Electrical simulations agree very well with measurements with a nearly constant offset of 0.2 dB in favor of simulations within the displayed LO power range. Knowing the simulated voltage gain of the IF amplifier, the mixer contribution can be estimated to −2.1 dB. This result is very close to the −1.9 dB predicted by the theory [4].

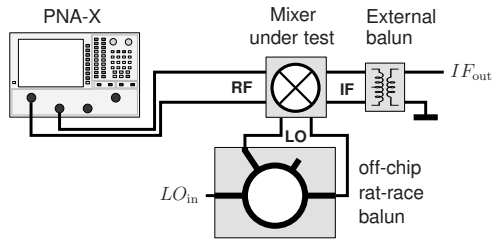


Fig. 4. Test-bench used for mixer characterization

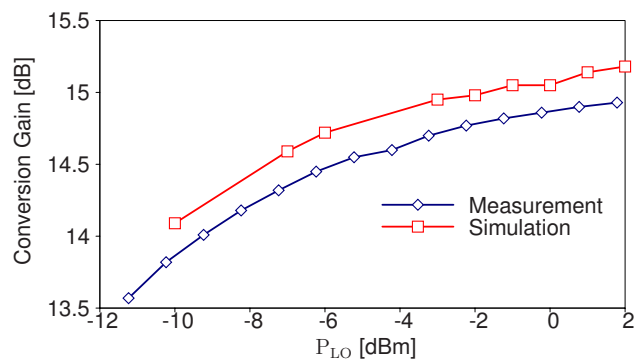


Fig. 5. Measured and simulated conversion gain

### B. 1dB Compression Point

Measured and simulated input-referred 1 dB compression points are −25.7 dBm and −24.5 dBm respectively. They are limited by the IF amplifier. Using simulations, we have been able to extract an input-referred 1 dB compression point of −5 dBm for the passive mixer alone. The linearity of the ring mixer is mainly limited by the rise and fall times of the LO pulses [7]. These switching times are minimized using small sized NMOS devices ($36 \times 0.12\mu m^2$) within mixer, as well as short interconnects, that are needed to reduce the capacitive load presented at the output of each pulse generator.

### C. Noise Figure

The noise figure is measured using the cold source technique. Two 50 Ω room temperature loads are connected to the RF balanced port of the mixer. The noise power $N_{mix}$ produced at the output of the circuit is then amplified by a LNA and measured using a spectrum analyzer. The test-bench contribution is de-embedded from the measured noise, and the equivalent noise temperature of the mixer $T_{mix}$ is computed using (1):

$$T_{mix} = \frac{N_{mix}}{\sum G_c \cdot \Delta f} \tag{1}$$

This relation requires the knowledge of all the RF frequency bands centered at $kf_{OL} \pm f_{IF}$ ($k \in \mathbb{N}$) from

which a significant conversion occurs inside the mixer. Fortunately, conversion gains vanish as $k$ increases. The noise figure is finally obtained from $T_{mix}$ using the relation (2), where $T_0$ is 290 K:

$$NF_{mix} = 1 + \frac{T_{mix}}{T_0} \tag{2}$$

This calculated noise figure is equivalent to an all-sidebands (ASB) definition.

Thanks to the PNA-X connected at RF ports, conversion gains around the $2^{nd}$ and $3^{rd}$ LO harmonics are extracted (Fig.6). These measurements show that frequency translations from 52.4 GHz and 54.4 GHz are significant, which was predicted by the electrical simulations as well as low conversions observed around the $2^{nd}$ LO harmonic. This behaviour may be very interesting for V-band applications, but it is out of the scope of this paper.

Finally, the noise figure is extracted from (1) and (2) and shown in Fig.7. A minimum NF of 6.3 dB is obtained at a $-1.2$ dBm LO power. Although noise contribution of the IF amplifier is included, this result represents a significant improvement against any usual 50% duty-cyle driven passive mixer, penalized by its conversion losses.

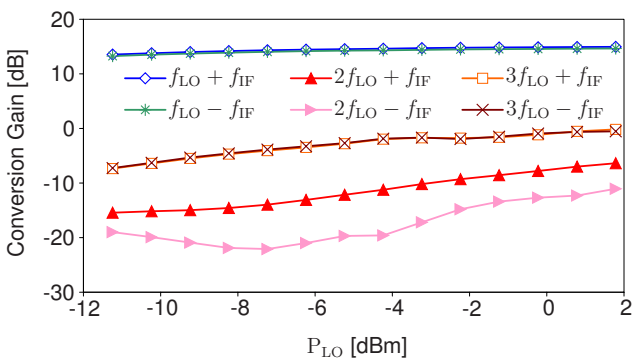


Fig. 6. Measured conversion gains around $1^{st}$ to $3^{rd}$ LO harmonics

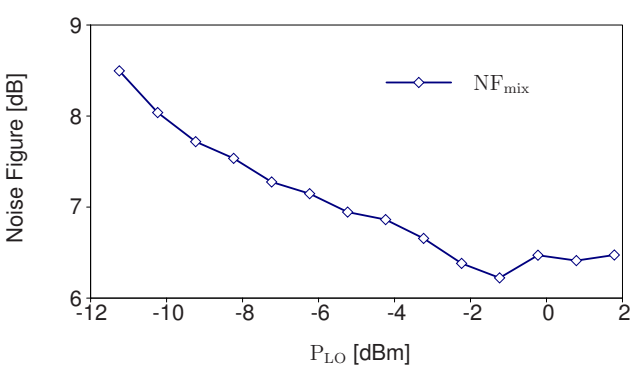


Fig. 7. Measured noise figure

## IV. Conclusion

The low duty-cycle passive mixer is widely used for low or zero-IF IQ receivers up to few GHz. However this architecture suffers from frequency-limited digital circuits for LO signal generation. This paper has shown how to extend the frequency range of such mixer up to within the K-band, replacing these CMOS digital clocks by non-linear analog pulse generators.

The designed circuit, including pulse generators and an IF buffer, has been integrated in a 0.13 µm BiCMOS process. The resistive mixer alone demonstrates a conversion gain as low as $-2.1$ dB and an input referred compression point of $-5$ dBm. For a LO power of $-1.2$ dBm, the overall gain and noise figure are 13.2 dB and 6.3 dB respectively.

## Acknowledgment

This work was supported under the Région Midi-Pyrénées and French state ELECTRA 2010 funded project WIATIC.

## References

[1] B. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. Pister, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, 2006.

[2] M. Camus, B. Butaye, L. Garcia, M. Sie, B. Pellat, and T. Parra, "A 5.4 mW/0.07 mm 2.4 GHz front-end receiver in 90 nm CMOS for IEEE 802.15.4 WPAN standard," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1372–1383, 2008.

[3] A. Mirzaei, H. Darabi, J. Leete, and Y. Chang, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 9, pp. 2353–2366, 2010.

[4] M. Camus, B. Butaye, C. Viallon, L. Garcia, and T. Parra, "A CMOS low loss/high linearity passive mixer for 2.45 GHz low power applications," in *Microwave Conference Proceedings (APMC), 2012 Asia-Pacific*, 2012, pp. 163–165.

[5] X. Zhang, Y. Yin, M. Cao, Z. Sun, L. Fu, Z. Xia, H. Feng, X. Zhang, B. Chi, M. Xu, and Z. Wang, "A 0.1~4GHz receiver and 0.1~6GHz transmitter with reconfigurable 10~100MHz signal bandwidth in 65nm CMOS," in *2012 IEEE Custom Integrated Circuits Conference (CICC)*, 2012, pp. 1–4.

[6] E. Coleman, S. Chakraborty, W. Budziak, T. Blank, and P. Roine, "Process compensated low power LO divider chain with asynchronous odd integer 50% duty cycle CML dividers," in *2011 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2011, pp. 1–4.

[7] E. Lin and W. Ku, "Device considerations and modeling for the design of an InP-based MODFET millimeter-wave resistive mixer with superior conversion efficiency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 8, pp. 1951–1959, 1995.