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# Diagnostic Tools For Accurate Reliability Investigations of GaN Devices

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**Abstract**— Intensive development of GaN-based HEMT devices has been largely pushed by their intrinsic capabilities for operation at high temperature under high voltage conditions, making the difference with the competitive technologies. However, a poor electrical reliability under high-electric-field operation is still hampering large-scale penetration of these technologies into the RF power market. From the early 2000, an increased number of works have addressed reliability issues. The first ones have been conducted on the basis of roadmaps issued from reliability investigations previously carried out on III-V and silicon based devices. These investigations have enlightened that several parameters such as surface passivation, processing techniques alternatives and piezoelectric effects severely impact device reliability. In order to get a deeper understanding of the correlation between physical and electrical events, we simultaneously report low frequency noise (LFN) measurements data (including separation of the different noise sources involved), and electrical measurements data (lag effects on drain and gate terminals, I-DLTS measurements, ...) conducted on the same devices. The later investigations are appropriate in order to identify defects that are able to produce noise. Noise measurements versus temperature on virgin and stressed devices are reported for different GaN processes developed by a French industrial foundry. Lorentzian noise shapes are identified and activation energies are extracted from Arrhenius plots. Additionally, I-DLTS measurements are performed. Electric lag measurements on the gate and drain terminals are finally used in order to relate stress impact to the electrical integrity of the devices. The identification of failure mechanisms needs accurate statements, and the effectiveness of such a melting of different kind of experiments is demonstrated.

**Keywords:** *Low Frequency Noise, Reliability, GaN HEMT devices, I-DLTS and Lag measurements*

## I. INTRODUCTION

Electronic systems are dedicated to different applications used under soft or harsh environment, and the forecast of their lifetime is of prime importance for many applications when reliability is a major issue for the equipment. Different figures such as mean time to failure (MTTF) or mean time between failures (MTBF) are employed for the estimation of the lifetime of an electronic system and for devices. As it is not

possible to assess the lifetime under real conditions of use (involving periods of investigation up to many years!), dedicated experiments are adapted to give an accurate appreciation of their expected lifetime: data issued from many users have shown that the experimental failure rate (given in failures per  $10^6$  hours) can be overestimated or underestimated in comparison with the predicted failure rate, with disagreements up to more than 2 orders of magnitude [1]. The part of the active devices in the overall percentage of failures differs according to the module function: up to 30% of the primary causes of failure are attributed to active components for small power hybrid circuits (10% for power hybrid circuits). If III-V and Si based processes are now mostly stabilized, GaN based large bandgap technologies are still largely investigated to understand the underlying mechanisms inducing degradation at the transistor level. GaN technologies have demonstrated excellent ability for high power applications, high power added efficiency (up to more than 60%), and higher thermal management than its narrow bandgap competitors. From the earlier developments at the end of the 1990-ties, USA and Japan have engaged strong projects on GaN devices development for high power applications (more than 10 W/mm [2], up to 30W/mm [3]), while few years later Europe has followed on a different way considering both power and low noise performances for robust integrated transceivers applications [4][5]. Fig. 1 presents the trend of the transition frequency  $F_t$  versus  $1/L_G$  ( $L_G$  is the gate length) for different GaN technologies.

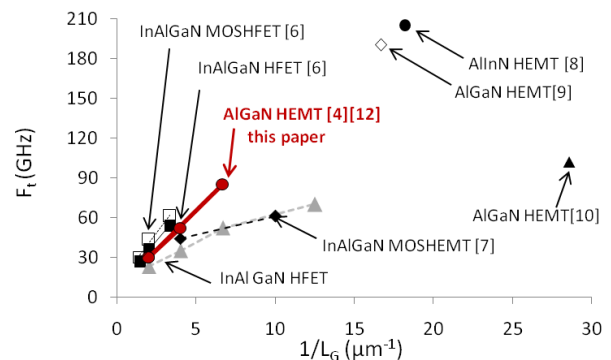


Figure 1. transition frequency versus  $1/L_G$  gate length for different technologies of GaN Field Effect Transistors

Devices have been provided by Sylvain Delage and Benoit Lambert (resp. from Thales III-V Labs and UMS).

As this technology now proposes interesting alternate architectures for defense and commercial applications from few MHz to more than 30 GHz, the associated processes make use of different techniques (passivation, epilayers heights and doping, Al content, Si or SiC substrate,...).

Depending on the application finality (Radar, cellular basestations, and satellite applications soon) these processes are optimized for the best compromise on the power/frequency/cost combination. In such a race against speed and power, GaN have to face a major critical issue concerning the device reliability. Whatever the substrate (SiC, Si, GaN or Al<sub>2</sub>O<sub>3</sub>), the transistors suffer from degradations on the RF output power or I<sub>DS</sub> biasing point under critical stress conditions. The lifetime testing protocol is of prime importance for an effective activation of the first or second order degradation parameters. Moreover, GaN transistors usually experience two kinds of degradations: non-destructive and reversible phenomena affect the transistor performances during the stress or under realistic conditions of use, but the device recovers its original state once the DC or RF signals are removed. A permanent degradation can be observed, related to more severe induced degradations. The decrease observed on I<sub>DS</sub> current versus time is given in Fig. 2 for one of the first developed devices we have studied. The constant of time of the drain current reduction without any accelerated stress (just biasing conditions) is not suitable for characterization over long term period (Low frequency noise measurement takes some 15mn per spectra, High Frequency noise measurement is around 30mn, ...). It can be seen that 3% degradation is attributed to recoverable defects (temporary activated states), whereas 1% reduction on I<sub>DS</sub> concerns definitive modification of the device integrity. Devices from newly developed technologies present similar behaviours over a larger period of time, with variable difference between initial and final I<sub>DS</sub> values (some few percents up to more than 30%).

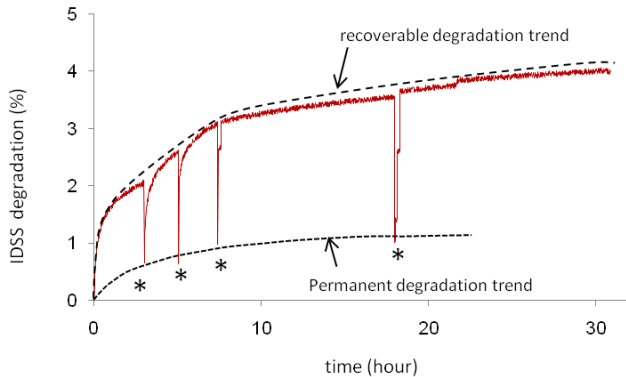


Figure 2. typical real-time degradation signature on I<sub>DS</sub> drain current versus time (devices featuring different gate geometries, biased at V<sub>GS</sub>=0V and V<sub>DS</sub>=10V). Symbol ‘\*’ represents time when the device has been removed from the experimental workbench for specific measurements (I-V, LFN).

First, it is needed to assess that the device does not evolve during the characterization campaign, so that the tracked defects can be effectively extracted. Fig. 3 represents the time and frequency range of the experimental tools, and stress workbenches, as well as the expected activated traps.

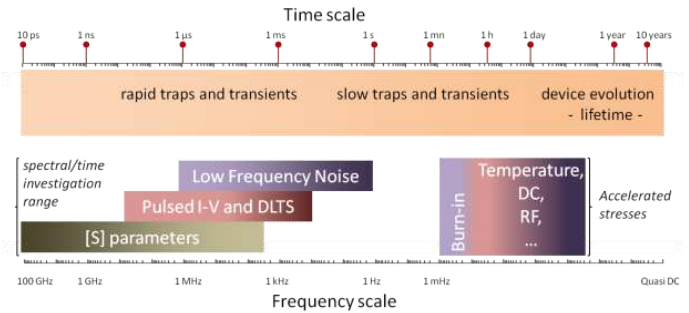


Figure 3. graphic representing the time/frequency staggering for LFN, electrical I-V and [S] parameters (investigation range), and stress induced time range. On the above strip are given the related activated traps. Measurement must be non-invasive vs. stress.

## II. STRESS CONDITIONS

Different life tests ageing have been performed on several GaN technologies:

-Tests S1: 2 batches of 4 samples of HEMTs have been stressed under DC and RF conditions. In the first batch of devices, the biasing has been kept the same, whereas in the second batch devices have been controlled by different gate levels (for I<sub>DS</sub> constant value, Low I<sub>GS</sub> and I<sub>DS</sub> constant, or without feedback). Fig. 4 represents the correlation found between I<sub>DS</sub> and P<sub>out</sub> variations. The inset represents the time dependency of these two parameters, with return measurements spike (device removed from stress workbench for characterizations). Each batch has been stressed for more than 2400 hours.

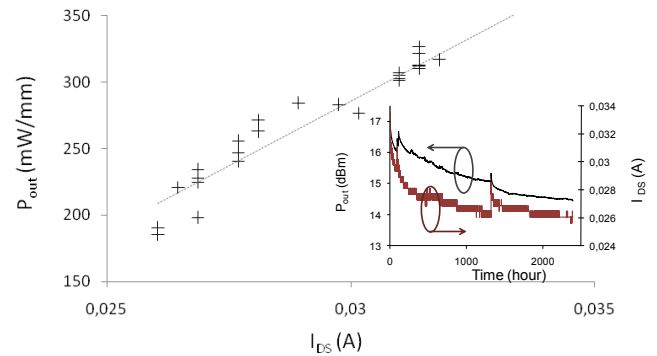


Figure 4. output power P<sub>out</sub> @ 3dB output compression (RF carrier is 10 GHz) versus I<sub>DS</sub> current over a 2400 hours time stress. The inset plots the output power and I<sub>DS</sub> variations versus time (spikes are located when the device has been removed for specific noise and electrical measurements). AlGaIn/GaN HEMT under test has a gate dimension of 0.25x2x75 μm<sup>2</sup>.

-Tests S2: larger periphery devices have been stressed (by manufacturer) HTRB (High Temperature Reverse Bias) over a 2000 hours period. HTRB stress is performed at T°=150°C (HTRB#1) and T°=25°C (HTRB#2) at gate voltage of V<sub>GS</sub>=-7V (drain is biased at 50V).

## III. INVESTIGATION TOOLS

As it is very difficult to establish a general rule of stress life testing conditions (particularly due to an inaccurate knowledge of the thermal resistance [12]), the use of different techniques

of investigation represent the opportunity to cross experiments, and to assess which defect effectively causes the device failure. Experimental workbenches and analytical tools that have been used and developed for these studies are presented next.

### A. Physical simulation

The use of 2D simulations offers a rapid tool of device and associated defects modelling: polarization charges, surface traps in specific regions of the device (mostly between gate and drain) can be calibrated to fit the measurements DC characteristics. We have developed a physical model for AlGaIn/GaN HEMT, and crossed simulations with electrical DC and LFN measurements. From the band diagram in fig. 5, it is possible to evidence the fade-in of a parasitic channel in the lower mobility AlGaIn layer for different biasing conditions [13]. Other studies propose analytical simulations of passivation and charge control effects, thermal effects as well as polarization charges and traps [14]. Sahoo et al. have developed a model where electron leakage between the 2 dimension electron gas (2DEG) to surface states can explain the current slump [15], and Brannick et al. models the thermal behaviour of the electrons using a hydrodynamic model to investigate on the role of the traps [16].

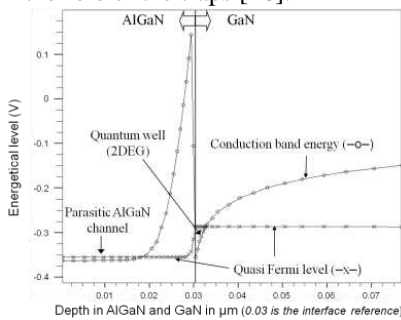


Figure 5. 2D simulation of AlGaIn/GaN HEMT (silvaco with arranged set of thermal and mobility equations)

### B. Experimental Workbenches

**Low frequency noise (LFN) measurements:** LFN sources in solid state devices are associated to crystal impurities ( $1/f^{\alpha}$ ) or trapping/detrapping processes (GR) that can evolve during the application of a stress. Their tracking versus time usually gives an accurate understanding about the evolution of the device during its accelerated lifetime. Different workbenches are available based on multi-impedance method and on transimpedance measurement [17]. An automatic extraction procedure of the noise sources constituting the noise spectra has been developed, and the extraction accuracy is known for each source according to its relative weight in magnitude and frequency (up to 3 GR/decade @  $\pm 4\%$ ) [18].

**Transient I-V measurements:** a dedicated experimental workbench has been developed to discriminate signatures of gate lag from drain lag and self-heating effects [19]. This measurement facility completes LFN tools, by providing information about transient type phenomena. The pulse duration  $\tau$  is chosen as short as possible (0,1  $\mu$ s) to limit self-heating, and the period T between pulses is set to 50 ms. Thereafter,  $V_{\text{quiescent}}$  (resp.  $I_{\text{quiescent}}$ ) represents the voltage (resp.

current) during the T period, while V (resp. I) represents the voltage (resp. current) measured during the duration  $\tau$  of the pulse (cf. Fig. 6 for the measurement of the  $I_{\text{DS}}$  current).

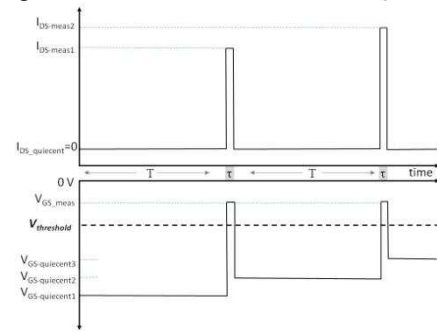


Figure 6. time representation of the pulse, with the quiescent (stand-off) current/voltage between 2 measurements (pulses  $\tau$ ). Here,  $V_{\text{DS}}$  is fixed at  $V_{\text{DS-quiescent}}$  for gate-lag measurements.

**I-DLTS measurements (current Deep Level Transient Spectroscopy)** of a semiconductor material allow the determination of the concentration and section of defects in the bulk material. We have adapted this DLTS workbench for HEMT device characterization. For each stressed and virgin devices, current DLTS plots are measured (Fig. 7, for a stressed device). Measurements are performed over a temperature range between 90 K and 450 K. The Fast Fourier Transform of the I-DLTS signal is used to convert data into the Arrhenius plot: the activation energy and the section of the traps are then extracted for each sample. Hole or electron traps can be discriminated according to the pulse profile.

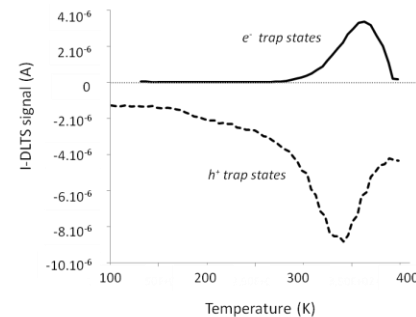


Figure 7. Current Deep Level Transient Spectroscopy for AlGaIn/GaN HEMTs featuring  $e^-$  like trap (virgin device) or  $h^+$  like trap (HTRB#1 stressed device). Device are biased at  $V_{\text{GS}}=-3\text{V}$ ,  $V_{\text{DS}}=3\text{V}$ .  $\Delta R=V/\Delta I$  measurements are performed at  $V=\text{constant}$ .

**[S] parameters and  $P_{\text{1dB}}$  compression point measurements** complete the device characterization with additional information about the small signal gain and non-linear changes before and after the application of the stresses. Aged transistors from tests S1 have their  $P_{\text{1dB}}$  decreased by 2dB to 3dB in comparison with virgin samples (Fig. 8.a). This can be assigned to accumulation of traps between gate and drain and/or gate and source contacts that decreases the respective non-linear capacitances. The transconductance gain  $g_m$  changes before and after the application of the stress when  $V_{\text{GS}}$  varies from pinchoff voltage to 0V (Fig. 8.b). It can be noticed

that the slight increase in gain at  $V_{GS}=0V$  correlates with the higher trend for the stressed device in Fig. 8.a. These results have been qualitatively assessed by electrical simulations on N.L models [20].

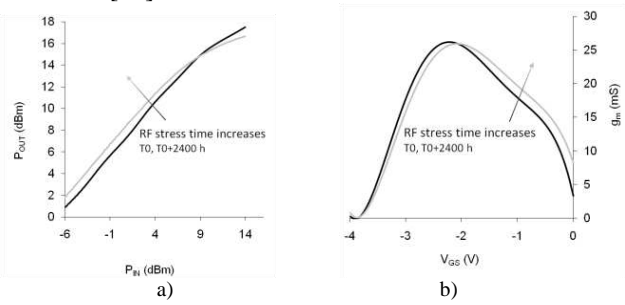


Figure 8. 2400h RF stress effect ( $f_{RF}=10GHz$ , 3dB power compression) on the  $P_{idB}$  (a : meas. at 10 GHz and  $V_{GS}=0V$ ,  $V_{DS}=10V$ ) and on transconductance  $g_m$  (b: at  $V_{DS}=10V$ ). AlGaIn/GaN HEMT under test has a gate dimension of  $0.25 \times 2 \times 75 \mu m^2$ .

#### IV. RESULTS AND DISCUSSIONS

LFN spectra on virgin devices usually feature known relationships versus  $I_D$  ( $S_{ID}$ ) or  $I_G$  ( $S_{IG}$ ) according to the choice of the biasing (excitation of a given noise source). However, when the device is stressed, major changes affect the structural integrity and electrical modeling of the device from its initial to its final state: thus links are not easy to bind electrical or noise signatures between aged and virgin transistors. First results have proved the great impact of the passivation on both the reduction of gate-lag and on the  $S_{IG}$  reduction before and after stress. Different techniques are developed to improve the gate leakage current stability versus stress (passivation ledge, gate deposition techniques, use of MIS gate structures [21], ...).  $S_{ID}$  spectra have been studied at variable  $V_{GS}$  and  $V_{DG}$  constant or  $V_{DS}$  constant so that gate-drain or gate-source induced noise sources can be extracted. Up to 9 GR centers are identified on the spectra from figure 8. Activation energies at 0.21eV and 0.38eV have been previously reported [22], related to defects in the passivation layer between gate and drain, and at the AlGaIn/GaN interface. From the many different stresses from test S2, devices under test feature larger and small gate peripheries ( $8 \times 125 \mu m$  and  $2 \times 175 \mu m$ ).

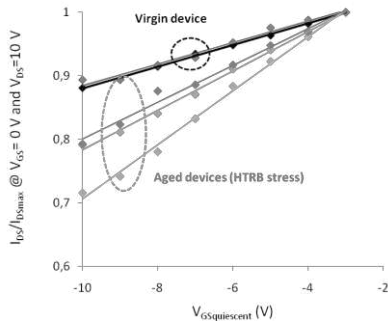


Figure 9. relative gate-lag effect on HTRB-aged and virgin devices measured at  $V_{GS}=0V$  and  $V_{DS}=10V$ .

Batches from test S2 studies reveal that HTRB stress type produces quite similar results on gate-lag and drain lag-effects whatever the temperature of the plate (cf. Fig. 9 and 10 for

gate-lag and drain-lag trends for HTRB#1, at higher plate  $T^\circ$ ). For the two batches, static measurements show 20% average diminution on  $I_{DS}$ , while  $I_{GS}$  increases by more than 3 decades for stressed devices. Buffer traps are usually associated to drain lag measurements, while surface traps can be identified by gate lag measurements: it is clear that both buffer traps and surface states are activated under HTRB stresses.

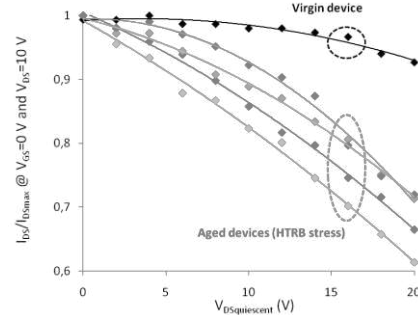


Figure 10. relative drain-lag effect on HTRB-aged and virgin devices measured at  $V_{GS}=0V$  and  $V_{DS}=10V$ .

However, LFN results on  $S_{ID}$  differ from the two HTRB batches: at lower plate temperatures,  $S_{ID}/I_D$  remains at a quite similar level (Fig. 11), even if up to five GR centers are activated by the application of the stress.

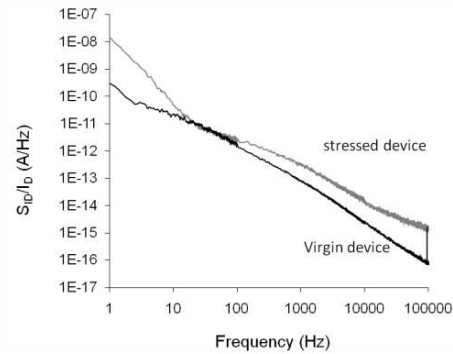


Figure 11. normalized drain current noise spectral density  $S_{ID}/I_D$  for HTRB#2 (lower storage temperature): devices are biased at  $V_{GS}=0V$  and  $V_{DS}=10V$ .

At higher plate temperatures,  $S_{ID}/I_D$  increases largely after the stress period (Fig. 12): it must be noticed that a voltage noise source  $S_V$  representation suits better for interpretation of serial noise contributions between source and drain.

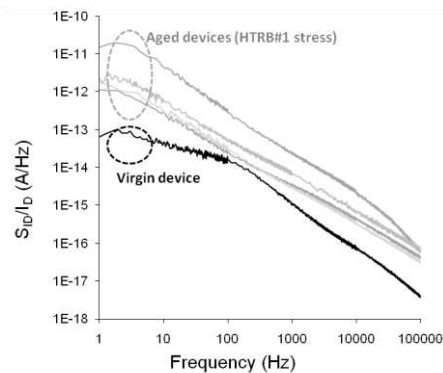


Figure 12. normalized drain current noise spectral density  $S_{ID}/I_D$  for HTRB#1 (high storage temperature): devices are biased at  $V_{GS}=0V$  and  $V_{DS}=10V$ .

However  $S_{ID}/I_D$  gives information about the transconductance gain change ( $g_m$ ), and also reveals stress activated noise sources. These thermally activated GR centers are distributed over the 1Hz-100kHz frequency window. It is clear that the junction temperature is a key parameter in the activation of trap. As previously shown, as the degradation of DC and RF characteristics are associated with large changes in drain leakage currents, the zone close to the gate (surface or depth) plays a strong contribution (high electric field conditions, high temperatures). Degradation can be electrically activated (energy levels), or also due to mechanical strain induced leakage paths. On the gate access, measurements of the gate current noise source  $S_{IG}$  feature a  $1/f^\gamma$  like behavior, with an abnormal low index frequency  $\gamma=0.5$  for batch HTRB#1 (high plate temperature), whereas at lower plate temperature for batch HTRB#2,  $\gamma=0.75$ . It has been previously shown that  $\gamma$  from  $S_{ID}$   $1/f^\gamma$  source is closely bind to transport mechanisms in the channel [13][23]. Concerning  $S_{IG}$ , additional studies have to be performed for an accurate identification of the origin of  $\gamma$  frequency index shifts. Once again, the assumption of continuously distributed traps can be developed. It can be noticed that the correlation between  $S_{ID}$  and  $S_{IG}$  becomes important as observed in [24] when gate leakage currents are elevated. In our study, correlation appears only on stressed devices, as seen in figure 12 on  $S_{IG}$  spectra. At first glance in Fig. 13,  $S_{IG}$  evolves with a close  $I_G^2$  dependency (same trend for devices from test S1).

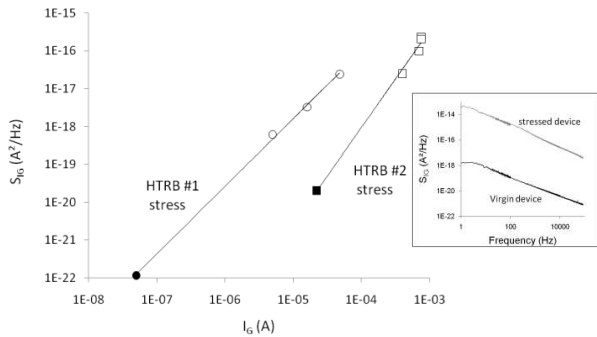


Figure 13. gate current noise spectral density from tests S2, HTRB batches at two different plate temperatures: Temp. HTRB#1 > Temp. HTRB#2 (black symbols represent virgin devices, white symbols are for aged devices, i.e. higher gate leakage currents). LFN measured at  $V_{GS}=-3V$  and  $V_{DS}=10V$ . The inset presents the frequency spectra for aged and virgin devices (HTRB#2).

From I-DLTS measurements, Arrhenius plots are extracted. Virgin devices feature two activation energies at  $E_a=0.57eV$  (trap section of  $\sigma_T=1.3 \cdot 10^{-15} cm^2$ ) and  $E_a=0.7eV$  (trap section of  $\sigma_T=7.5 \cdot 10^{-15} cm^2$ ). Devices from HTRB#2 batch (lower plate temperature) have been measured with an activation energy of  $E_a=0.206eV$  ( $\sigma_T=6 \cdot 10^{-17} cm^2$ ). All these traps are electron trap states. Transistors from HTRB#1 batch (higher plate temperature) feature electron trap states with  $E_a=0.64eV$  (trap section  $\sigma_T=3.7 \cdot 10^{-15} cm^2$ ), and hole trap states with  $E_a=0.3eV$  (trap section of  $\sigma_T=6 \cdot 10^{-20} cm^2$ ). Electron trap states and hole trap states can probably be associated to interface states at the surface near the gate, and possibly in the AlGaIn bulk. Polarization of the AlGaIn material induces pairs of

electrons and holes on opposite surfaces as shown in Fig. 14. The removal of a hole (resp. electron) is balanced by the disappearance of an electron (resp. hole) on the opposite side. During the high dynamic RF signal stress (test S1), or high thermal reverse DC bias stress (test S2), mobile surface or interface charges are generated between drain and source at the interface between 2DEG and AlGaIn layer, and also between the AlGaIn and the passivation layers. This occurs when the applied electric field (RF and/or DC) exceeds the barrier height  $E_G$  of the AlGaIn layer. The so-called current collapse seen in Fig. 2 and Fig. 4 is associated to a drastic increase in gate leakage current and a reduction in drain current. Mobile holes or electrons from part of the interfaces can be collected at the drain access, by surface leakage or tunnelling mechanisms [25][26][27], and  $I_D$  decreases under a more negative gate effective voltage  $V_{DG-eff}$  in the active zone.

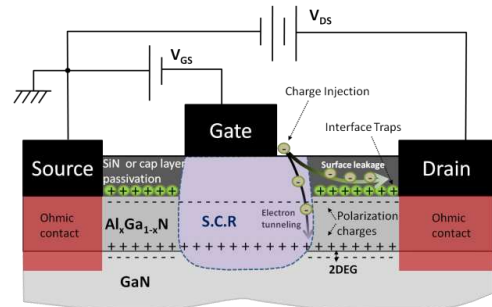


Figure 14. schematic representation of the surface traps and bulk traps location. Gate leakage current can tunnel from the gate to the 2DEG channel when critical energy is brought to electrons to overcome the barrier height.

Moreover, the shift in pinchoff voltage and transconductance  $g_m$  change before and after stress can be attributed to gate and epilayer interfacial zone modifications: gate metal interdiffusion could be the root cause of the device degradation [28]. From LFN measurements, the numerous GR centers constituting the spectra essentially noticeable on aged devices under high thermal storage conditions suggest the presence of broad range distributed traps. These traps are activated by tunnelling process, but also thermally activated traps. Studies on thermal activation of traps versus temperature are still ongoing. Storage of devices under only thermal conditions (more than  $300^\circ C$ ) have demonstrated no electrical or noise change. Lag effects on the gate (rep. drain) confirm the modification of the surface states (resp. bulk). These effects are not permanent and can be recovered after a time of inactivity, but the device rapidly returns to its last state: this confirms that holes and electrons traps are still active after the removal of the stress conditions.

## V. CONCLUSION

Storage of biased AlGaIn/GaN HEMT under high temperature and/or RF signal stands as a harsh stress that affects the transistor performances through a decrease of its drain current and of its output power. This behavior of the transistor is clearly evidenced by gate current increase, and also by mean of low frequency noise measurements, transient lag and I-DLTS characterizations. It has been shown that high thermal reverse bias stress accelerates the degradation process

all the more since temperature increases. Activation energies have been found at  $E_a = 0.206\text{eV}$  and  $E_a = 0.64\text{eV}$  for electron trap states, and hole trap states with  $E_a = 0.3\text{eV}$ . Traps are located at the vicinity of the gate, expected between gate and drain where the electric field is elevated. Surface states (resp. buffer traps) are evidenced by gate (resp. drain) lag measurements. Low frequency noise measurements reveal numerous GR centers after the application of the stress. These centers have a greater impact on LFN signatures on drain and gate current noise sources when the temperature increases. However, the associated parameter still concerns high  $V_{DG}$  (static or dynamic) stresses, as no degradation has been found on devices stored under high temperature conditions (no DC bias). Studies are still on going to understand the underlying phenomena corresponding to the conduction mechanisms of the gate, and to propose alternate solutions. Moreover, the high electric field and mechanical strains under the gate can be the origin of another mechanical stress in the AlGaN crystal. This defect can create a sudden and fatal conduction path from the gate to the channel, already seen on electric measurement at high  $V_{DG}$  voltage. The field of investigations on failure analysis for GaN based devices is now strongly reinforced with multiphysics programs in Japan, USA and Europe, making use of opto-electrical measurements for non-destructive techniques, FIB and TEM methods for in-situ visualization of defects. This represents a new challenge and a wonderful opportunity to deploy new reliability methods and tools for a 'reliable' expertise on wide bandgap technologies.

#### ACKNOWLEDGMENT

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