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Stable microcrystalline silicon thin-film transistors produced by the layer-by-layer technique

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Microcrystalline silicon thin films prepared by the layer-by-layer technique in a standard radio-frequency glow discharge reactor were used as the active layer of top-gate thin-film transistors (TFTs). Crystalline fractions above 90% were achieved for silicon films as thin as 40 nm and resulted in TFTs with smaller threshold voltages than amorphous silicon TFTs, but similar field effect mobilities of around 0.6 $cm^2/V\,s$. The most striking property of these microcrystalline silicon transistors was their high electrical stability when submitted to bias-stress tests. We suggest that the excellent stability of these TFTs, prepared in a conventional plasma reactor, is due to the stability of the μc-Si:H films. These TFTs can be used in applications that require high stability for which a-Si:H TFTs cannot be used, such as multiplexed row and column drivers in flat-panel display applications, and active matrix addressing of polymer light-emitting diodes. © *1999 American Institute of Physics.* [S0021-8979(99)05324-4]

I. INTRODUCTION

Active matrix liquid crystal displays (LCD) in which each pixel is addressed by an a-Si:H based thin-film transistor (TFT) are the base of a mature industry,[1,2] in spite of hydrogenated amorphous silicon (a-Si:H) TFTs having low mobility and poor threshold voltage stability. This can be due to the metastability of a-Si:H films or to a carrier trapping in the insulator.[3,4] Polycrystalline silicon films produced by thermal or laser annealing of a-Si:H have resulted in highly stable thin-film transistors with mobilities above 100 $cm^2/V\,s$,[5,6] that can be used for both multiplexing the LCD and making drive circuits. However, thermal annealing requires quartz substrates and is not suitable for large area displays. Laser annealed polycrystalline silicon TFTs require complex processing, and there remain problems with the stability and large area uniformity of the laser annealing process. For manufacturing, it would be more attractive if displays incorporating integrated drive circuits could be made by the simpler a-Si:H TFT fabrication process, but with some process steps modified to give superior devices.[5] The highest level of driver circuit intergration, which requires the lowest number of interconnects and external drivers, requires high stability and high mobility TFTs. However, multiplexed row and column drivers, which reduce the number of interconnects, can still be made with low mobility TFTs.[7,8] The high duty ratio (ON time/OFF time) of some of the transistors in drive circuits means that high mobility TFTs with the poor stability of a-Si:H TFTs would result in drive circuits with an unacceptably short lifetime. In addition, TFTs for active matrix addressing of organic and polymer light-emitting diodes (LEDs) must also have high stability. For this reason, we have investigated the properties of TFTs made by a standard a-Si:H top-gate TFT process, but with the a-Si:H layer replaced by microcrystalline (μc-Si:H) films directly deposited by plasma enhanced chemical vapor deposition (PECVD) at low temperature, with particular emphasis being placed on device stability.

Compared to a-Si:H, μc-Si:H films should result in thin-film transistors with higher field effect mobility and improved stability. Indeed, microcrystalline silicon (μc-Si:H) thin films produced at low temperatures by PECVD have been largely studied for their application to thin-film transistors.[9–11] However, very few publications report on μc-Si TFT mobilities higher than those of a-Si:H TFTs.[12,13] In most cases, the mobility is smaller, and no information is provided on the stability of the devices. Although the smaller grain size in μc-Si:H films produced by PECVD, with respect to laser crystallized ones, can partly explain the smaller mobility, other factors like grain boundary passivation and the quality of the crystallites in the channel region may have more of an effect on the field effect mobility. The production[14] of μc-Si:H films from SiF_4 precursors with mobilities above 30 $cm^2/V\,s$ and thin-film transistors[12] with mobilities up to 40 $cm^2/V\,s$ confirms that low temperature deposited μc-Si:H films are a serious alternative to higher temperature processes such as solid phase crystallization and laser annealing. Moreover, it has been shown that μc-Si:H films with crystalline fractions above 60% are stable[15] and that they result in stable solar cells.[16]

Here we report on the production of stable μc-Si:H TFTs in a standard radio-frequency glow discharge reactor.

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II. EXPERIMENTS

Top-gate transistors were prepared as follows. Indium tin oxyde (ITO) on glass was patterned to form source and drain contacts. In a multichamber PECVD system, the substrates were exposed to a PH_3 plasma, followed by the deposition of a 20-nm-thick *a*-Si:H layer. It has been shown that this forms doped *a*-Si:H layers in contact with the ITO.[17] After an HF dip to remove the native oxide, the substrates were loaded into a multiplasma-monochamber reactor[18] for the deposition of the μc-Si:H layer and a 80-nm-thick *a*-SiN:H layer at 250 °C. Silicon nitride films were produced at 40 Pa from the decomposition of a gas mixture consisting of 2 sccm of silane, 100 sccm of NH_3, and 100 sccm of hydrogen under an rf power of 60 mW/cm^2 resulting in a deposition rate of 1 Å/s and a material with an optical gap E_{o4} of 5.5 eV. In some cases, SiO_2 films deposited at 250 °C in a IDECR reactor[19] were used as an alternative dielectric layer.

Microcrystalline silicon films were produced by the layer-by-layer technique,[20] in which the deposition of a thin *a*-Si:H film is followed by its exposure to an hydrogen plasma, and this sequence is repeated until the desired thickness is achieved. The deposition and hydrogen exposure times were fixed at 20 and 30 s, respectively. Because of the hydrogen plasma treatment, the porosity of the *a*-Si:H film increases during the first LBL cycles. In subsequent silane/hydrogen cycles, the nucleation of crystallites takes place; the crystalline fraction increases while the amorphous phase and porosity decrease until a steady state growth is reached. After this the crystalline fraction remains constant[21] but the transport properties improve with film thickness.[14] The *a*-Si:H deposition was carried out from a 50% silane in hydrogen mixture at 10 mW/cm^2, whereas the hydrogen plasma exposure was performed at 100 mW/cm^2. The process pressure was kept constant at 40 Pa. Under these conditions, the effective deposition rate was 0.15 Å/s. This deposition rate can be increased up to 1 Å/s by an appropriate choice of the plasma conditions.[22] In principle, all of the plasma processes could have been carried out in a single PECVD system, but at the moment, we have different processes optimized in different deposition systems.

After μc-Si:H and *a*-SiN:H or SiO_2 deposition, the samples were processed into standard top-gate TFT structures, which included a second *a*-SiN:H deposition to make a total gate dielectric thickness of 330 nm.

Top-gate TFTs were chosen in preference to bottom-gate TFTs because the channel is formed on top of the microcrystalline silicon where the growth process has stabilized, rather than at the bottom surface where the nucleation takes place. We expect the top surface to have better material properties and to be more reproducible. The TFT measurements reported here were made on long channel TFTs ($w = 1000\,\mu$m and $L = 100\,\mu$m), to avoid contact limitations. Annealing the TFTs for 1 h at 200 °C resulted in a 10%–20% increase of their mobility, and a decrease of their threshold voltage. The transfer characteristics were measured at 30 °C on annealed TFTs with source-drain voltages of 0.25 V (linear regime) and 20 V (saturation regime). Stress tests were performed under a gate voltage of 30 V and a substrate temperature of 60 °C.

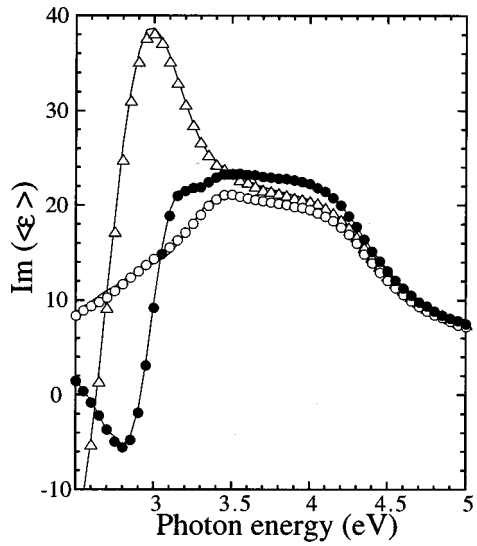

FIG. 1. Spectroscopic ellipsometry measurements performed on (i) a μc-Si:H film obtained after 80 LBL cycles on a Corning glass (full circles); (ii) the same film deposited on a crystalline silicon substrate coated with 50-nm-thick *a*-Si:H film (open circles); and (iii) a μc-Si:H film obtained after 60 LBL cycles on a Corning glass (open triangles). The three films were produced at 250 °C.

III. RESULTS AND DISCUSSION

Figure 1 shows the result of spectroscopic ellipsometry measurements performed on samples codeposited with the TFT structures, without the *a*-SiN:H layer. Full circles represent the imaginary part of the pseudo-dielectric function ($\langle \epsilon_2 \rangle$) of a μc-Si:H film obtained after 80 LBL cycles directly on Corning glass (Cg), while open circles show the spectrum of a film deposited in the same run but on a crystalline silicon substrate coated with 50-nm-thick *a*-Si:H layer, in order to reproduce the conditions used for the TFTs fabrication. Apart from the differences in the low energy part of the spectra (interference fringes with different substrates), one can see that the amplitude of Im($\langle \epsilon_2 \rangle$) of the μc-Si:H film deposited on *a*-Si:H is smaller than that of the film directly deposited on glass. Indeed, the growth of μc-Si:H on *a*-Si:H strongly depends on the quality of the *a*-Si:H layer[23] and may result in μc-Si:H films with higher surface roughness. The analysis of the spectra presented in Fig. 1, with Bruggeman effective medium approximation,[21] shows

TABLE I. Thickness and composition of the microcrystalline silicon films deduced from the analysis of the spectroscopic data shown in Fig. 1. *N* is the number of cycles used in the deposition of the μc-Si:H layer, *d* the layer thickness, F_c the crystalline fraction and F_a the amorphous fraction. The complement to 100% corresponds to the fraction of voids.

		Surface roughness			Bulk		
Sample	*N*	*d*(Å)	F_c(%)	F_a(%)	*d*(Å)	F_c(%)	F_a(%)
EP20/Cg	80	36	48	8	564	87	6
EP20/*a*-Si:H	80	82	46	20	413	98	0
EP16/Cg	60	53	49	13	208	86	11

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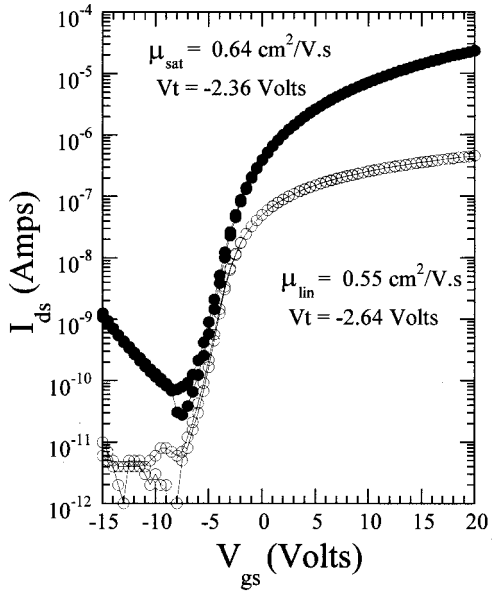

FIG. 2. Transfer characteristics of a μc-Si:H TFT measured in the linear regime (V_{DS}=0.25 V) and in the saturated regime (V_{DS}=20). The threshold voltage and effective field effect mobility are also shown.

that the surface layer is more amorphous in the case of deposition on a-Si:H (see Table I). The higher amorphous fraction and roughness of the film in the channel region of the TFT can be of crucial importance for the TFT characteristics. In the case of the film on glass after 60 cycles (open triangles), we obtain a higher void fraction in the bulk and the higher amorphous fraction in the surface layer region, as expected in a film for which a steady-state growth has not been achieved. Then, TFTs produced at $N=60$ have μc-Si:H films deposited during the evolutionary phase of LBL growth, where the film porosity decreases and its crystalline fraction increases, and $N=80$ corresponds to the steady-state growth with maximum crystalline fraction.[20]

Figure 2 shows the transfer characteristics of top-gate TFT EP20 measured with a gate voltage swept from -15 to $+20$ V. In the linear regime, the source-drain voltage was 0.25 V, and 20 V in the saturated regime. The values of the field effect mobility and threshold voltage in each regime are also shown in the figure. Despite the high crystalline fractions (see Table I), mobility values are typical of a-Si:H TFTs. However, the threshold voltage and the OFF current

TABLE II. Summary of the microcrystalline TFT characteristics. The mobility and threshold voltage are those measured in the saturated regime. The leakage current was measured under a gate voltage of -15 V and a source-to-drain voltage of 20 V. ΔV_T is the shift in the threshold voltage measured after 1000 s stress with a gate voltage of 30 V and a substrate temperature of 60 °C. The I_{ON}/I_{OFF} ratio has been measured at $+15/-15$ V and a source-to-drain voltage of 0.25 V. Only EP20 has SiO_2 as a dielectric layer.

Sample	N	μ (cm²/V s)	V_T (V)	I_{OFF} (A)	I_{ON}/I_{OFF}	ΔV_T (V)
EP6	80	0.60	−0.4	9.10^{-8}	4.10^{4}	0.64
EP21	80	0.54	−1.2	2.10^{-9}	1.10^{4}	0.62
EP17	60	0.49	1.3	3.10^{-9}	3.10^{4}	0.87
EP20	80	0.64	−2.4	1.10^{-9}	5.10^{4}	−0.18

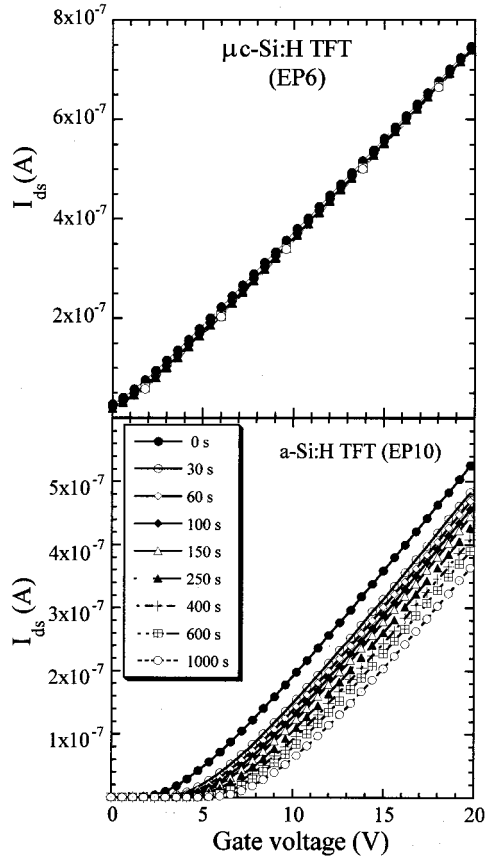

FIG. 3. Linear transfer characteristics taken during threshold voltage shift measurements on a μc-Si:H TFT (EP6) and on a standard a-Si:H TFT (EP10).

are respectively smaller and higher than those of a-Si:H TFTs, as expected for μc-Si:H TFTs. Table II summarizes some properties of μc-Si:H TFTs. EP6 and EP21 where nominally made with the same process, but produced and measured at a six month interval. We can see that there is a good reproducibility of the characteristics, which is further supported by the stability tests. We attribute the factor of 50 lower value of the OFF current in sample EP21 to a better process in the formation of the ohmic contact between the ITO source/drain contacts and the a-Si:H layer. TFT EP17, with a thinner μc-Si:H layer ($N=60$ as for EP16) had a somewhat lower field effect mobility and higher threshold voltage, suggesting a less crystallized channel region, in agreement with the spectroscopic ellipsometry results (Table I). Finally, sample EP20, with a SiO_2 dielectric layer shows mobility and OFF-current values comparable to those of TFT EP21 deposited under the same conditions, but with a-SiN:H as the dielectric layer. However, the negative threshold voltage shift of only 0.18 V indicates that SiO_2 gives more stable results than a-SiN:H. Let us now focus on the stability of these μc-Si:H TFTs.

Figure 3 shows the linear transfer characteristics taken during threshold voltage shift measurements on a μc-Si:H (EP6) and a standard a-Si:H (EP10) top-gate TFTs. The characteristics are recorded at different stressing times (0, 30, 60, 100, 150, 250, 400, 600, and 1000 s). Compared to the standard a-Si:H TFTs, the stability of the μc-Si:H TFT is

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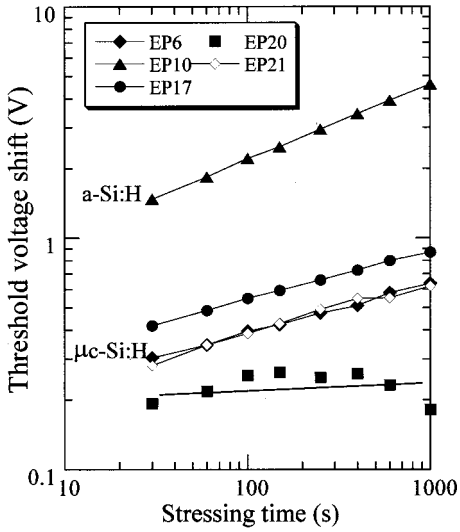

FIG. 4. Threshold voltage shifts as functions of stressing time at 60 °C under a gate voltage of 30 V. Note the small shift for the μc-Si:H TFTs, especially when compared to the a-Si:H TFT and the excellent stability of TFT EP20 in which SiO_2 was used as a gate dielectric. The lines are provided as guides to the eye.

remarkable and comparable to that of a-Si:H TFT prepared by hot wire chemical vapor deposition.[24] The stability of these μc-Si:H TFTs is also demonstrated in Fig. 4, where we plot the threshold voltage shift as a function of the stressing time for four μc-Si:H TFTs and a standard a-Si:H TFT of comparable mobility. Clearly, all μc-Si:H TFTs show smaller threshold voltage shifts than the a-Si:H TFT. One can notice again the excellent reproducibility of the results (EP6 versus EP21) and a slightly higher shift for the TFT with the thinner and less crystallized surface layer (EP17). Finally, TFT EP20 with SiO_2 as a dielectric layer shows almost no threshold voltage shift.

We attribute the stability of these μc-Si:H TFTs to the high crystalline fraction achieved in the layer-by-layer technique even for very thin μc-Si:H layers. Indeed, stability studies performed on μc-Si:H layers have shown that films with crystalline fractions above 60% are stable.[15] All of the microcrystalline TFTs had much better stability than amorphous silicon TFTs, such as EP10. Also samples EP6 and EP21 had a higher crystalline fraction than EP17 (Table I), and they also had a better V_T stability. These results indicate that the stability of μc-Si:H films is the main reason for the stable TFTs. Nevertheless, the improved stability for TFT EP20 with an SiO_2 dielectric layer suggests that the insulator does have a secondary effect.

IV. CONCLUSIONS

As a conclusion, we have shown that stable microcrystalline silicon thin-film transistors with mobilities similar to those of a-Si:H TFTs can be produced by the standard rf glow discharge technique. While further work is necessary to increase their field effect mobility, the remarkable stability of these transistors will favor their use as driver circuits directly incorporated onto flat-panel displays, and other applications that require high stability devices.

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