Efficient dynamic configuration of a multi-ASIP turbo decoder

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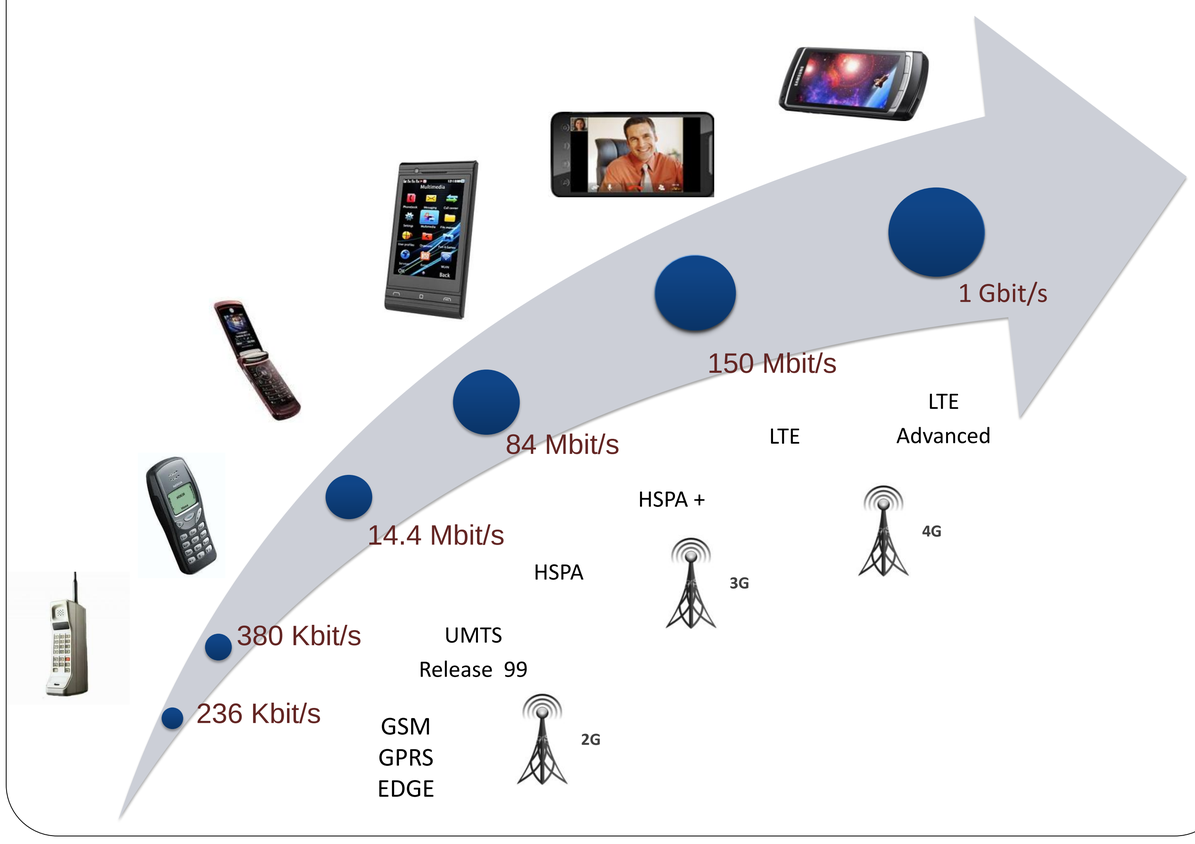
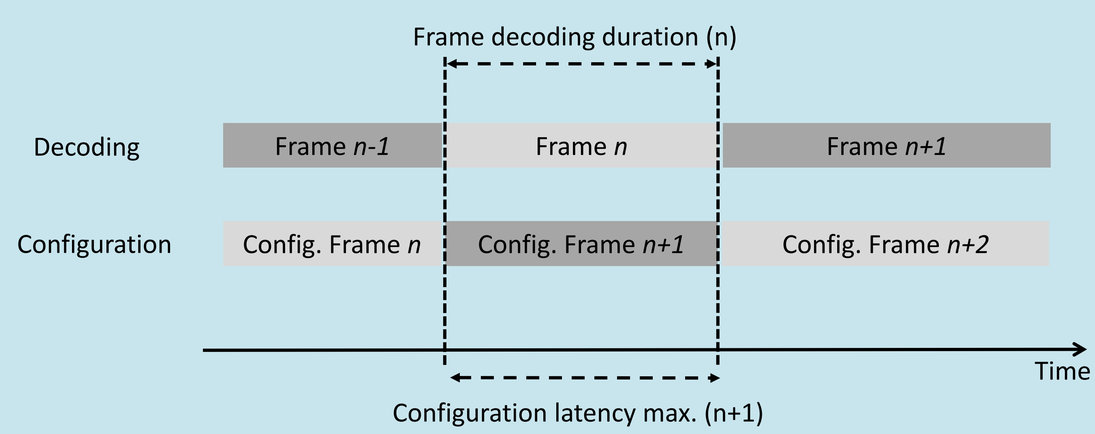
Throughput evolution in telecommunication standards



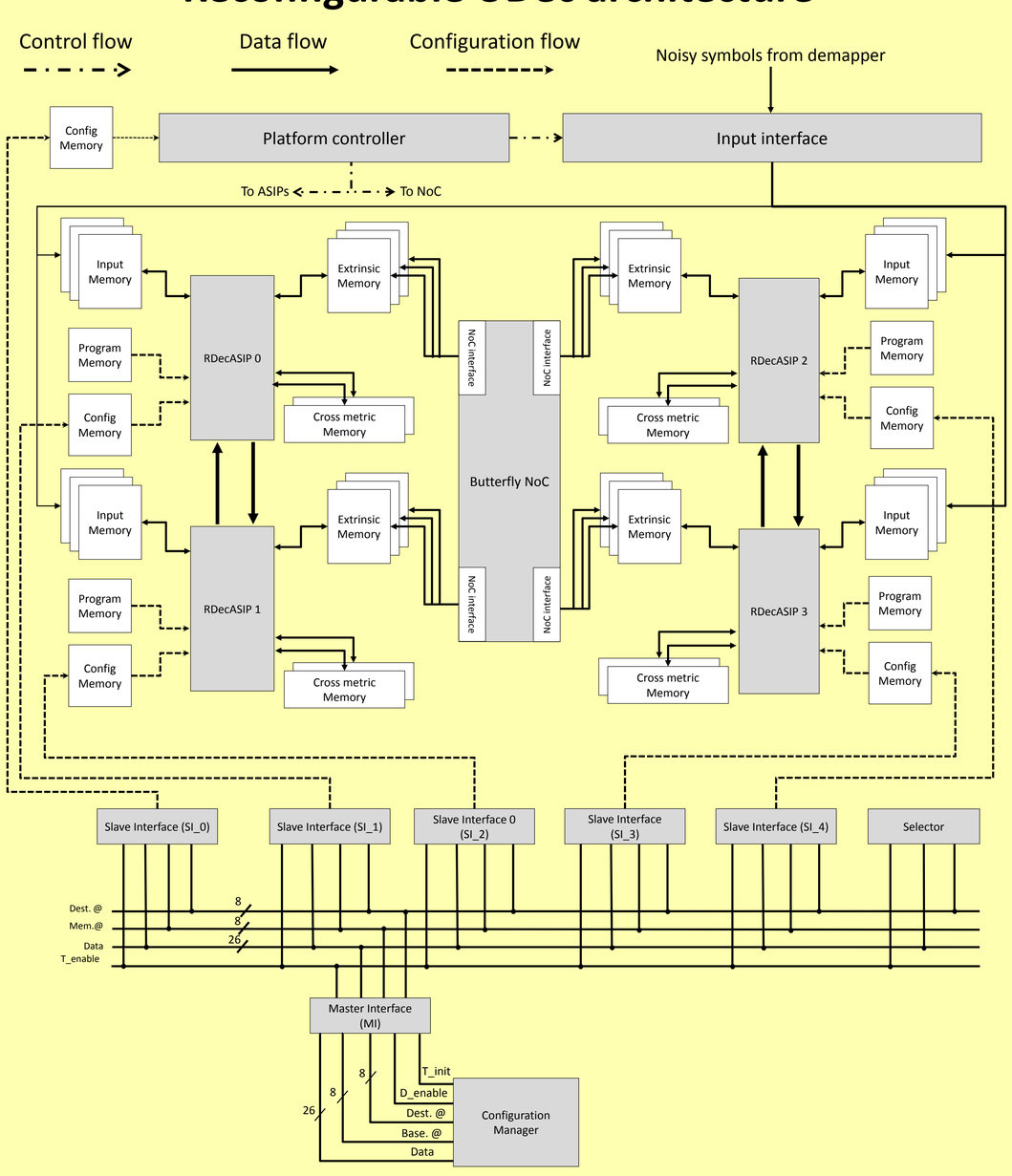
Configuration scenario



- Each frame can require a specific configuration.
- A new configuration is generated and loaded during the decoding of the current frame.

Due to high throughput, the frame decoding duration decreases.
Thus, the maximal configuration latency critically decreases too
Reconfiguration in few µs becomes mandatory

Reconfigurable UDec architecture



RDecASIP

- SBTC and DBTC
- Max-Log MAP algorithm
- 12 Windows of 64 symbols

Optimized for high speed configuration

- Generic Program for turbo decoding
- Multi configuration storage
- 1 cycle re-initialization (for the same configuration parameters)
- Smart memory organization
  - ➢ Unicast, multicast and broadcast for low latency configuration transfer

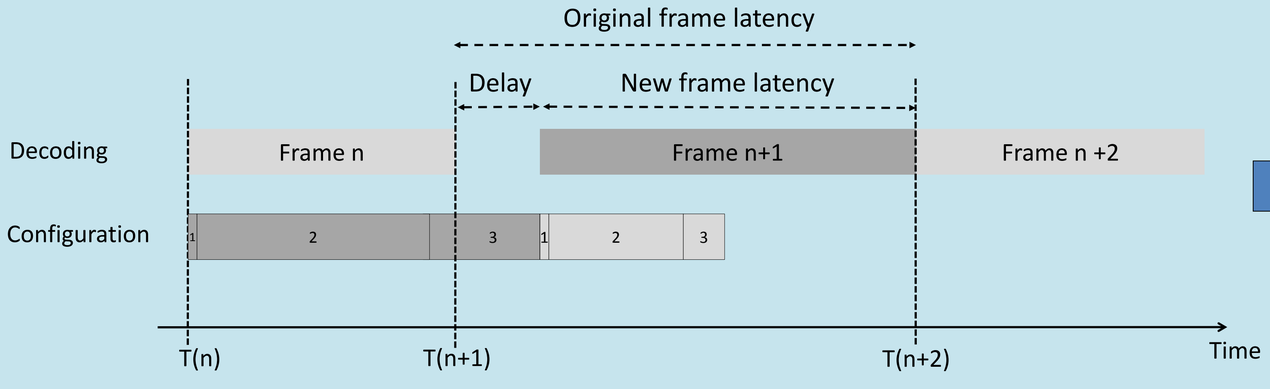
Configuration infrastructure

- Bus-based pipelined interconnect structure
- Unicast, multicast and broadcast mechanisms
- Incremental burst transfer

Configuration transfer latency (FPGA prototype, 125 MHz)

Nb. ASIPs	Transfer latency (in ns)			Speedup	
	This work	CoreConnect PLB 4	AMBA AXI 4	vs. CoreConnect PLB 4	vs. AMBA AXI 4
4	1 032	3 872	2 212	3.75	2.14
6	1 176	5 808	3 168	4.94	2.69
8	1 320	7 744	4 224	5.87	3.2
16	1 896	15 488	8 448	8.17	4.45
32	3 048	30 976	16 896	10.16	5.54
64	5 352	61 952	33 792	11.57	6.31

Configuration management for very low frame decoding duration



1 Configuration manager reads new frame parameters ; 2 configuration generation ; 3 Configuration transfer

Configuration research