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# High temperature, Smart Power Module for aircraft actuators

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## ABSTRACT

More electric aircraft require converters that can operate over a wide temperature range (-55 to more than 200°C). Silicon carbide JFETs can satisfy these requirements, but there is a need for suitable peripheral components (gate drivers, passives. . .). In this paper, we present a “smart power module” based on SiC JFETs and dedicated integrated gate driver circuits. The design is detailed, and some electrical results are given, showing proper operation of the module up to 200°C.

## Keywords

Power electronics; SiC; SOI; Power module.

## 1 Introduction

The aircraft are currently designed around a so-called “more electrical” architecture, in which most of the classical hydraulic and pneumatic actuators are replaced by electrical systems. This results in an increase in the total electrical power consumption (more than 1 MW for a Boeing 787). A new standard in power distribution, that increases the electrical network from 270 to 540 V has then been defined to transfer more power and to keep the weight of the wiring within acceptable limits.

Power electronics converters are required to control the electrical actuators. It is desirable to place these converters as close as possible to the actuators they drive : this reduces electro-magnetic emissions (EMI), wiring, and mechanical complexity. A consequence is that the converters are exposed to the same environment as the actuators. In particular, for jet engine or brake applications, the power electronic systems must sustain ambient temperatures ranging from -55 to 200°C.

Several converter, designed for high temperature operation, have been presented in recent years [1]. In the extreme environments, such as in [2] (450°C), only the power devices are submitted high temperature, the rest of the circuit (some passives, the gate drivers, etc.) being kept at a milder ambient. More recently, a power module integrating the power devices (SiC MOSFETs) as well as their gate drivers was presented in [3]. It is designed to withstand continuous operation at 250°C.

In this paper, we present a “half bridge” power module designed to operate over a wide temperature range, on a 540 V DC bus. This power module non only includes power semiconductors (SiC JFETs), but also the corresponding driver circuits (custom-designed SOI ASICs) and their associated discrete components. The technologies were chosen carefully to achieve high temperature capability.

In the first section of the article, we present the chosen power devices. The second part is dedicated to the description of our custom-designed gate driver ASIC. The hardware (power module and test bench) will be shown in the third section, and the electrical results in the fourth.

## 2 Power devices

Operation at high temperature (> 200°C ambient) and high voltage (540 V in the case of a “HVDC” aeronautic network) exceeds the capability of silicon power devices [4]. In such conditions, power devices based on wide-bandgap materials are required. Silicon Carbide offers the most advanced manufacturing technology, with many transistor structures available (MOSFET, JFET, BJT, . . .). Among these devices, the JFET is attractive for high temperature applications, because of the absence of gate oxide (which causes reliability concerns at high temperature [5]), and because being a FET device, it only require a very low quiescent current.

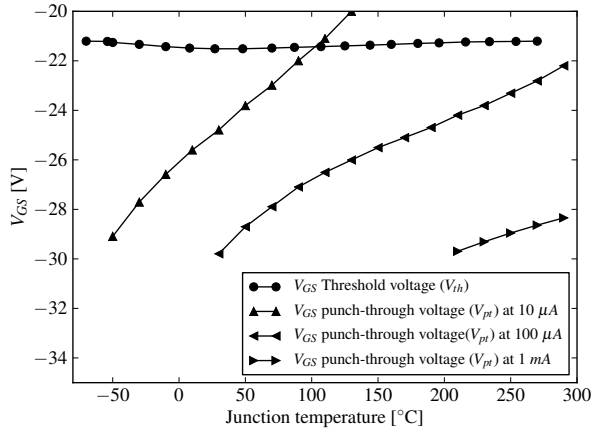


Figure 1: Gate characteristic of the  $4.08 \times 4.08 \text{ mm}^2$  SiC JFET die (SiCED). To properly block the JFET, the gate-to-source voltage must be lower than  $V_{th}$  and higher than  $V_{pt}$ .

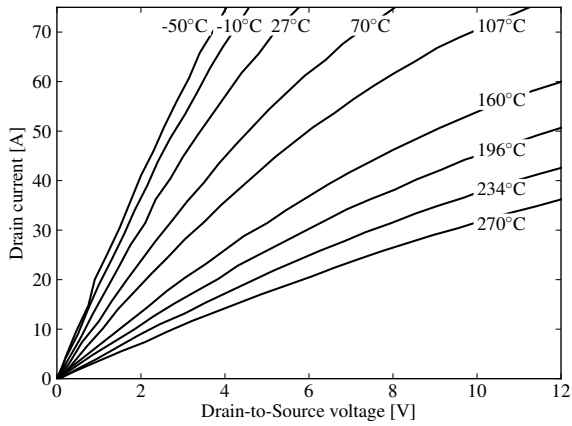


Figure 2: On-state ( $V_{gs} = 0V$ ) characteristic of the JFET, for ambient temperatures ranging from  $-50$  to  $270^\circ\text{C}$ .

Furthermore, some JFET structure provide an anti-parallel “body diode”, which can be used in inverter commutation cells. This is the case with the JFETs manufactured by SiCED (and now by Infineon), which were chosen for the present study. The main drawback of these components is their “normally-on” behaviour: if no (negative) voltage bias is applied between gate and source, the JFET is in the on-state. Some precautions must therefore be taken to ensure safe failure modes (e.g. the loss of the drivers power supply shouldn’t result in a short circuit on the power circuit).

The devices selected for the power module are  $4.08 \times 4.08 \text{ mm}^2$  SiC JFET dies from SiCED. They are rated at 1200 V, and have a  $R_{DS(on)}$  value (measured) of  $60 \text{ m}\Omega$  at  $25^\circ\text{C}$ . These devices were characterized using a specific test setup (offering high temperature capability and 4-points measurements) described in [6]. Some results are presented in figures 1 and 2.

In figure 1, we extracted the threshold voltage and the punch-through voltage of the JFET from their static I(V) characteristic. As can be seen, the threshold voltage is

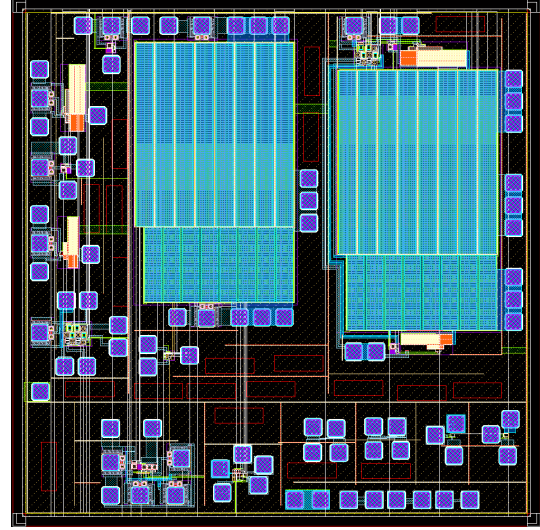


Figure 3: SOI Driver layout. The two large rectangles are the output transistors. Total die size is  $3 \times 3 \text{ mm}^2$ .

fairly stable from  $-70$  to  $+270^\circ\text{C}$ , at  $-21.5 \text{ V}$ . The punch-through voltage (i.e. the breakdown voltage of the gate-to-source junction), however, is much more variable with the temperature. It must be stressed that the definition of the punch-through voltage is somehow arbitrary, as it depends on the quiescent current allowed through the gate. For the JFET under study, if the gate driver can supply a quiescent current of  $1 \text{ mA}$ ,  $V_{pt}$  remains lower than  $-28 \text{ V}$  up to  $290^\circ\text{C}$ . This means that this device can be blocked with for  $-21.5 > V_{gs} > -28 \text{ V}$  over the complete temperature range, from  $-70$  up to  $290^\circ\text{C}$ .

In the on-state (for  $V_{gs} = 0 \text{ V}$ ), the I(V) characteristic is plotted in figure 2, for ambient temperatures ranging from  $-50^\circ\text{C}$  to  $270^\circ\text{C}$ . As the electrical resistivity of SiC increases with temperature, so does the  $R_{DS(on)}$  of the transistor, resulting in higher drain-to-source voltage ( $V_{ds}$ ) at a given drain current level, and therefore in higher conduction losses. In our case, with a maximum ambient temperature of  $200^\circ\text{C}$  (and therefore a higher junction temperature), the maximum drain current of the JFET should not exceed 8 to 10 A to avoid excessive power dissipation in the on-state.

### 3 Design of the ASIC driver

As described in the previous section, the selected SiC JFETs require driving signals that are fairly different from those of the classical Si MOSFETs or IGBTs. Furthermore, most standard driver circuits are designed for a maximum junction temperature of  $150$  to  $175^\circ\text{C}$  only [7]. For operation of SiC JFETs over an extended temperature range, a dedicated driver circuit is therefore required.

Silicon On Insulator (SOI) is commonly used as the base material for integrated gate driver circuits [8], as each transistor of the integrated circuit can be isolated from the other using a silicon oxide layer. This is

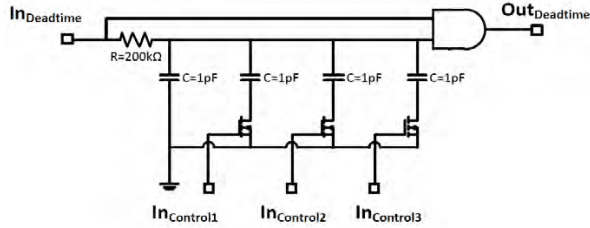


Figure 4: To avoid cross-conduction of its output stage, the gate driver is equipped with a dead-time circuit. The delay can be adjusted for various operating conditions.

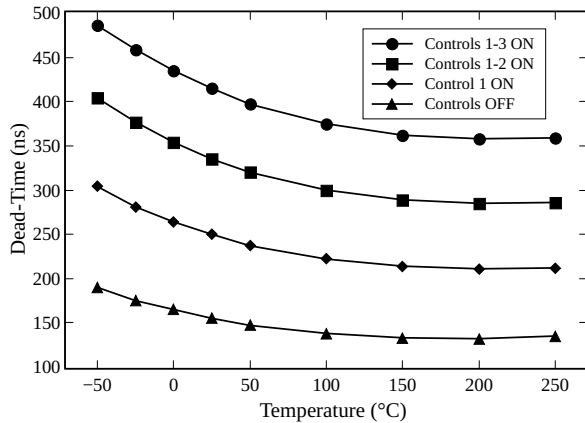


Figure 5: Dead-time delay measurements, using various configurations of the dead-time generation circuit (see figure 4).

especially valuable for high temperature operation, as the leakage current in bulk silicon become prohibitively large as the temperature increases.

The circuit presented in this article is based on an industrial SOI technology, Smartis-1 (Smart-power Integrated Systems), manufactured by ATMEL. It is an  $0.8 \mu\text{m}$  Bipolar-CMOS (BCD) technology, made on a partially-depleted SOI wafer, with 3 AlSiCu metal layers and Ti/AlSiCu/TiN interconnects that offer good resistance to electromigration.

A gate driver usually has several functions:

- the output stage, that is connected to the gate of the power device. It must be fast and capable of delivering current levels in the order of 1 A or more;
- the level shifter is the interface between the input of the driver, which uses logic levels, and the output stage;
- the under-voltage lock-out (UVLO) protection circuit, which ensure safe shutdown of the power circuit if the driver power supply is lost;
- the short-circuit protection turns the JFET off if  $V_{ds}$  exceeds a given value in the on-state, denoting an over-current condition;
- a thermal protection also turns the JFET off if the temperature of the driver becomes excessive;

- an isolation block ensures the transfer of both power supply (for the driver IC) and driving signal to the input of the gate driver. In the case of an inverter, as described below, this is required to drive the upper transistor.

All these functions were developed for our Application-Specific Integrated Circuit (ASIC). However, not all of them are used for the gate driver presented here. Basically, for the prototype described in this paper, only the output stage and the level shifter block are used. The signal and power isolation is provided by external (and low-temperature-rated) components. The layout of the  $3 \times 3 \text{ mm}^2$  driver die is visible figure 3.

As an example of the effect of the wide temperature-range on the ASIC design, the dead-time generation circuit is visible in figure 4. This dead-time delay is used to avoid cross-conduction of the push-pull output stage. For the sake of flexibility, it was decided to design a configurable dead time function, in which the delay could be adjusted using three transistors. As the generation of the delay is based on an R-C circuit, the increase of the parasitic resistances with the temperature would result in an increase of the delay. To limit this effect, a negative temperature coefficient (NTC) resistance was used. The measurement of the dead-time duration as a function of the temperature, for 4 different configurations, is given in figure 5. It can be seen that the NTC resistor actually dominates up to  $200^\circ\text{C}$ . Even with a single capacitor (“controls OFF” configuration), the dead-time delay remains superior to 120 ns. This value was found to be sufficient at any temperature to avoid cross-conduction of the push-pull stage.

## 4 Prototype and test setup

In addition to the SiC JFETs and the gate drivers ASIC, some passive components are required to build the circuit from figure 6: 6 low-voltage capacitors (Eurofarad) provide local decoupling for the gate drivers. 2 RC network, using a high temperature resistor (Vishay PHT, with  $230^\circ\text{C}$  max. capability) and a low voltage capacitor are used to connect the gate drivers to the JFETs. Finally, a high voltage ceramic capacitor (Presidio) provides local DC bus decoupling.

All the components of the inverter are assembled on a ceramic substrate (Curamik DBC) using silver sintering, and the substrate itself is sintered in a metal package. Wirebonding is performed using  $150 \mu\text{m}$  aluminium wire and  $50 \mu\text{m}$  gold wire (for the gate driver).

For the tests presented here, no encapsulation was used in the module, so we limited the DC bus voltage to 200 V in order to avoid arcing in air.

A picture of the test setup is given in figure 8: the module is attached to a hotplate (an aluminium block with a heating cartridge and a temperature controller). A PCB break-out board was designed to provide a con-

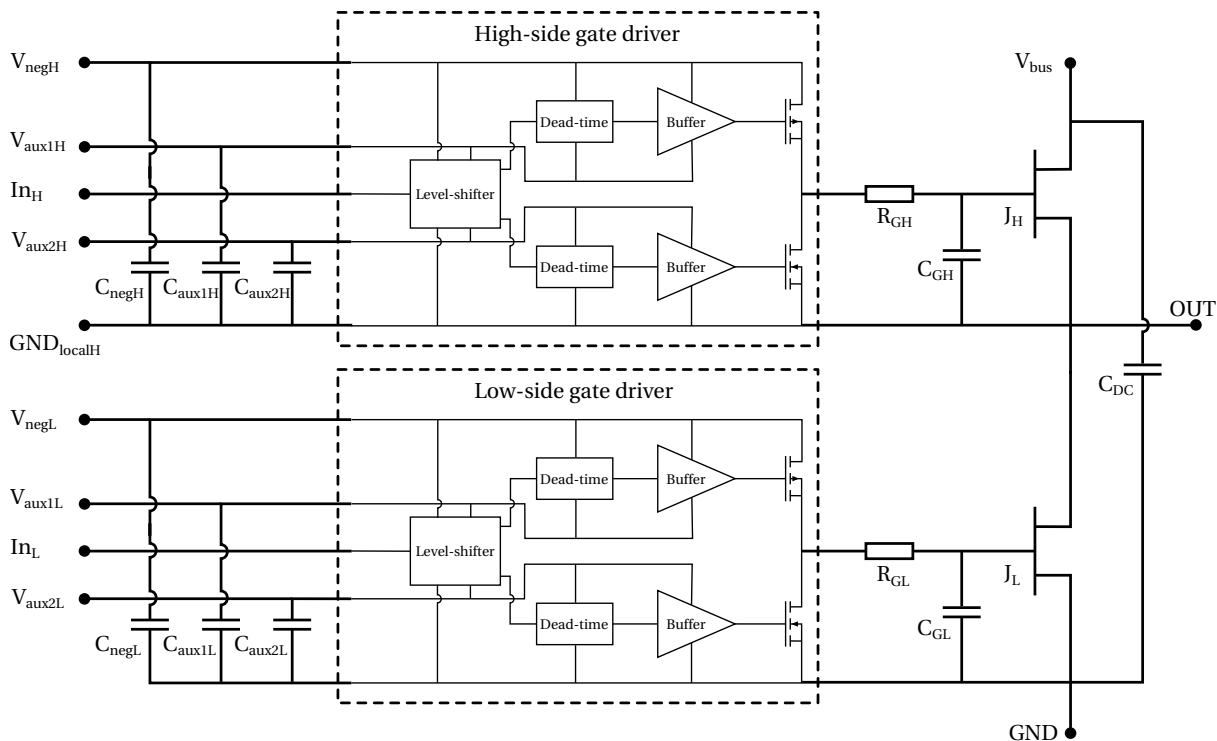


Figure 6: Schematic of the power module

venient way to connect the external power supplies and driving signals, and to host a 1  $\mu$ F, 1000 V, ceramic capacitor (DC decoupling). All the measurements presented were performed on this board. The temperature of the hotplate was varied from the ambient up to 200°C.

The driving signals are generated using a dedicated control board, built around a FPGA to ensure accurate and adjustable timing. For the measurements presented here, the driving waveforms were set to 10 kHz, 50% duty cycle, and a 1.2  $\mu$ s dead-time. The signals are transmitted through fiber optics to two adapter boards, which host the isolated auxiliary power supplies (connected to terminals  $V_{neg}$  and  $V_{auxX}$  in figure 6) and the driving signal conditioning. These boards are then connected to the break-out board.

The measurements were performed using a MSO4104 Tektronix oscilloscope, two P6139 500 MHz passive voltage probes and a TCP202A 50 MHz current probe. A power resistor, with a low parasitic inductance, was connected between the “OUT” and the “GND” terminals of the power module (see figure 6) with  $\approx$  50 cm cables.

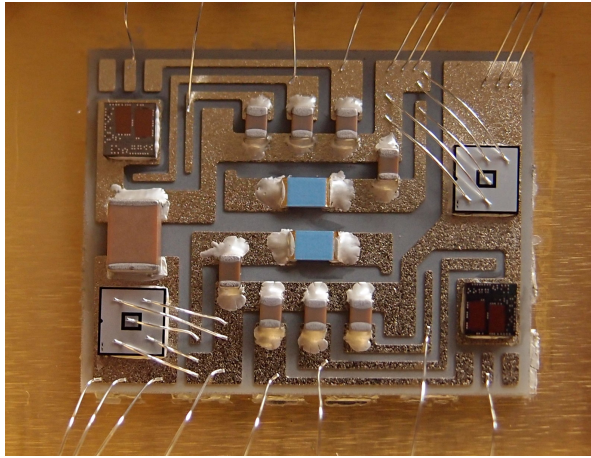
## 5 Experimental results

Some of the waveforms measured on the prototype are given in figure 9. At  $t=-48.85 \mu$ s, the upper transistor ( $J_H$  in figure 6) is turned-on. The voltage rise is very fast,  $\approx$  15 ns, and shows very little ringing, thanks to the DC decoupling capacitors (1  $\mu$ F on the break-out board, and 10 nF in the power module). The corresponding

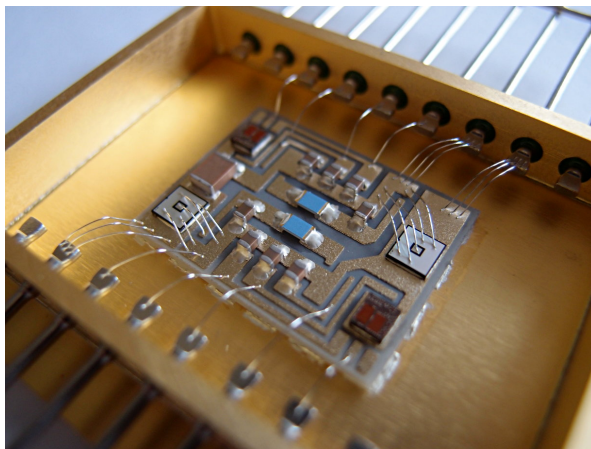
current rise is also very fast, albeit with more oscillations, probably caused by some parasitic inductance in the output load. However, note that the frequency of these oscillations (40 MHz) is close to the bandwidth limit of the current probe, and more investigations are required to actually point their cause and properly assess their amplitude.

The turn-off waveforms of  $J_H$  are slower, and look the same on both the voltage (figure 9a) and the current (figure 9b) graphs. This indicates that at this timescale the parasitic elements of the output load are negligible and it has a resistive behaviour. As this output resistance is fairly high (100  $\Omega$ ), it forms a RC cell with the parasitic capacitances of the JFETs (in the order of a few hundred of picofarad each), slowing-down the switching waveforms. Note, however, that this is due to the high impedance of the output load (as well as to its asymmetrical connection between the GND and OUT terminals), and would not occur with more realistic loads. Tests performed (at lower DC bus voltage) with a 50  $\Omega$  load showed switching times reduced from 500 ns down to 250 ns. Furthermore, as we chose a fairly conservative dead-time, the turning-on of  $J_L$  is not visible in figure 9. A more aggressive dead-time value (100 to 200 ns) would have resulted in a faster transient.

As mentioned above, the tests were limited to 200 V DC bus voltage to prevent arcing, as no encapsulation was used at this stage (to get access to the internals of the power module and enable electrical measurements). For the same reason, we limited the test temperature to 200°C. Regarding the switching waveforms, no change was observed from room temperature up to 200°C: the



(a)



(b)

Figure 7: The populated power substrate (before wirebonding of the drivers) (a) and the substrate in its hermetic case (with-out lead) (b).

rising and falling times were identical, as were the ringing amplitude and frequency. The voltage drop in the upper JFET, which is supposed to increase with temperature (due to the increase in  $R_{DSon}$  was too small (estimated at 100 to 200 mV) to be measured using our test setup.

## 6 Conclusion and future work

The test module presented in this paper not only contains power switches, but also their gate drive and associated passive components. Its operation was demonstrated up to 200°C ambient temperature, under a reduced bus voltage (200 V) and drain current (2 A peak).

Once a suitable passivation material has been applied (probably a silicone gel), tests will be performed over a higher voltage range, and with a lower impedance load. As this power module was designed to suit the needs of the new aeronautic HVDC bus, its nominal operating voltage is 540 V. The operating temperature is currently limited by the temperature ratings of most capacitors we

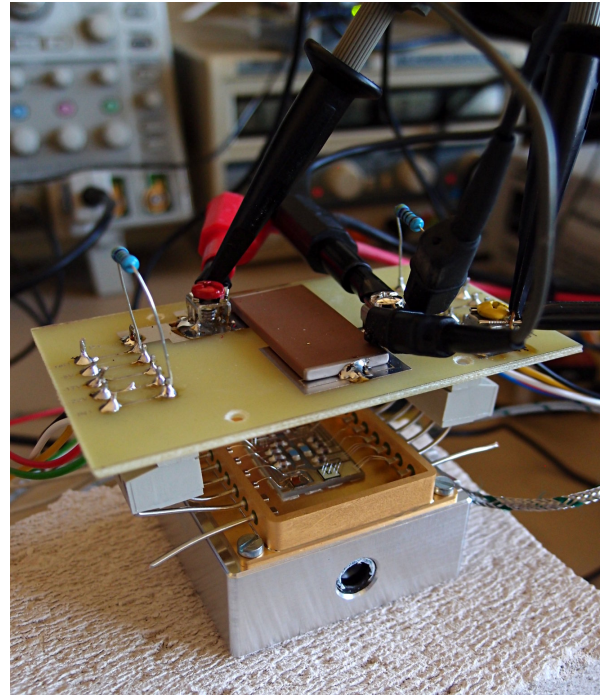


Figure 8: The module, attached to a temperature-controlled support, with a break-out board on top

used (200°C). As some capacitors are now available for higher temperatures (250 to 260°C), the next stumbling block is expected to be the silicone gel (with a temperature limit below 250°C). Other passivation schemes, such as hermetic packaging or fluorinated parylene must therefore be investigated.

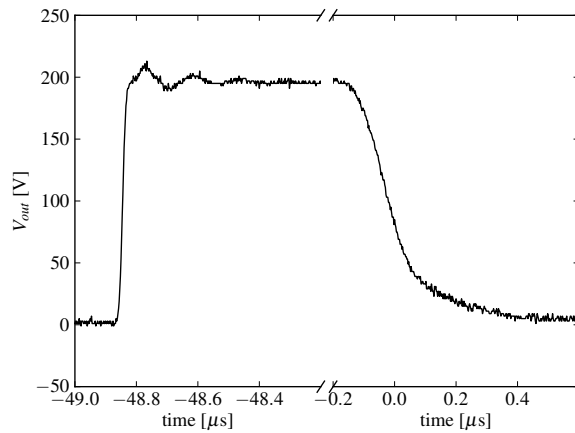
For the next generation, the main objective is to integrate more functions in the power module. In particular, all the isolation blocks (power and signal to the drivers) need to be integrated. This requires non only some transformers that can withstand higher operating temperatures, but also transformers with a very high frequency capability and very low parasitic capacitance, to match the speed of the SiC power switches.

## Acknowledgments

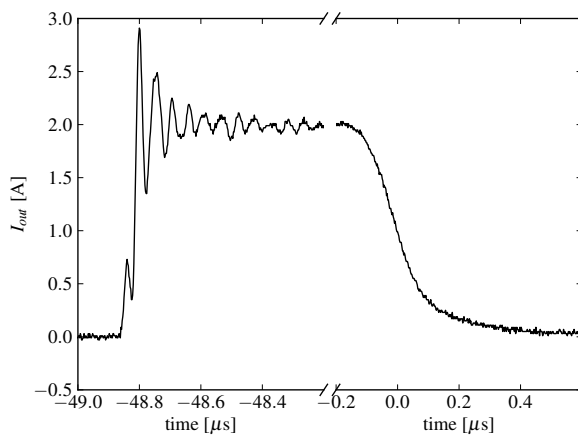
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(a)



(b)

Figure 9: Voltage (a) and current (b) waveforms measured at 200°C, with 200 V DC bus voltage and a 100 Ω power resistor connected between the output terminal of the module and the ground.

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