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Analysis of the SiC VJFET gate punch-through and its dependence with the temperature

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Keywords

«Silicon Carbide (SiC)», «JFET», «Device characterisation», «Device modeling», «High temperature electronics».

Abstract

Turning off a SiC VJFET from INFINEON requires to apply a gate-to-source voltage comprised between the JFET gate threshold voltage and the punch-through voltage. Unfortunately, for applications operating over a large temperature range, these two limits vary with the temperature and reduce the useful blocking gate-to-source voltage range as the temperature rises. So, the punch-through temperature dependence is a very important feature for applications operating in a wide temperature range like aeronautic applications. This paper addresses the analysis and modeling of the punch-through phenomenon and its dependence to the temperature. The proposed model gives a good agreement with the experimental data.

Introduction

On a vertical SiC-JFET like those of INFINEON, there is a N-type lateral channel with two P-layers connected to the source and the gate terminals respectively. Because of the difference in potentials between the two P-regions of a PNP structure (Fig. 1), the punch-through phenomenon may occur. When this happens, the gate current dramatically increases.

The punch-through phenomenon was firstly described in bipolar junction transistors [1]. It occurs when the two space-charge regions of a PNP structure join. Holes may then diffuse from one P-layer to the other one.

Punch-through can also be observed in PIN diodes, when the space-charge region spreads all over the low-doped base [1]. This corresponds to a PNN⁺ structure, so there is no current increase, but an electric field rise. Therefore, this is a very different phenomena, even though it has the same name.

The devices under test (DUTs) investigated here are 100 mΩ, 1200 V VJFETs from SiCED which is the company which developed the VJFET for INFINEON. In such a VJFET, the punch-through occurrence defines the practical gate-to-source voltage limit (Fig. 2), i.e. when the hole current starts to flow in the PNP structure, V_{PT} as shown in Fig. 2. This was described in [2].

Fig. 3 shows the measurement of the threshold voltage, V_{T0} , and the punch-through voltage, V_{PT} , versus the temperature. The threshold voltage, V_{T0} , is classically defined from the saturation current characteristics, $i_D^{SAT}(V_{GS})$ [3]. A quadratic fitting of the characteristics around zero current is useful to improve the accuracy of V_{T0} extraction.

$$i_D^{SAT}(V_{T0})=0 \quad (1)$$

The punch-through voltage, V_{PT} , is defined from the characteristic in Fig. 2. The punch-through reference current is arbitrarily defined as in [4],

$$i_{PT}^{REF} = 200 \mu A \quad (2)$$

And the punch-through voltage, V_{PT} , is defined as,

$$i_G(V_{PT}) = i_{PT}^{REF} \quad (3)$$

Clearly as shown in Fig. 3, the gate-to-source voltage range allowed to turn the JFET off decreases with the temperature. So the point has to be carefully accounted to design a system operating over a wide range of temperature for example in aeronautic applications. Therefore, the analysis and the modeling of both $V_{T0}(T)$ and $V_{PT}(T)$ are of great interest.

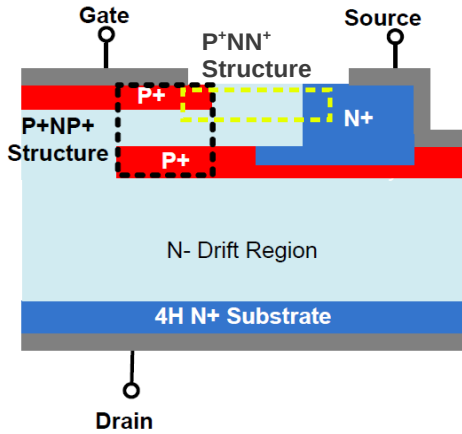


Fig. 1: Typical structure of a VJFET from INFINEON with the highlighted punch-through region

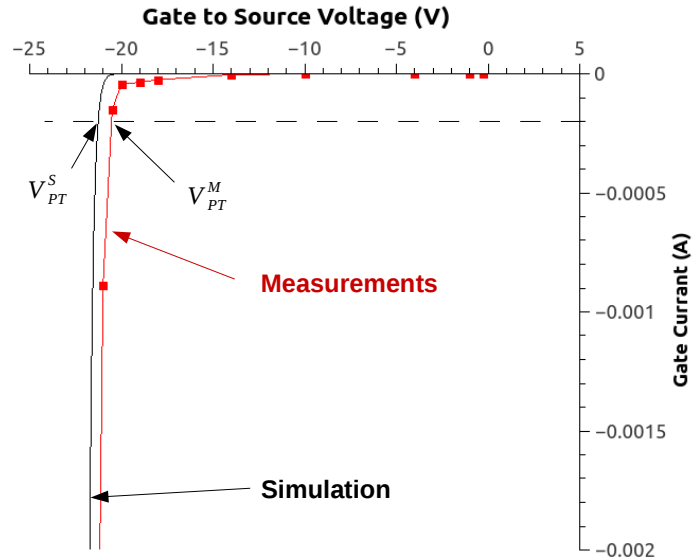


Fig. 2: Measurements and simulation of the I-V gate characteristics for the DUT in linear scales.

Analysis and modeling of the punch-through phenomenon

The detailed modeling of the punch-through current is given in appendix. It is classically based on the calculation of the current passing through a potential barrier height [5], given by,

$$i_{PT} = -\frac{i_{PT}^0 \frac{\sqrt{\pi}}{2} \sqrt{\frac{u_T}{V_p}}}{\frac{1}{a} \int_0^{2a} \exp \frac{\psi(y)}{u_T} dy} \left(1 - \exp \left(\frac{V_{GS}}{u_T} \right) \right) \quad (4)$$

Where, V_{GS} , is the gate-to-source voltage, u_T , is the thermal potential, a , is the half thickness of the channel, i_{PT}^{ref} , is a reference punch-through current defined in appendix, and $\psi(y)$ the electric potential along the channel. Fig. 4 shows the simplified 1D representation of the punch-through phenomenon as already shown in [2] and [4]. The computation of the punch-through current in the PNP case was presented in [4] and yields to

$$i_{PT} = i_{PT}^0 \left(1 - e^{-\frac{V_{GS}}{u_T}} \right) e^{-\frac{u_B}{u_T}} \quad (5)$$

where $i_{PT}^0 \approx 7 kA$ is a constant defined in appendix representing the maximal punch-through current. The pinch-off voltage is classically given by,

$$V_p = \frac{q N_D a^2}{2 \epsilon} \quad (6)$$

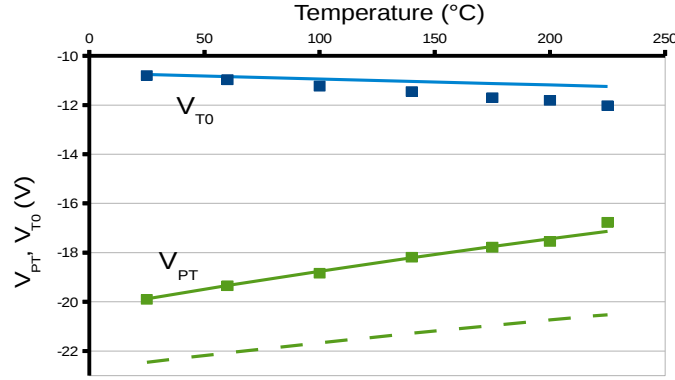


Fig. 3: Measurements (dots) and simulation (lines) of the threshold (top) and punch-through (bottom) voltages, versus the temperature, for the DUT. The green dashed line corresponds to the simulation of the punch-through voltage for $k=1$ (see Eq. 10).

The barrier height is given by,

$$u_B = V_P \left(1 + \frac{V_{GS}}{4 V_P} \right)^2 \quad (7)$$

Symbol	Definition	Value
N_A	Doping concentration in both gates	$5 \times 10^{19} \text{ cm}^{-3}$
A_G	Gate Equivalent Area, estimated from the die area.	8 mm^2
V_P	Pinch-off voltage	7.29 V

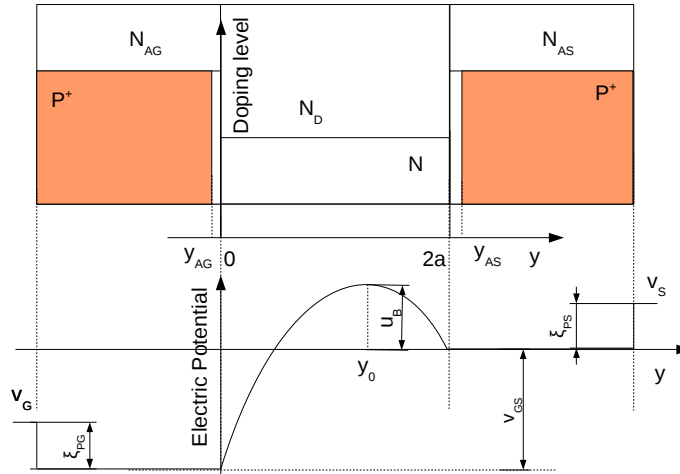


Fig. 4: Typical representation of the electric potential for V_{GS} between V_{T0} and V_{PT}

Fig. 7 and Fig. 8 show the leakage current between gate and source. From 0 to the break in Fig. 8 the current is the leakage current of the P+NN+ junction (see Fig. 1) between gate and source. Classically in SiC devices, the measured leakage current is much greater than the generation current of this junction [6]. Higher values of the current correspond to the punch-through current. Fig. 6 shows numerical simulation of the punch-through current and yields to a similar value of the punch-through voltage. The simulated leakage current is very low too !

The calculation is detailed in appendix. The parabolic shape of the electrical potential shown in Fig. 5, is confirmed by the numerical simulations in Fig. 5 and in Equation (7).

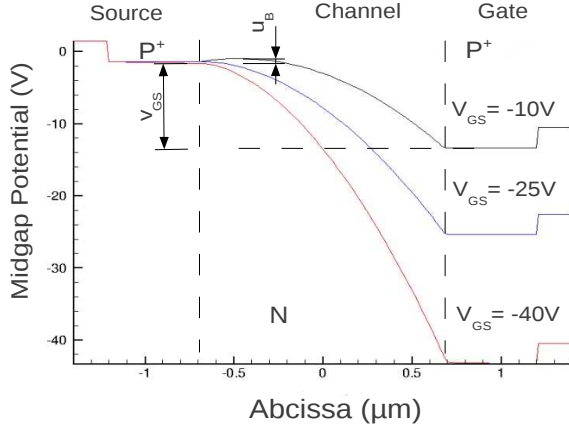


Fig. 5: Numerical simulation (using Sentaurus) of the potential across the PNP structure for various V_{GS} values

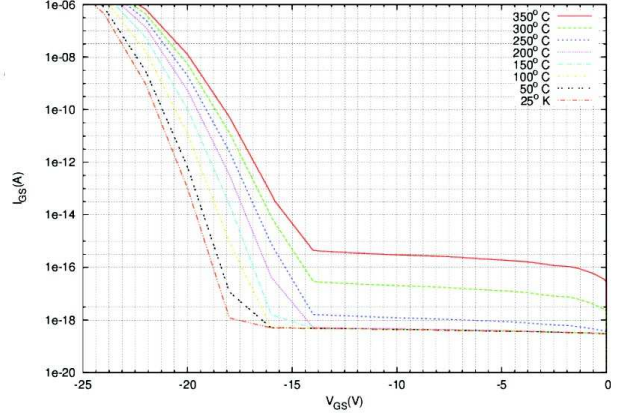


Fig. 6: Numerical simulation (using Sentaurus) of punch-through current in the PNP structure

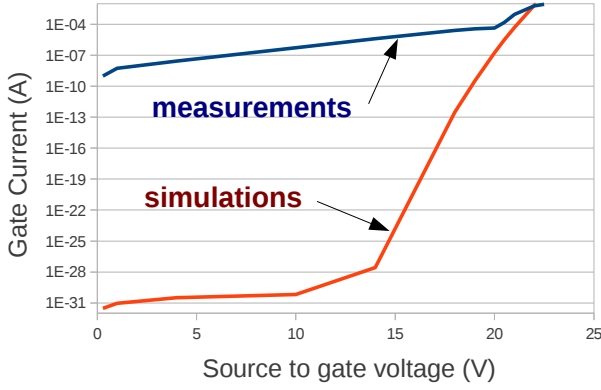


Fig. 7 Comparison between simulation and measurements of the gate current (showing the generation current)

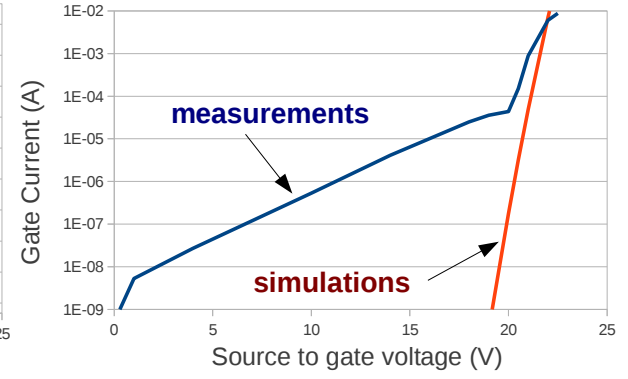


Fig. 8: Comparison between simulation and measurements of the gate current (Zoom)

Computation of the punch-through voltage

Clearly, for sufficiently negative gate-to-source voltage, the punch-through current increases dramatically, and $1 \gg e^{\frac{V_{GS}}{u_T}}$ so equation (2) may be simplified as,

$$i_{PT} = i_{PT}^0 e^{-\frac{u_B}{u_T}} \quad (8)$$

Considering the definition of V_{PT} in (3), combining (8) with (7), yields to

$$\alpha = \ln \left(\frac{i_{PT}^0}{i_{PT}^{ref}} \right) = \frac{u_B}{u_T} = \frac{V_P}{u_T} \left(1 + \frac{V_{PT}}{4 V_P} \right)^2 \quad (9)$$

So,

$$V_{PT} = 4 V_P \left(1 - \sqrt{(k + \alpha) \frac{u_T}{V_P}} \right) \quad (10)$$

Which defines the temperature dependence of V_{PT} because of the temperature dependence of the thermal voltage, u_T , and the hole mobility, μ_p , through i_{PT}^0 (Eq. 37). The factor k has been introduced to account the current level. Without this ratio, $i_{PT}^{REF} \sim 1 \text{ nA}$ has to be chosen which is not acceptable for the measurement data, but it is compatible with the numerical simulation in Fig. 6. Moreover, the

temperature dependencies are defined by the equations given in appendix and the material data used in [7].

Computation the gate threshold voltage

The threshold voltage, V_{T0} , is by definition the gate-source voltage threshold for which the saturation current reach zero as given in (1). Reference [3] yields a model of the double channel JFET and gives the following expression for the pinch-off current in the lateral channel,

$$i_{CH}^p = \frac{V_p}{3R_{CH}} \Delta(\gamma_1, \gamma_2) \quad (11)$$

Where R_{CH} is the non-modulated channel resistance and γ_1 and γ_2 are standardized driven values. In blocking condition, that yields to the definition of standardized driven values as,

$$\gamma_1^{OFF} = \frac{V_{BI} - v_{GS}}{V_p} \quad (12)$$

and,

$$\gamma_2^{OFF} = \gamma_0 = \frac{V_{BI}}{V_p} \quad (13)$$

By definition, in blocking condition the pinch-off current equals zero [3], so,

$$\Delta(\gamma_1^{OFF}, \gamma_2^{OFF}) = 0 \quad (14)$$

The plot of the Δ function is given in Fig. 9.

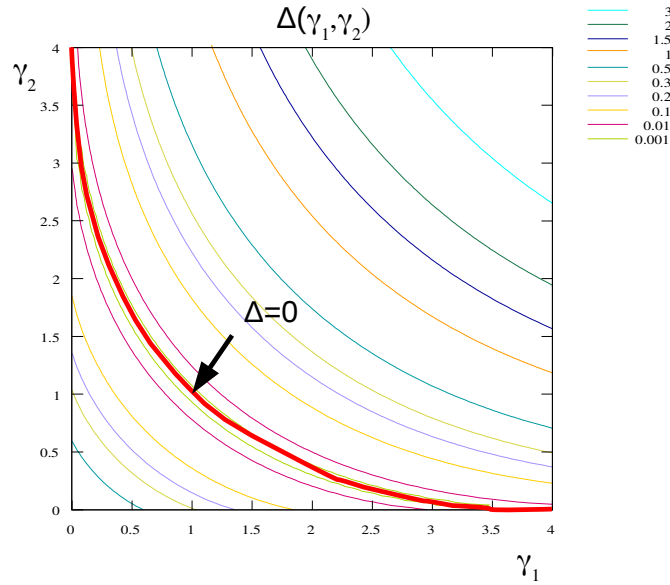


Fig. 9: Plot of the Δ function

So that defines a relation between γ_1^{OFF} and γ_2^{OFF} or γ_0 .

$$\gamma_1^{OFF} = \Gamma_1(\gamma_0) \quad (15)$$

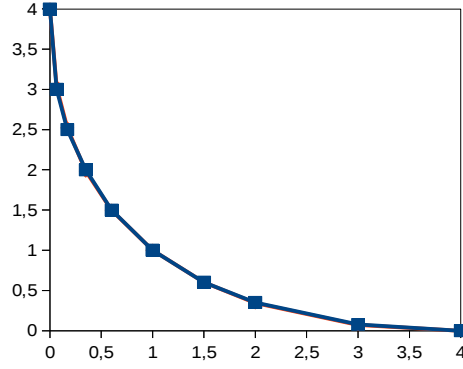


Fig. 10: Plot of Function $\Gamma_1(\gamma_0)$

At the blocking threshold, Equation (12) may be rewritten as,

$$v_{GS} = V_{T0} \quad (16)$$

$$\gamma_1^{OFF} = \frac{V_{BI} - v_{T0}}{V_p} \quad (17)$$

Which may be expressed as,

$$V_{T0} = V_{BI} - \Gamma_1\left(\frac{V_{BI}}{V_p}\right)V_p \quad (18)$$

The later expression yields the temperature dependence of V_{T0} through the temperature dependence of V_{BI} .

Notice that Equation (18) is different from the standard JFET model given by,

$$V_{T0} = V_{BI} - V_p \quad (19)$$

Results and discussion

The punch-through and threshold voltages were computed using equation (10) and (19) respectively. Fig. 5 Shows the superimposition of these computations and the experimental data. Clearly a good agreement was reached. An empirical value, k , has been used in equation (10) to reach a better fitting with experimental data. The issue is probably related to the modeling of the leakage current that classically failed in wide band gap device as shown in Fig. 6 but the obtained temperature dependence is very good, and based on physical data of the SiC-4H material. Moreover the empirical value, k , introduces a shift of about 2 V in the value of the punch-through voltage, so about 10% of error without correction with the empirical factor. If the computation seems to be complex because of the number of equations, these equations may be easily implemented in a compact model of the JFET, as in [3] using a modeling language like MAST or VHDL-AMS.

Conclusion

The punch-through voltage, V_{PT} , and the threshold voltage, V_{T0} , are the limits that define the gate-to-source range allowed to block the VJFET. Unfortunately, both parameters depend on the temperature. The paper has presented some measurement results versus the temperature of these parameters. Clearly, the useful gate-voltage range reduces with increasing temperatures. The paper has also developed from a physical analysis of the VJFET device, a complete analysis of the dependence of these parameters with respect to the temperature by deriving analytical expressions of these parameters. The obtained models are in good agreement with the experimental data. It remains to integrate these expressions in a complete model of the VJFET.

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Appendix

Calculating the barrier height

In the N-type region, it is obtained,

$$\frac{\partial E}{\partial y} = \frac{q N_D}{\epsilon} \quad (20)$$

Which yields to the following expression for the electric potential in the N-region,

$$\psi(y) = \psi_M - \frac{q N_D}{\epsilon} \frac{(y - y_0)^2}{2} = \psi_M - V_p \left(\frac{y - y_0}{a} \right)^2 \quad (21)$$

Assuming,

$$\psi(2a) = 0 = \psi_M - V_p \left(\frac{2a - y_0}{a} \right)^2 \quad (22)$$

The definitions in Fig. 2 yield to,

$$\psi(0) = v_{GS} = \psi_M - V_p \left(\frac{0 - y_0}{a} \right)^2 \quad (23)$$

The maximum is reached for,

$$\psi(y_0) = u_B = \psi_M \quad (24)$$

So, the difference between Equations (23) and (22) yields to,

$$v_{GS} = -V_p \left(\left(2 - \frac{y_0}{a} \right)^2 - \left(\frac{y_0}{a} \right)^2 \right) = -4 V_p \left(1 - \frac{y_0}{a} \right) \quad (25)$$

and

$$\frac{y_0}{a} = 1 - \frac{v_{GS}}{4 V_p} \quad (26)$$

Substituting it in (22) yields to Equation (7),

$$u_B = \psi_M = V_p \left(2 - \frac{y_0}{a} \right)^2 = V_p \left(1 + \frac{V_{GS}}{4 V_p} \right)^2 \quad (27)$$

The electrical potential is obtained from Equation (21) by substituting (26) and (27),

$$\psi(y) = V_p \left[\left(1 + \frac{V_{GS}}{4 V_p} \right)^2 - \left(\frac{y}{a} - 1 + \frac{V_{GS}}{4 V_p} \right)^2 \right] = V_{GS} - V_p \left[\frac{y^2}{a^2} + \frac{2y}{a} \left(\frac{V_{GS}}{4 V_p} - 1 \right) \right] \quad (28)$$

Calculating the punch-through current

Assuming a constant hole-mobility, the drift-diffusion equation for the holes may be written as,

$$J_p = q \mu_p (p E - u_T \frac{\partial p}{\partial y}) = -q \mu_p (p \frac{\partial \psi}{\partial y} + u_T \frac{\partial p}{\partial y}) \quad (29)$$

Moreover it is well known that,

$$\frac{\partial}{\partial y} \left(p e^{\frac{\psi}{u_T}} \right) = \frac{\partial p}{\partial y} e^{\frac{\psi}{u_T}} + \frac{p}{u_T} e^{\frac{\psi}{u_T}} \frac{\partial \psi}{\partial y} = e^{\frac{\psi}{u_T}} \left(\frac{\partial p}{\partial y} + \frac{p}{u_T} \frac{\partial \psi}{\partial y} \right) \quad (30)$$

So,

$$J_p e^{\frac{\psi}{u_T}} = -q \mu_p u_T e^{\frac{\psi}{u_T}} \left(\frac{p}{u_T} \frac{\partial \psi}{\partial y} + \frac{\partial p}{\partial y} \right) = -q \mu_p u_T \frac{\partial}{\partial y} \left(p e^{\frac{\psi}{u_T}} \right) \quad (31)$$

The integration of equation (31) in the interval $[0 - \epsilon_y, 2a + \epsilon_y]$ where ϵ_y is a small length that insures the side are both in the P+ layers, yields to,

$$\int_{-\epsilon_y}^{2a+\epsilon_y} J_p e^{\frac{\psi}{u_T}} dy = -q \mu_p u_T \int_{-\epsilon_y}^{2a+\epsilon_y} \frac{\partial}{\partial y} \left(p e^{\frac{\psi}{u_T}} \right) dy = -q \mu_p u_T \left[p e^{\frac{\psi}{u_T}} \right]_{-\epsilon_y}^{2a+\epsilon_y} \quad (32)$$

Assuming a uniform current density inside the channel, that may be simplified as,

$$J_p \int_{-\epsilon_y}^{2a+\epsilon_y} e^{\frac{\psi}{u_T}} dy = -q \mu_p u_T \left(N_{AS} e^{\frac{\psi(2a+\epsilon_y)}{u_T}} - N_{AG} e^{\frac{\psi(-\epsilon_y)}{u_T}} \right) \quad (33)$$

Assuming same value of the doping concentration in the both sides, it is obtained,

$$J_p \int_0^{2a} e^{\frac{\psi}{u_T}} dy = q \mu_p u_T N_A \left(1 - e^{\frac{V_{GS}}{u_T}} \right) \quad (34)$$

The current through the structure is given by,

$$i_{PT} = J_p A_G \quad (35)$$

So Equation (4) is obtained,

$$i_{PT} = - \frac{i_{PT}^{r0}}{\frac{1}{a} \int_0^{2a} \exp \frac{\psi(y)}{u_T} dy} \left(1 - \exp \left(\frac{V_{GS}}{u_T} \right) \right) \quad (36)$$

Where,

$$i_{PT}^{r0} = \frac{q \mu_p N_A u_T A_G}{a} \quad (37)$$

And,

$$\alpha_{PT} = \frac{1}{a} \int_0^{2a} \exp \frac{\psi(y)}{u_T} dy \quad (38)$$

Equation (36)

$$i_{PT} = -\frac{i_{PT}^{r0}}{\alpha_{PT}} \left(1 - \exp \left(\frac{V_{GS}}{u_T} \right) \right) \quad (39)$$

Using (28) Equation (38),

$$\alpha_{PT} = \frac{1}{a} \int_0^{2a} \exp \left(\frac{v_{GS} - V_P \left[\frac{y^2}{a^2} + \frac{2y}{a} \left(\frac{v_{GS}}{4V_P} - 1 \right) \right]}{u_T} \right) dy \quad (40)$$

Defining,

$$\beta_{PT} = \frac{V_P}{u_T} \quad (41)$$

$$y_{PT} = \frac{v_{GS}}{4V_P} - 1 \quad (42)$$

$$u = \frac{y}{a} \quad (43)$$

$$z = u + y_{PT} \quad (44)$$

Equation (40) may be rewritten as,

$$\alpha_{PT} = \frac{a}{u_T} \exp \frac{v_{GS}}{u_T} \int_0^2 \exp \left(-\beta_{PT} [u^2 + 2u y_{PT}] \right) du \quad (45)$$

or,

$$\alpha_{PT} = \exp \frac{v_{GS}}{u_T} \int_0^2 \exp \left(-\beta_{PT} [z^2 - y_{PT}^2] \right) dz \quad (46)$$

so,

$$\alpha_{PT} = \exp \left(\frac{v_{GS}}{u_T} + \beta_{PT} y_{PT}^2 \right) \int_0^2 \exp \left(-\beta_{PT} z^2 \right) dz \quad (47)$$

Accounting the error function definition,

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x \exp -\eta^2 d\eta \quad (48)$$

Using,

$$\eta = \sqrt{\beta_{PT}} z \quad (49)$$

it is obtained,

$$\int_0^x \exp -\eta^2 d\eta = \int_0^{\frac{x}{\sqrt{\beta_{PT}}}} \exp -\beta_{PT} z^2 \sqrt{\beta_{PT}} dz = \frac{\sqrt{\pi}}{2} \text{erf}(x) \quad (50)$$

Equation (47) may be rewritten as,

$$\alpha_{PT} = \frac{1}{2} \sqrt{\frac{\pi}{\beta_{PT}}} \exp \left(\frac{v_{GS}}{u_T} + \beta_{PT} y_{PT}^2 \right) \text{erf}(2\sqrt{\beta_{PT}}) \quad (51)$$

Assuming that,

$$\beta_{PT} \gg 1 \quad (52)$$

and the error function is very near 1 for high abscissa values, Equation () yields to

$$\alpha_{PT} \simeq \frac{1}{2} \sqrt{\frac{\pi}{\beta_{PT}}} \exp\left(\frac{v_{GS}}{u_T} + \beta_{PT} \gamma_{PT}^2\right) = \frac{\sqrt{\pi}}{2} \sqrt{\frac{u_T}{V_P}} \exp\left(\frac{v_{GS}}{u_T} + \frac{V_P}{u_T} \left(\frac{v_{GS}}{4V_P} - 1\right)^2\right) \quad (53)$$

So,

$$i_{PT} = \frac{i_{PT}^{r0}}{\left(\frac{\sqrt{\pi}}{2} \sqrt{\frac{u_T}{V_P}}\right)} \exp\left(-\frac{v_{GS}}{u_T} - \frac{V_P}{u_T} \left(\frac{v_{GS}}{4V_P} - 1\right)^2\right) \left(\exp\left(\frac{V_{GS}}{u_T}\right) - 1\right) \quad (54)$$

Which may be written as Equation (5),

$$i_{PT} = i_{PT}^0 \exp\left(-\frac{u_B}{u_T}\right) \left(\exp\left(\frac{V_{GS}}{u_T}\right) - 1\right) \quad (55)$$

Where,

$$i_{PT}^0 = \frac{i_{PT}^{r0}}{\left(\frac{\sqrt{\pi}}{2} \sqrt{\frac{u_T}{V_P}}\right)} = \frac{q \mu_p N_A u_T A_G}{\sqrt{\frac{\pi}{2}} L_{ND}} \quad (56)$$

and,

$$L_{ND} = \sqrt{\frac{\epsilon u_T}{q N_D}} = a \sqrt{\frac{u_T}{2 V_P}} \quad (57)$$

An assessed value is given by,

$$i_{PT}^0(300K) = \frac{q \mu_p u_T N_A A_G}{\sqrt{\frac{\pi}{2}} L_{ND}} \simeq 7.0 \text{ kA} \quad (58)$$