

Thermal stability of SiC JFETs in conduction mode

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Introduction

JFET Characterization

Experimental study of the runaway condition

Conclusions

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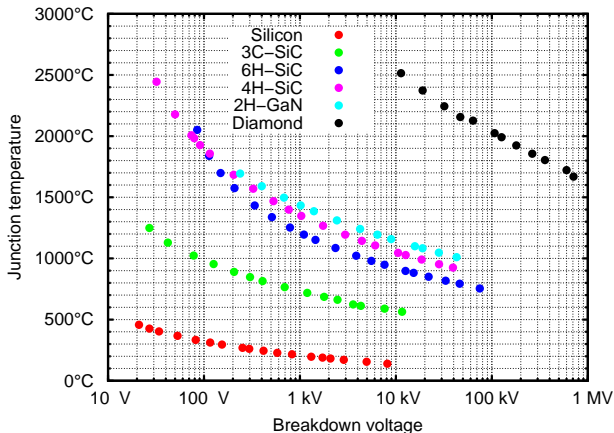
JFET Characterization

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Maximum operating temperature – Theory



- ▶ Silicon operating temp is intrinsically limited at high voltages.
- ▶ Wide-bandgap semiconductors (inc. SiC) go much higher



Maximum operating temperature – Practically

Example: SiCED JFET:

| | material | max. temp. | cause |
|---------------------|-----------|------------|---------------|
| Semiconductor | SiC | 2730 °C | sublimation |
| backside metal | Ag | 962 °C | melting point |
| Top metallization | Al | 660 °C | melting point |
| second. passivation | polyimide | 500-620 °C | decomposition |

- ▶ Most of these limitations can be overcome by the die manufacturer (e.g. topside metal)
 - ▶ Other will depend on the packaging technology
 - ▶ Case material (ceramic, plastic, ...)
 - ▶ Solder alloys, etc.
- $T_J > 300\text{ °C}$ is possible



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Reduced cooling

Take advantage of the high junction temp. capability of SiC devices to save on thermal management



Source: APEI [1]. Converter operating at 150°C ambient, with 250°C junction temperature, using passive cooling.

- ▶ Operation in milder ambient
- ▶ Reduction in
 - ▶ Volume, weight
 - ▶ Complexity (passive vs active)
- ▶ Many applications:
 - ▶ Transports
 - ▶ Low-maintenance, high-rel.

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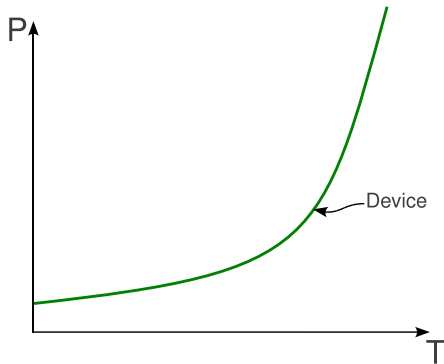
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→ Thermal runaway issues must be considered

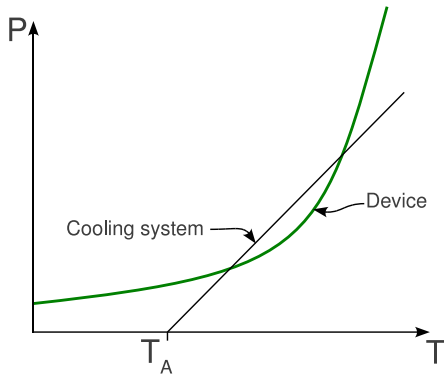


Thermal Run-away mechanism – Principle



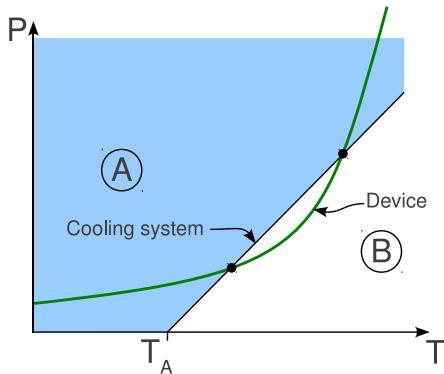
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- ▶ its associated cooling system
- ▶ in region A, the device dissipates more than the cooling system can extract
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- ▶ two equilibrium points: one stable and one unstable
- ▶ above the unstable point, run-away occurs

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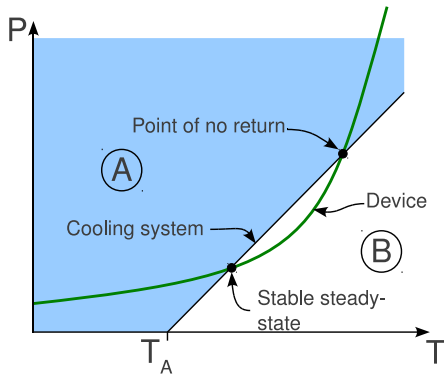
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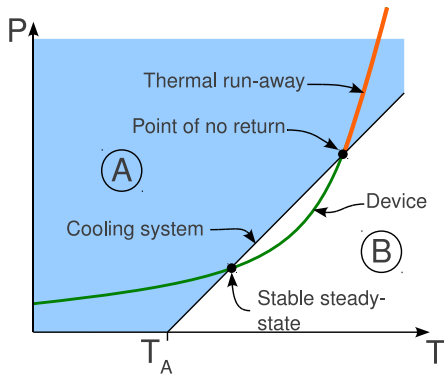
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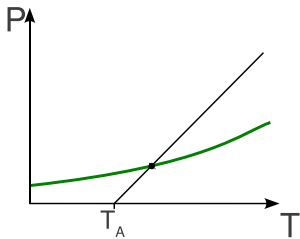
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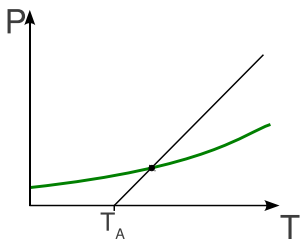
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Thermal Run-away mechanism – examples

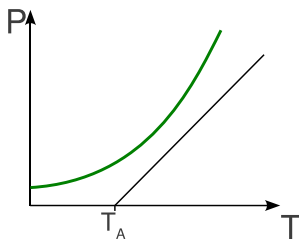


Always stable

Thermal Run-away mechanism – examples

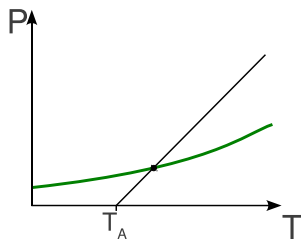


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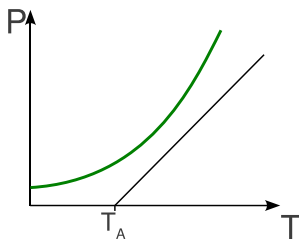


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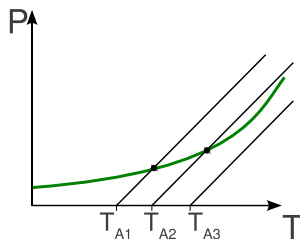
Thermal Run-away mechanism – examples



Always stable



Always unstable



Becoming unstable
with ambient
temperature rise

Aim of the study

- ▶ **JFETs can operate at high temperature**
- ▶ We might take advantage of this to size the cooling system down



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Is there a risk of thermal runaway of JFETs?

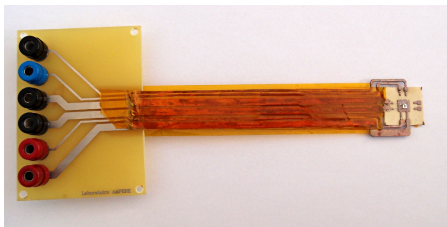
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Test configuration



- ▶ High temperature test system
 - ▶ Silver-sintered interconnects
 - ▶ Ceramic substrate (DBC)
 - ▶ Copper-kapton leadframe
- ▶ DUT: 500 m Ω SiC JFET from SiCED
- ▶ characterization:
 - ▶ Tektronix 371A curve tracer
 - ▶ Thermonics T2500-E conditioner

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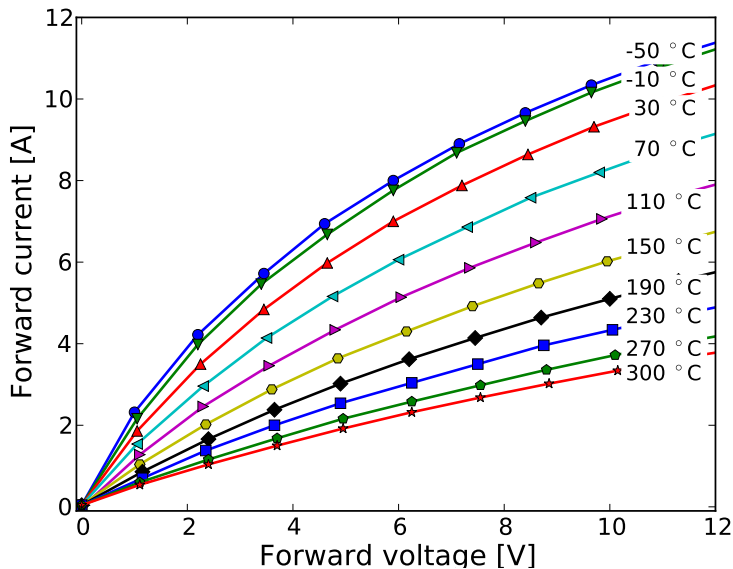


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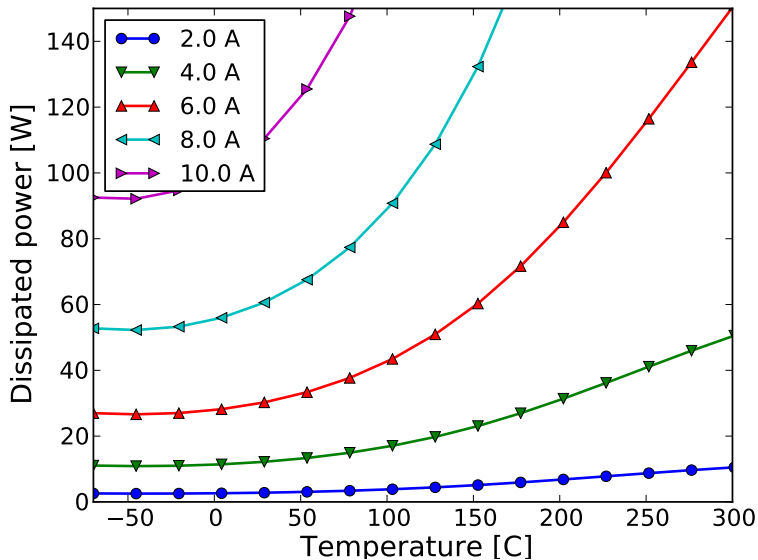
Source: Thermonics T-2500SE Datasheet

Static Characterization over a wide temperature range

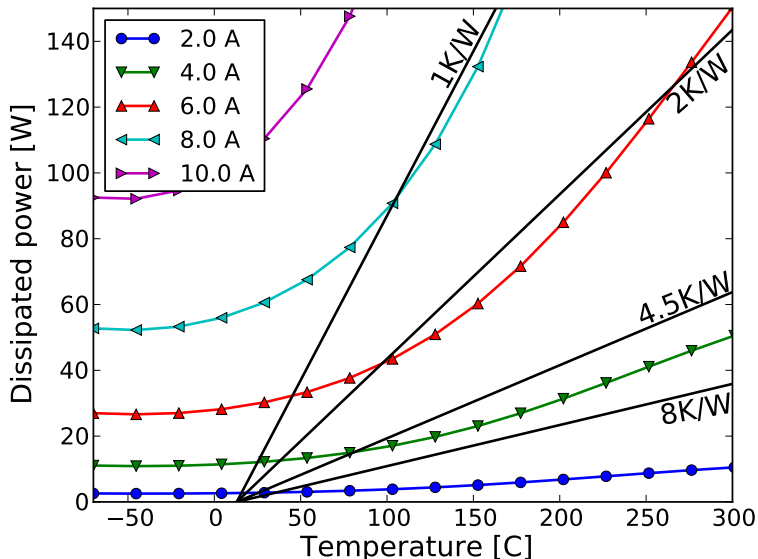


$V_{GS} = 0 V$, i.e. device fully-on

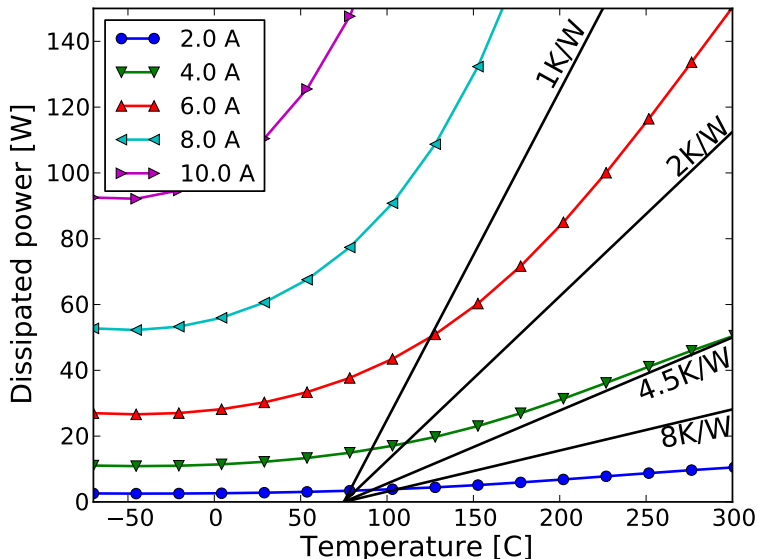
Power dissipation as a function of the junction temp.



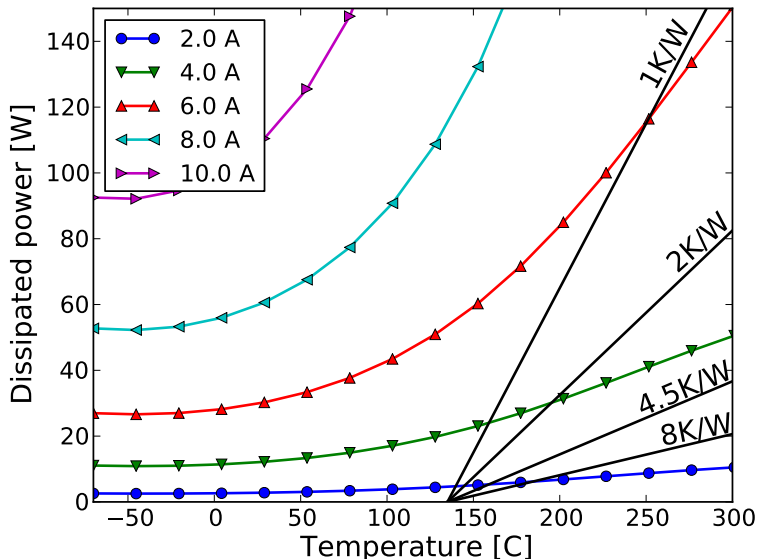
Power dissipation as a function of the junction temp.



Power dissipation as a function of the junction temp.



Power dissipation as a function of the junction temp.



Conclusion on static characterization

- ▶ Conduction losses of the JFET (P) increase with the temperature
- ▶ This increase can be faster than the increase in cooling capability (Q)

$$\frac{\partial P}{\partial T_j} > \frac{\partial Q}{\partial T_j}$$

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→ Thermal runaway seems possible

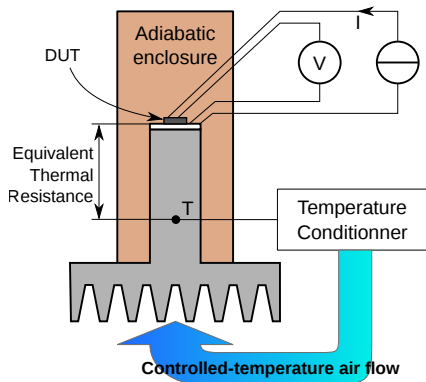
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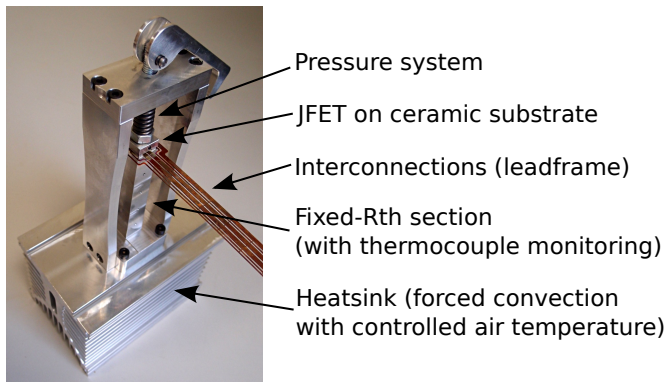
Test Bench



- ▶ Temperature at point T controlled using the conditioner
- ▶ Separate control of R_{Th} and T_A
- ▶ DUT in conduction mode, supplied by a current source
- ▶ Here, $R_{Th} = 4.5 \text{ K/W}$, $T_A = 13, 75, \text{ or } 135^\circ\text{C}$

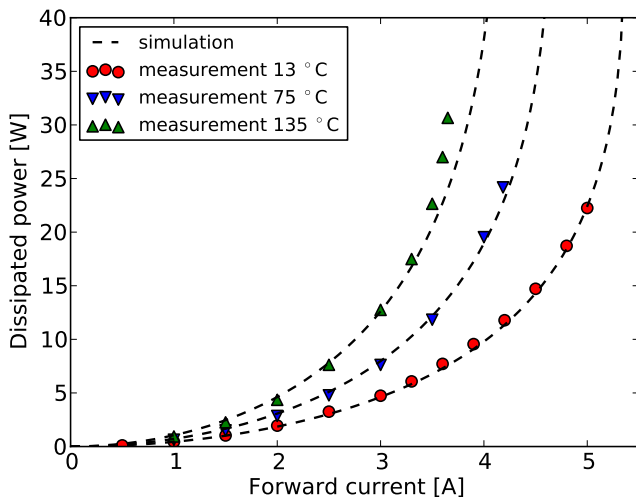


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Thermal Runaway – 1

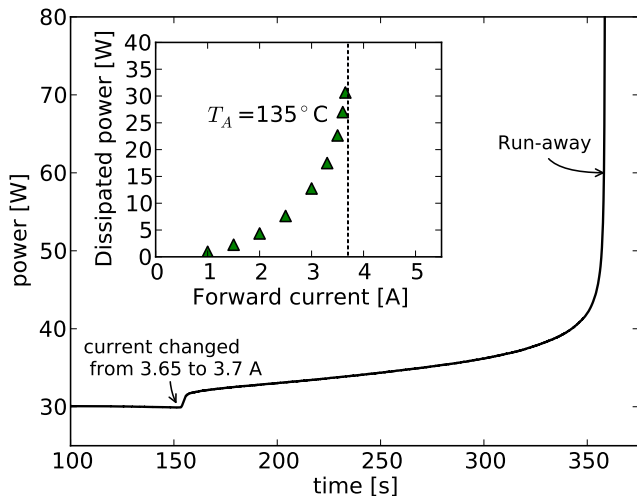


“Simulation”: losses due to the theoretical increase in R_{DSon}

$$\text{with } T_j: R_{DSon}(T_j) = R_{DSon}(300\text{ K}) \left(\frac{T_j}{300} \right)^{2.4}$$



Thermal Runaway – 2



Power supply limit: 100 W, $T_j \approx 135 + 4.5 \times 100 = 585^\circ\text{C}$
The JFET survived the test.



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High temperature operation

- ▶ JFETs can operate at very high T_j ($> 300^\circ\text{C}$)
- ▶ Newer generations have higher current capability

Thermal runaway

- ▶ They are sensitive to thermal runaway in conduction
 - ▶ Their $R_{DS_{on}}$ increases strongly with temperature
- ▶ Their cooling system should be carefully designed
 - ▶ Providing R_{Th} is low enough, JFETs are stable
- ▶ slow phenomenon, can be avoided by driver protection
 - ▶ Much like the *desat* protection for IGBTs, to ensure graceful response to unexpected transients



Thank you for your attention,

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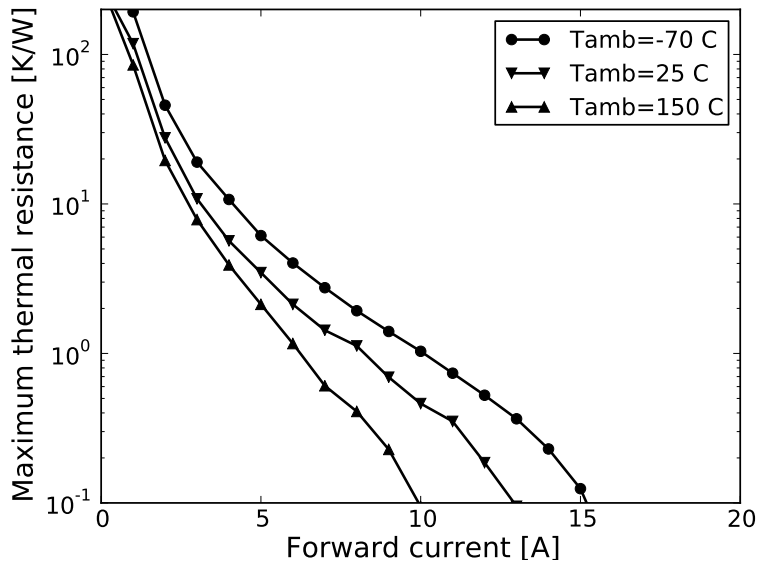


Properties of some semiconductors

| | "Classical" | | wide-bandgap | | | | |
|--------------------------------------------------------------------------------|-------------------|-------------------|---------------------|---------------------|-------------------|-------------------|-------------------|
| | Si | GaAs | 3C-SiC | 6H-SiC | 4H-SiC | GaN | Diamond |
| Bandgap Energy E_g (eV) | 1,12 | 1,4 | 2,3 | 2,9 | 3,2 | 3,39 | 5,6 |
| Elec. mobility μ_n (cm ² .V ⁻¹ .s ⁻¹) | 1450 | 8500 | 1000 | 415 | 950 | 2000 | 4000 |
| Hole mobility μ_p (cm ² .V ⁻¹ .s ⁻¹) | 450 | 400 | 45 | 90 | 115 | 350 | 3800 |
| Critical elec. field E_C (V.cm ⁻¹) | 3.10 ⁵ | 4.10 ⁵ | 2.10 ⁶ | 2,5.10 ⁶ | 3.10 ⁶ | 5.10 ⁶ | 10 ⁷ |
| Saturation velocity v_{sat} (cm.s ⁻¹) | 10 ⁷ | 2.10 ⁷ | 2,5.10 ⁷ | 2.10 ⁷ | 2.10 ⁷ | 2.10 ⁷ | 3.10 ⁷ |
| Termal cond. λ (W.cm ⁻¹ .K ⁻¹) | 1,3 | 0,54 | 5 | 5 | 5 | 1,3 | 20 |



Maximum allowed R_{Th} for $2.4 \times 2.4 \text{ mm}^2$ JFET





J. M. Hornberger, E. Cilio, R. M. Schupbach, A. B. Lostetter, and H. A. Mantooh, "A High-Temperature Multichip Power Module (MCPM) Inverter utilizing Silicon Carbide (SiC) and Silicon on Insulator (SOI) Electronics," in *Proceedings of the 37th Power Electronics Specialists Conference (PESC)*. Jeju, Korea: IEEE, Jun. 2006, pp. 9–15.