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# Thermal stability of SiC JFETs in conduction mode

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## Keywords

« Thermal design », « JFET », « High temperature electronics », « Silicon carbide », « Reliability »

## Abstract

Although they can operate at elevated junction temperature, silicon carbide power devices can in some cases fail, even at low ambient temperature. This destruction mechanism, called the thermal run-away, is described in the paper. Then, the sensitivity of normally-on SiC JFETs (SiCED) to this mechanism is evaluated using a model based on experimental measurements performed over a wide temperature range (from  $-50^{\circ}\text{C}$  to  $300^{\circ}\text{C}$ ). It is shown that above a certain current level, run-away can occur. An experimental test bench is used to validate the modelling and explore the safe-operating area of these devices. The measurements confirm the sensitivity of the device to thermal run-away. Mitigation techniques are discussed.

## Introduction

Replacing classical, silicon-based power semiconductor devices with wide band-gap materials such as silicon carbide (SiC) allows for operation at a much higher junction temperature [1]. A possible benefit could be the reduction in size and performance of the cooling system required to keep the power devices within their permitted temperature range. However, a recent article [2] highlighted that, much like with silicon, SiC devices are prone to thermal run-away, even at moderated ambient temperatures.

This thermal run-away condition occurs when the heat dissipated by a device increases faster with its junction temperature than the cooling capability of its associated thermal management system. As this mechanism is dependent on the device behaviour with temperature, a specific evaluation is required for each device type. For example, in [3], it is shown that Schottky-Barrier Diodes are sensitive to thermal run-away, while the addition of a bipolar diode to form a Merged PiN-Schottky (MPS) diodes makes it more stable. In [4], a SiC MOSFET is studied. Although it is an unipolar device and should therefore suffer from the strong increase in dissipated power described in [2], the lowering of its gate-to-source

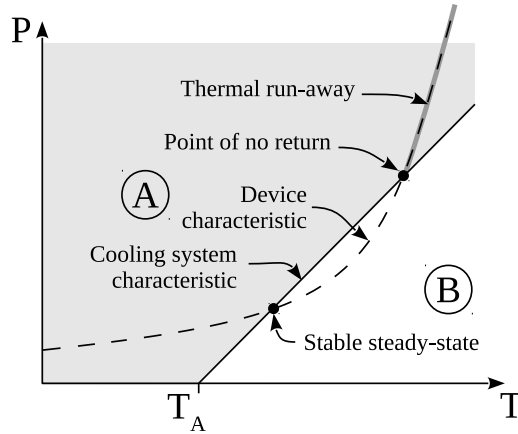


Figure 1: Plot of the power dissipated by an imaginary device as a function of its junction temperature (for a constant current). This highlights the equilibrium points, where the dissipated power is equal to the cooling system capability. One of these points is unstable, meaning that any increase in dissipated power will trigger the runaway mechanism.

threshold voltage with temperature opposes the increase in drain-to-source resistance and stabilises the device regarding run-away condition.

The present article describes a thermal run-away analysis performed on SiC-Junction Field Effect Transistors (JFETs). These devices are considered mature and suited to high junction temperature operation. It is therefore important to evaluate their thermal stability. The analysis will be limited to the conduction losses, which, as we will see below, have a strong sensitivity to the temperature.

In the first section of this paper, the principle of the thermal runaway mechanism is described. The second section presents the experimental characterization of an actual device (a SiC JFET from SiCED). Based on this characterization, a model is built (section 3) and is used to forecast the thermal runaway behaviour of the JFET. Finally, in section 4, these predictions are validated using a dedicated test bench, and the results are discussed in section 5.

## 1 Thermal runaway mechanism

A simple explanation of the thermal runaway mechanism is described in figure 1. We plotted on this graph the  $P = f(T_j)$  characteristic of a device (where  $P$  is the power dissipated in conduction mode, or conduction losses, and  $T_j$  is the junction temperature of the device) and that of a simple cooling system (a thermal resistance  $R_{Th}$  related to the ambient temperature  $T_A$ ). One can define two regions: in region A (grey area), the device dissipates more heat than the cooling system can extract. It will therefore heat up until it crosses the cooling system characteristic. On the opposite, in region B (white area), the device dissipates less power than its cooling system can extract, so it cools down.

An equilibrium (steady state) is reached when the device dissipation equals the cooling capability, that is when the “device” and the “cooling system” curves intersect. In the case depicted in figure 1, there are two such equilibrium points. Only the lower, however, offers a stable equilibrium: if, for some reason, the device temperature changes slightly, it will be attracted back to this equilibrium. For example, if the device becomes any cooler, it will enter region A and will therefore heat up. If it becomes hotter, it will reach region B and start cooling down.

The second equilibrium point (named “point of no return” in figure 1) is unstable: any minute change in device temperature will result in dramatic changes. In particular, if the device becomes any hotter, it will enter region A, dissipating more power than the cooling system can extract. If not interrupted, this ends in the destruction of the device (run-away condition).

A simple model for the JFET on-state behaviour is a drain to source resistance ( $R_{DS_{on}}$ ). If we consider that  $R_{DS_{on}}$  has the same temperature dependence as the resistivity of a uniformly-doped SiC layer [2], it

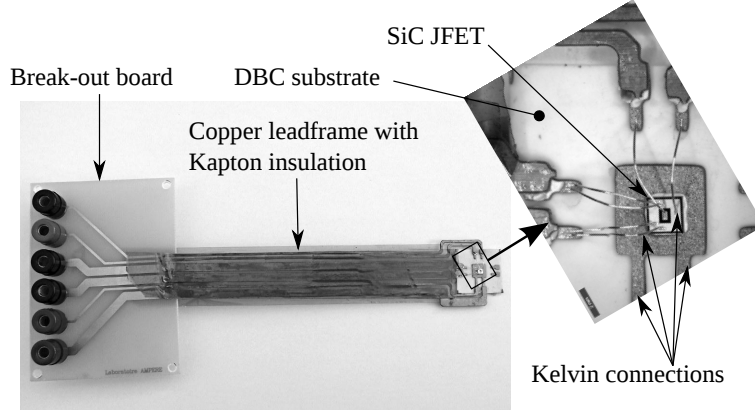


Figure 2: The test setup: a device is attached to a ceramic (DBC substrate), and the external connexions are provided by a copper leadframe and Kapton adhesive tape. All elements are attached using silver sintering. This test setup offers a high temperature capability.

is equal to

$$R_{DS_{on}} = R_{300K} \left( \frac{T_J}{300} \right)^{2.4} \quad (1)$$

With  $T_J$  the junction temperature of the JFET and  $R_{300K}$  the value of  $R_{DS_{on}}$  at 300 K. Therefore, for a constant drain current  $I_D$ , the power dissipated in the on-state is

$$P = R_{DS_{on}} I_D^2 = R_{300K} \left( \frac{T_J}{300} \right)^{2.4} I_D^2 \quad (2)$$

While the cooling capability of the thermal management system is

$$Q = \frac{T_J - T_A}{R_{Th}} \quad (3)$$

From (2) and (3), it can be seen that the device and the cooling system characteristics of the JFET should have similar trends as depicted in figure 1: the “cooling system” characteristic has a linear dependency on  $T_J$  (3), while the “device” characteristic (2) is dependent on  $T_J^{2.4}$ . This device should therefore be sensitive to thermal run-away.

## 2 Device Characterization

Several JFET dies (provided by SiCED) were mounted on a specific test fixture (figure 2), offering high temperature capability: dies and terminals are silver-sintered onto a ceramic substrate (DBC, with  $300 \mu\text{m}$ -thick copper tracks). The terminals are formed by a  $350 \mu\text{m}$ -thick leadframe providing kelvin connections to the drain and source of the JFET. Aluminium wirebonds are used between the top side of the die and the DBC substrate. This assembly was tested successfully at  $300^\circ\text{C}$  ambient temperature, and can in theory sustain a much higher temperature. All the data presented in this paper come from a  $2.4 \times 2.4 \text{ mm}^2$  die size,  $1200 \text{ V}$  JFET, which has a (measured)  $R_{DS_{on}}$  value of  $490 \text{ m}\Omega$  at room temperature. Once mounted on the test fixture, the direct I(V) characteristic of the JFETs was measured using a Tektronix 371A curve tracer in pulse mode, for junction temperature values ranging from  $-50$  to  $300^\circ\text{C}$ . The temperature was controlled by a Thermonics T2500-E temperature conditioner. As we focus on conduction losses, only the characteristic measured for  $V_{GS} = 0 \text{ V}$  (JFET fully-on) are used in this paper. This data is plotted in figure 3.

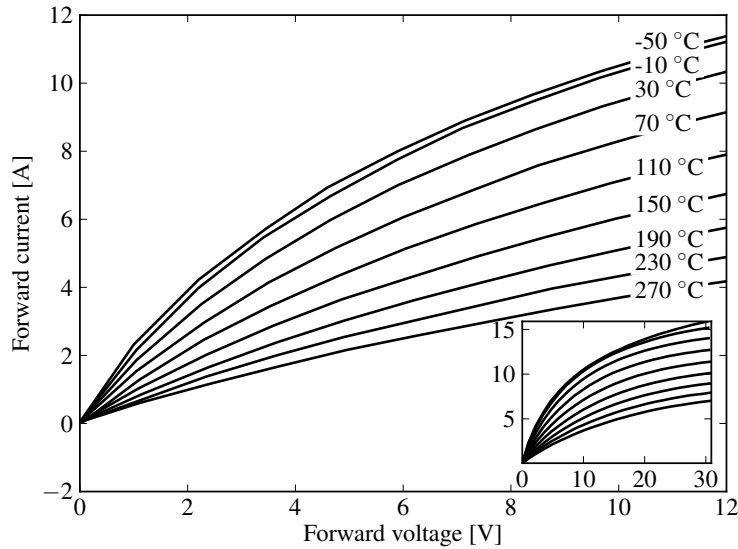


Figure 3: On-state characteristic, for a  $2.4 \times 2.4 \text{ mm}^2$ , 1200 V, fully-on SiC JFET from SiCED ( $V_{GS} = 0 \text{ V}$ ) as a function of temperature.

### 3 Thermal behaviour

We then fitted the data with a simple, empirical model  $I_D = f(V_{DS}, T_j)$  on the experimental data [5]. Using the model, we were able to plot a  $P = f(T_j)$  graph, much like that in figure 1, this time for several values of the drain current  $I_D$ . This can be seen in figure 4(a). The characteristics of several cooling systems (ranging from 1 to 8 K/W) are superimposed on figure 4(a). 1 K/W corresponds to a fairly efficient cooling system, and yet it can be noted that this cooling characteristic barely crosses the 8 A device characteristics. This means that there is no stabilization point above 8 A for this device at 1 K/W cooling efficiency. This is obviously dependent on the ambient temperature (which corresponds to the intersect between the cooling characteristic and the x-axis,  $T_A$  in figure 1). Any increase in ambient temperature will shift the cooling system characteristics to the right side of the graph.

Another representation of the same data is depicted in figure 4(b): here we plotted the maximum allowed thermal resistance as a function of the drain current, for three values of the ambient temperature. As an example, the junction-to-case thermal resistance of a device in a TO-220 package is in the order of 0.8 K/W. The SiC die alone has a thermal resistance of around 0.2 K/W.

### 4 Experimental Verification

To validate the predicted behaviour, we designed a test bench where the cooling system can be properly controlled (both its thermal resistance and the ambient temperature). The diagram in figure 5 presents the principle of the test bench: the test vehicle described in section 2 is thermally linked to a heatsink through an aluminium column. A temperature measurement is performed at a set location on the column, and a temperature conditioner keeps that temperature constant by adjusting the temperature of the air in contact with the heatsink. This corresponds to having an equivalent thermal resistance (the thermal resistance of the aluminium column) connected to a perfectly controlled temperature source (the temperature at point T). An adiabatic enclosure (vermiculite) ensures that no parasitic convection or radiation phenomenon can affect the thermal environment.

The test vehicle is then supplied with DC current, and the voltage drop within the die is measured using the kelvin connections. A picture of the test bench, without the adiabatic enclosure, is visible in figure 6. Using the JFET  $R_{DS_{on}}$  as a temperature-sensitive parameter, the equivalent  $R_{Th}$  was found to be 4.5 K/W. Three different ambient temperature values were studied: 13, 75 and 135°C. For each of them, the drain current of the JFET was gradually increased until it was no longer possible to reach a stable  $V_{DS}$ .

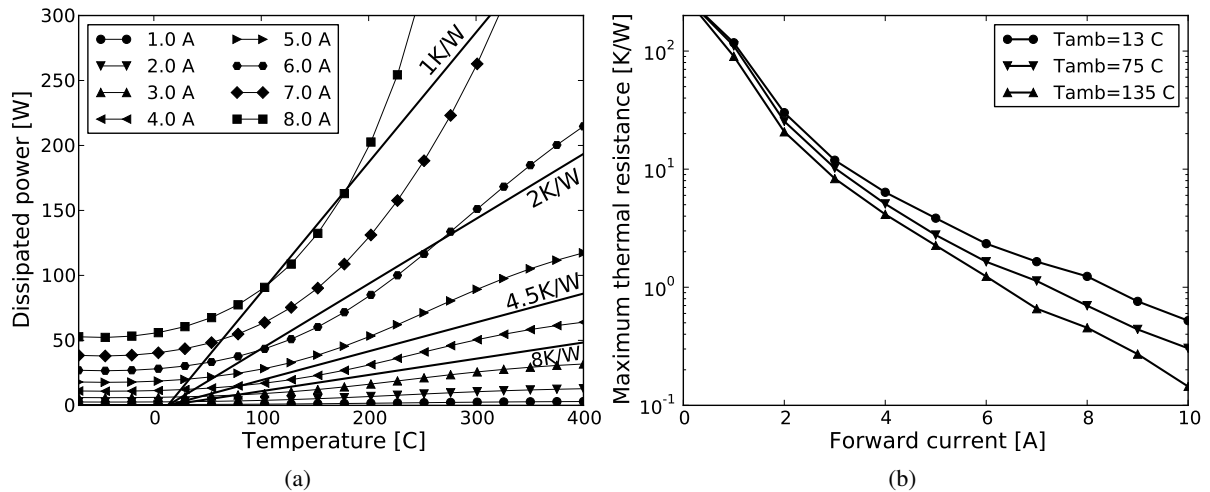


Figure 4: Dissipated power as a function of the junction temperature, for various drain current values, and thermal characteristics of 4 cooling systems (1 to 8 K/W) with an ambient temperature of 13°C (a). Maximum allowable thermal resistance as a function of the drain current, for three ambient temperatures (13, 75 and 135°C) (b).

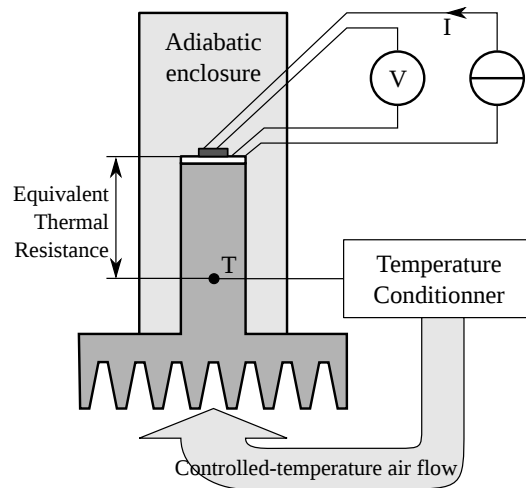


Figure 5: Principle of the run-away test bench

voltage within the limits of the power supply (set at 100 W maximum power). For each point, the drain current, the  $V_{DS}$  voltage (and therefore the dissipated power  $P = V_{DS} \times I_D$ ) were measured, using precision multimeters (Keithley 2700) and a shunt (Metrix HA0171). An oscilloscope was also used to monitor the time-domain evolution of  $V_{DS}$ .

The results are summarized in figure 7. The dots represents the power dissipation measured as a function of the drain current, in the cases where a steady-state operation point could be achieved. The dashed lines is the power calculated using equations (2) and (3).

The thermal run-away transient measured for one of the ambient temperatures values (135°C) is also presented (note that comparable run-away mechanisms were observed for 13 and 75°C). It can be observed that after the drain current was increased from 3.65 A to 3.7 A, the dissipated power could not reach a steady state. After 150-200 s of slow increase (corresponding to the thermal time constants of the test bench), the dissipated power suddenly exhibit a very steep rise, which is only limited by the capability of the power supply.

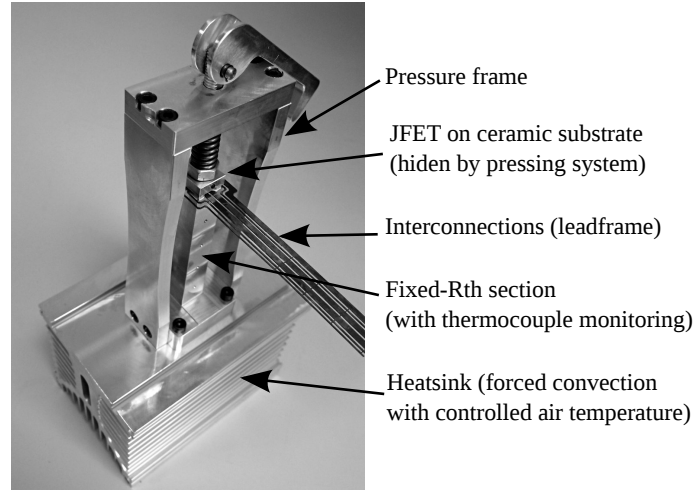


Figure 6: Picture of the thermal test fixture developed to host the JFETs assemblies of figure 2 for the final tests.

## 5 Discussion

Using the graph in figure 4(a), for an ambient temperature of 13°C and a thermal resistance of 4.5 K/W, it can be expected that the thermal run-away should occur between 4 and 5 A.

In the same conditions, the experimental results from figure 7 show that the thermal run-away occurs at a slightly higher current level (just above 5 A). This difference can be attributed to the accuracy of the analytical model that was used to plot figure 4(a), which tends to predict a slightly lower  $R_{DS_{on}}$  values than actually measured for temperatures below 30°C [5].

The comparison between the experimental power dissipation (the dots in figure 7) and the power dissipation computed using the temperature dependence of the resistivity of SiC (the dashed lines in figure 7) shows that the actual thermal run-away is triggered at slightly lower current values than expected. This is particularly clear for the 135°C ambient. The same difference was confirmed more clearly on more recent JFETs generations (results not presented here), and can be attributed to the added effect of the reduction of the saturation current with the temperature: as the junction temperature increases, there is an increase in the  $R_{DS_{on}}$  (the slope of the curves at  $V_{DS} = 0$  V in figure 3) and a reduction in the saturation current (the “plateau” in the inset graph of figure 3). Both result in an increase in  $V_{DS}$  at a given  $I_D$ . This means that eq. (2) only provides an approximation of the power dissipated by the JFET, which is actually higher.

In [2], the author predicts that this sensitivity to thermal run-away is common to all unipolar devices, because of the increase in electrical conductivity of SiC with the temperature, causing higher conduction losses. It should be stressed, however, that some were found not to exhibit such a large increase in conduction losses with the temperature. Some SiC MOSFET, in particular, were found to have a relatively constant  $R_{DS_{on}}$  over a large temperature range[4]. This can be attributed to the contradicting effects of the increase in material resistivity and the decrease in the threshold gate-to-source voltage of the transistor. Such phenomenon was described for Si MOSFETs [6]. For the JFET studied in the present paper, however, the threshold voltage was found to be constant ( $-18 \pm 0.5$  V) over a wide temperature range ( $-70$  to  $+300^\circ\text{C}$ ). As a consequence, the variation in  $R_{DS_{on}}$  of this JFET is dictated by the increase in electrical resistivity of the SiC, with no mitigating effect of the threshold voltage.

Although they are sensitive to thermal run-away, the SiCED SiC JFETs are still attractive devices, as they can operate reliably at high junction temperatures ( $>200^\circ\text{C}$ ). Furthermore, as visible in figure 7, the thermal run-away is controlled by thermal (i.e. relatively slow) time constants. It is therefore simple to integrate a safety mechanism in the gate driver that would shut down the system should the drain-to-source voltage of the JFET exceed a given threshold (exactly as the so-called desaturation protection that is found in gate drivers for IGBTs). The thermal run-away risk can be reduced further by de-rating the JFETs (using them at a lower current level) or by providing them with an efficient cooling system.

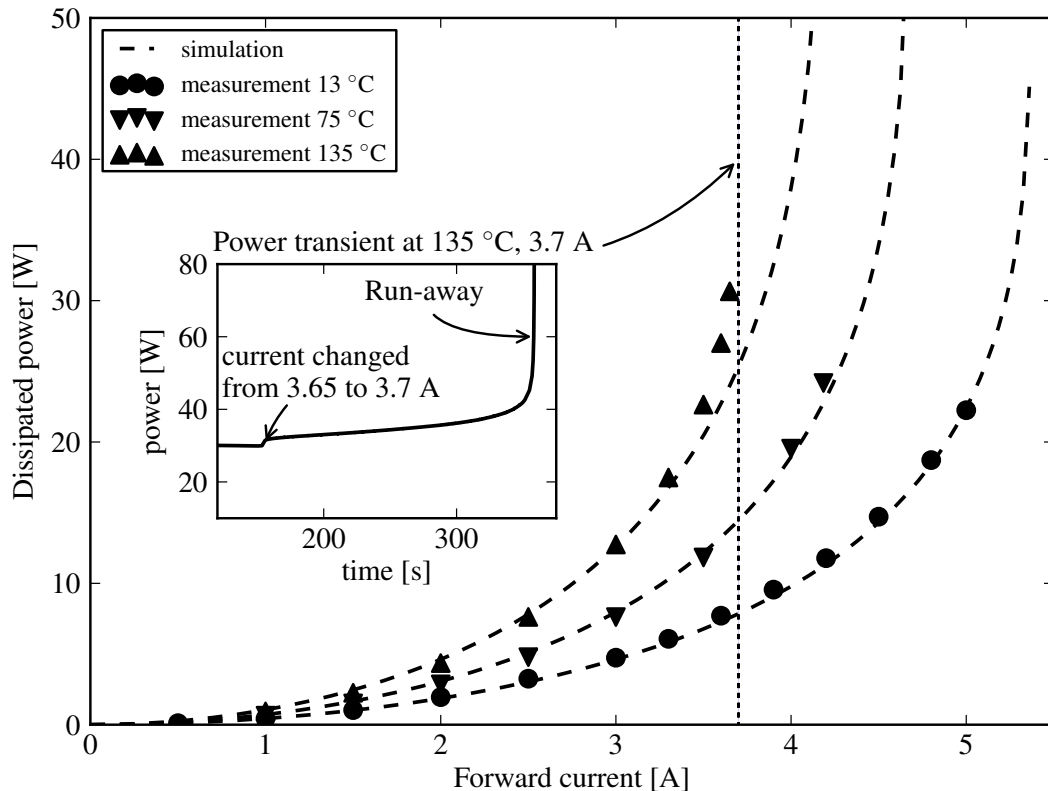


Figure 7: Measured conduction losses as a function of the drain current, for three ambient temperature and a thermal resistance, junction to ambient of 4.5 K/W. The inset graphs represents the temporal evolution of the power as a run-away condition occurs.

## 6 Conclusion

In this paper, we investigated the sensitivity of SiC JFETs (manufactured by SiCED) to thermal run-away. A first estimation showed that these devices are indeed sensitive to thermal run-away. This was confirmed using a dedicated test bench. Thermal run-away was found to occur at relatively low current levels, and at low ambient temperature.

It should be stressed, however, that this issue does not constitute a show-stopper for the SiC JFET, which remains attractive, especially for high temperature operation. It simply results in a set of precautions that should be taken to use these devices safely: proper thermal management, current de-rating and protection functions integrated in the gate driver.

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