Design and Implementation of Integrated Common Mode Capacitors for SiC JFET Inverters

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***Abstract*—This paper deals with the issue of electromagnetic interference (*EMI*) in *SiC-JFET* inverter power modules, and proposes a solution to limit conducted emissions at high frequencies. *SiC-JFET* inverters can achieve very fast switching, thereby reducing commutation losses, at the cost of a high level of *EMI*. In order to limit conducted *EMI* emissions, it is proposed to integrate small-value common mode (*CM*) capacitors, directly into the power module. High frequency noise, which is usually difficult to filter, is then contained within the module, thus keeping it far from the external network. This approach is in line with the current trend towards the integration of various functions (such as protection, sensors or drivers) around power devices in modern power modules. To demonstrate this concept, the resulting CM noise was investigated, and compared with a standard configuration. Simulations were used to design the integrated capacitors, and measurements were carried out on an experimental *SiC-JFET* half-bridge structure. A significant reduction was achieved in the experimentally observed *CM* conducted emissions, with a very minor influence on the switching waveforms, losses and overall size of the system. The benefits and limitations of this design are discussed, for the case of mid-power range inverters for aircraft applications.**

***Index Terms*—Electromagnetic compatibility, Inverters, Multi-chip modules.**

I. Introduction

WIDE-bandgap semiconductors are now reaching a satisfactory level of maturity for power devices. Their performance and capabilities are very useful and promising for very high efficiency, high temperature or high voltage applications [1]. Among wide-bandgap materials, the most technologically advanced is Silicon Carbide (*SiC*). Beyond their primary power-switching applications, such power devices require an appropriate converter design. Drivers, filters, packaging and various other elements need to be updated, in order to meet the specifications arising from new fields of application. The aerospace industry is now studying these technologies, with the aim of improving avionics and energy management, which would ultimately allow "more electrical" aircraft to be built. By combining the advantages of *SiC* power devices with improved electronic integration, the concept of the "Smart Electro-Mechanical Actuator (*EMA*)" has been developed, as illustrated in Fig. 1. With this type of configuration, the converter is mounted directly on the actuator. When compared with conventional aircraft applications in which adjustable speed drives are used, there is no output *EMI* filter or harness on the *AC* side of the circuit. Despite its reduced filtering potential, the inverter must be capable of fast switching, whilst at the same time producing a low level of *EMI*. The solution proposed in the present paper was designed for this type of configuration, which is encountered mainly in embedded power systems.

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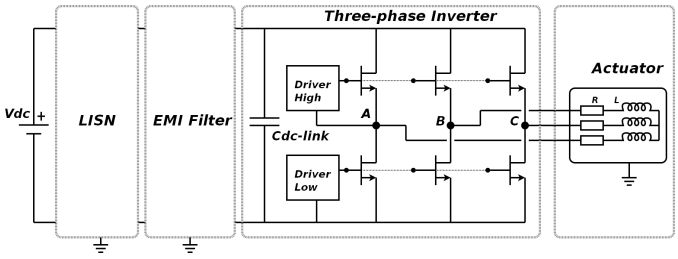

Fig. 1. Electrical diagram of an adjustable speed drive including a *LISN*, generally referred to as a "Smart Electro-Mechanical Actuator (*EMA*)

A. SiC Power Converters

1) SiC Power Devices: SiC devices have recently become commercially available items. Because they can operate at junction temperatures as high as 450 °C [2], it has now become possible to improve their power density by decreasing the size of the heatsink. Alternatively, a given power device operating range can be achieved at higher temperatures. On the other hand, lower switching losses allow higher switching frequencies to be used, thus leading to a decrease in the volume of the passive energy-storage components. Several high-density converter designs using *SiC-JFET* devices have been demonstrated [3], [4], and the building blocks for high ambient temperature, *SiC-JFET* inverters have been described by [2], [5]. The topologies of these devices correspond mainly to inverters and synchronous rectifiers, for aircraft or photovoltaic applications [6]. Moreover, it is noteworthy that the *JFET* appears to be the most mature and robust *SiC* power switching structure at the present time [7].

2) Electro-Magnetic Compatibility (EMC) Issues in Adjustable Speed Drives: The differential mode (*DM*) current and voltage are confined to the power loop, and depend strongly on the switching frequency. The *DM* current is filtered mainly by a line inductor and the *DC*-link capacitors in the voltage switching inverters (*VSI*). The *CM* current flows from the power lines through parasitic impedances to the ground, and is produced by high rates of change in voltage (dv/dt) which occur during switching. The *CM* noise is the main

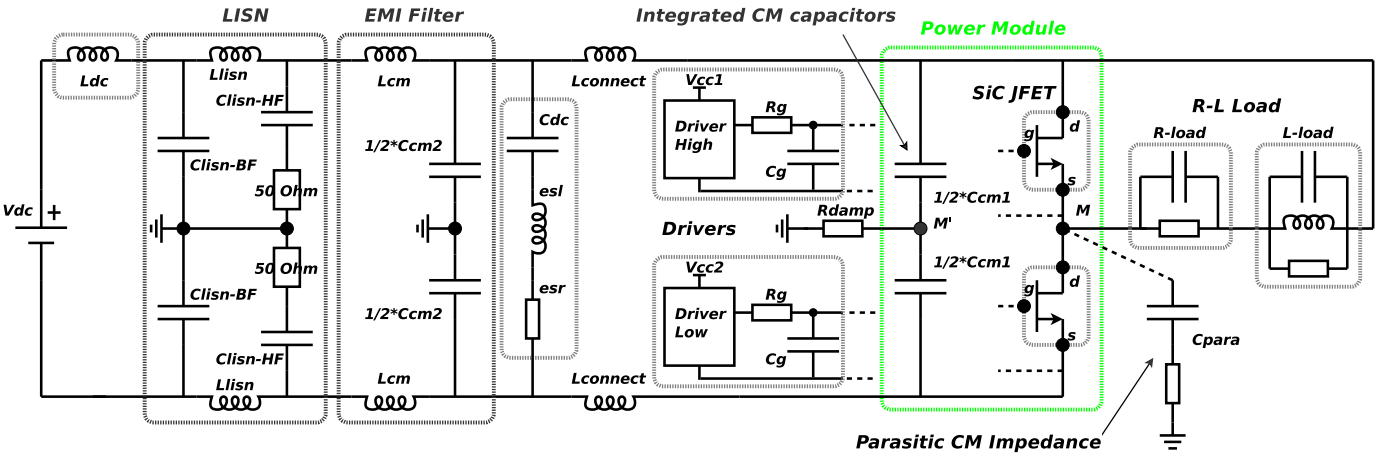

Fig. 2. Electrical diagram of the phase-leg inverter and *LISN*, including the *CM* impedances. Note that although the stray inductances and resistances of the power module are not represented, their influence was taken into account in the simulation, as described in section III-A3.

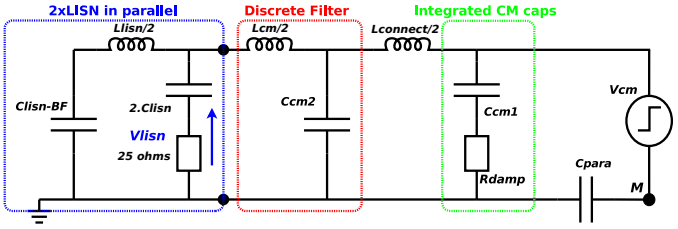

Fig. 3. Common Mode equivalent circuit of a "Smart Electro-Mechanical Actuator (*EMA*)" with a *LISN*. Vcm is the *CM*-equivalent noise source, and $Cpara$ is the *CM*-equivalent parasitic capacitance. This circuit was derived from that shown in Fig. 2, in which only the *CM* path, from point M to the ground, is considered.

contributor to high frequency conducted emission [8]. The main issues to be dealt with are the electromagnetic field radiated by long cables, bearing currents, winding insulation stress close to the actuator, and cross-talk with the control signals. Due to the considerable mass and volume of the converter, optimization of the *EMI* filter is a critical issue for avionics.

The switching speed of *SiC-JFET* devices is 2 to 10 times higher than that found with *IGBT*-based inverters [9]. This leads to higher dv/dt and di/dt transients, which in turn produce stronger, wide-bandwidth *CM* noise. It is also important to bear in mind that in a "Smart *EMA*" topology, no output filter is used on the *AC* side of the device. It is thus essential to make use of a suitably designed *EMI* input filter [10], [11], [12], to protect the electrical network from CM noise generated by the converter, and transmitted through the cable and the electrical machine.

B. Presentation of the Proposed Power Module Concept

1) Towards an Integrated Power Module: Today, considerable research activity is devoted to the integration of power converters, with the aim of improving power density, efficiency or standardization. Although a significant effort has been made in the field of input filter development [13], [14], [15] in the mid-power range, i.e. between approximately 1 and 50 kW, a discrete filter is still required for adjustable speed drives. The design presented in this paper extends the filtering capabilities of a discrete input *EMI* filter, allowing it to cope with the greater noise levels produced by the fast commutations of *SiC* power devices.

As has already been proposed by [16], we present a design in which *CM* filtering capacitors are integrated directly into the power module. The aim of this approach is to allow fast commutation, whilst at the same time ensuring high-frequency *EMI* containment. Since the high-frequency noise is generated by power switches, and the capacitors are located close to these components, only small capacitances are needed. Since most of the *CM* current should be "recycled" and contained within a closed loop, lower *EMI* noise levels can be expected from a *SiC-JFET* inverter, without taking up an excessive amount of space in the power module.

As shown in the circuit of Fig. 2, and in the *CM*-equivalent circuit of Fig. 3, an additional filter stage is created for high frequency filtering. This stage is composed of the integrated capacitors, $Ccm1$, and the stray inductances, $Lconnect$. In association with the discrete filter, the integrated *CM* capacitors take advantage of the stray inductance of the conductor between the discrete filter and the power module. Thanks to the additional noise reduction achieved by the use of integrated *CM* capacitors, a simple design can be found for the discrete input filter. With a standard (i.e. unfiltered) power module, a higher-order input filter would be required to cover the complete frequency range.

2) Methodology: The present study is dedicated to adjustable speed drives operating in the mid-power range. In order to provide a demonstration of this concept, the study focused on the design of a half-bridge inverter, also known as a phase-leg inverter. The results could easily be extended to three-phase *VSI* or synchronous rectifiers.

The present paper is organized as follows: section II presents a customized power module in a standard configuration, without the integrated capacitors. The layout and packaging technologies are described. In section III, the module is modeled and tested under realistic three-phase *VSI* operating conditions. The model is validated, and simulations are used to determine the most appropriate value for the integrated

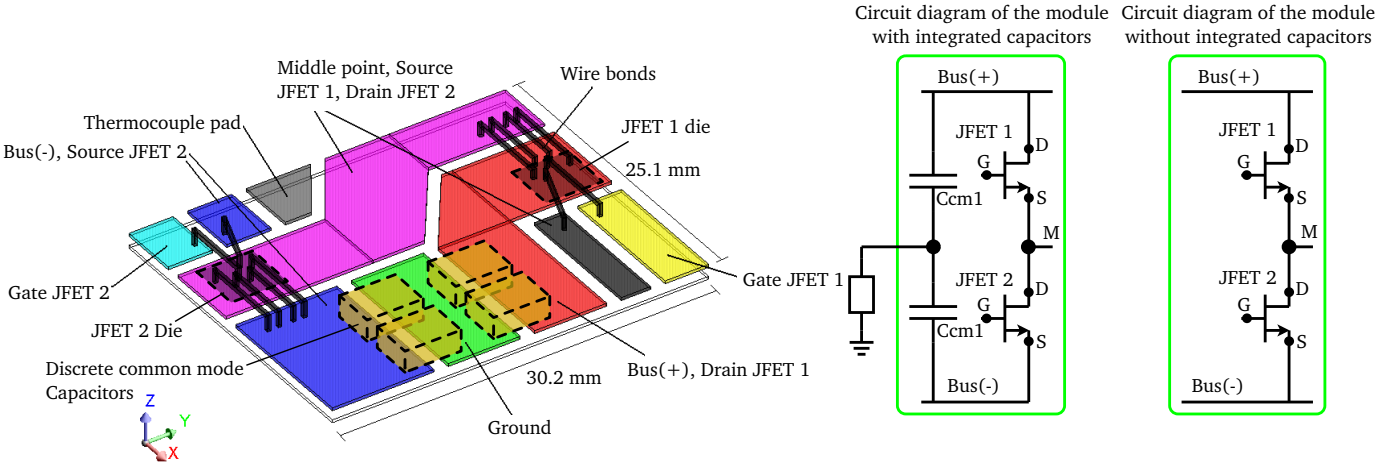

Fig. 4. Perspective view of the *SiC-JFET* power module used for *PEEC* modeling, and corresponding module circuit diagrams, with and without the integrated *CM* capacitors, as described in section IV. The position of the capacitors and JFETs can be seen in the perspective view.

CM capacitors, in terms of their benefits and impact on the inverter. Finally, in section IV, the integrated capacitors are implemented inside the power module. Two configurations were tested experimentally: the standard configuration and the *CM* configuration, involving the use of integrated *CM* capacitors. The results are then analyzed and discussed. The aim of this approach is to experimentally determine the impact of the CM capacitors on the power signals, control signals and *EMI*.

II. Description of the Power Module

A power module, intended for applications in a phase-leg inverter topology, was specifically designed for this study. A significant effort was devoted to this aspect of the design, in terms of packaging and manufacturing technologies. High temperature resistance and low parasitic effects are required, as a result of the high junction temperature and high switching speed capabilities of the *SiC-JFET*. Thermal and electrical considerations are the most important aspects of the power module design: thermal management is dominated by the packaging technologies, whereas the electrical characteristics are more strongly related to the layout and characteristics of the power devices.

A. Packaging Technologies

A conventional assembly was selected for the power module, with the ability to withstand high junction temperatures, since the *SiC-JFET* has a high junction temperature capability (up to 300 °C). The temperature limitations of the design were driven mainly by the secondary passivation of the die and the solder joint. An additional requirement was imposed by the maximum operating temperature of the integrated *CM* capacitors (200 °C), since they share the same substrate with the power devices. A description of these packaging technologies is given in [17]. The dies were soldered with high-temperature solder, on an Al_2O_3 Direct-Bonded-Copper (*DBC*) substrate. The *DBC* substrate was comprised of a 635 μm-ceramic layer, which was co-fired with 200 μm-copper layers on both sides. Aluminum-wire bonds connected the top of the dies to the tracks of the *DBC*, for the gate and source contacts. Several 250 μm diameter wire bonds were used between the source of the *JFET* and the *DBC*, in order to reduce on-state resistance. Copper leads were soldered for the external connections. A silicone gel was applied as an encapsulant, for insulation purposes. At the end of the process, the module was attached to a low thermal-impedance heat sink, using a silver-loaded epoxy adhesive.

B. Power Module Layout

The power module layout shown in Fig. 4 represents a phase-leg inverter comprising two power switches. As the selected *JFETs* (further described in section III) have an intrinsic body diode with acceptable properties [18], [19], no external diode is used. The power module layout can thus be simplified by using only two dies. The current density where the power current flows into the tracks is approximately 5 A/mm^2. If it is assumed that cooling is achieved by conduction through the bottom layer of the *DBC*, the copper losses would typically be lower than 0.1 W/cm^2. When this value is compared with the losses in the power device, which are reported to lie between 100 W/cm^2 and 300 W/cm^2 for *SiC-JFET* power devices [20], it can be seen that the Joule effect inside the tracks is negligible. The large track width of the design, as well as the copper backside of the substrate, have the additional advantage of reducing stray inductances in the circuit.

A further consideration is the distance separating the power loop and control loop source contacts. Only one wire bond is used as a reference potential for the gate-to-source voltage, and four wire bonds are connected from the source contact to the negative *DC* voltage, inside the power loop. The clearance between the tracks is set to 1 mm, to provide insulation at voltages up to 1.2 kV. A thermocouple is included, to measure the temperature inside the power module.

In order to anticipate the integration of *CM* capacitors inside the power module, a track connected to the ground is included, as indicated by the green track in Fig. 4. After having modeled the power module and simulated its behavior and performance, the integrated *CM* capacitors were surface-mounted at the

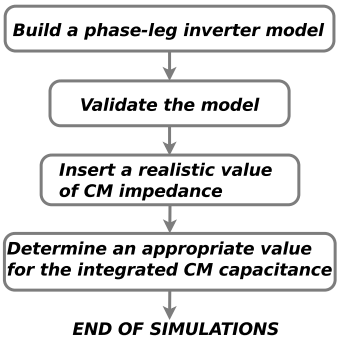

Fig. 5. Simulation procedure.

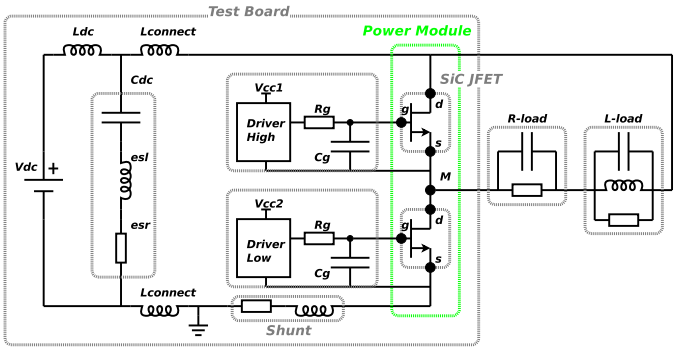

Fig. 6. Circuit diagram of the phase-leg inverter used to validate the model described in section III-A. This circuit diagram was used to simulate the waveforms shown in Figs. 8 and 10. Note that although the stray inductances and resistances of the power module are not represented here, they were included in the simulation described in section III-A3.

locations shown in Fig. 4. The same layout was used for all of the configurations described in this paper. The capacitor footprints increase the size of the module by 30 %, when compared to a "normal" power module, in this specific case. It should be noted that the phase-leg inverter with only two dies corresponds to the worst-case scenario. The applications for which this power module is intended are three-phase inverters.

III. Simulation Model and Analysis

Simulations were used to set an appropriate value for the integrated *CM* capacitors, referred to as $Ccm1$ in Fig. 3. The flow-chart of Fig. 5 illustrates the different steps required to simulate the phase-leg inverter. Before introducing *EMC* considerations into the simulation, a model based on a real setup was built. This model was then validated by comparing the results produced by the simulation with the measurements at a typical operating point, corresponding to 365 V and 4.2 A on the *DC* side of the module. Then, *CM* impedances representing a realistic *CM* path for an adjustable speed drive were added, and different integrated *CM* capacitor values were investigated and compared to the standard configuration (without the integrated capacitors). Finally, the most appropriate value in terms of *EMI* was selected for implementation into the power module.

A. Phase-leg Inverter Modelling

All of our simulations were run with Saber®, a circuit-simulation software using the *MAST* descriptive language. The

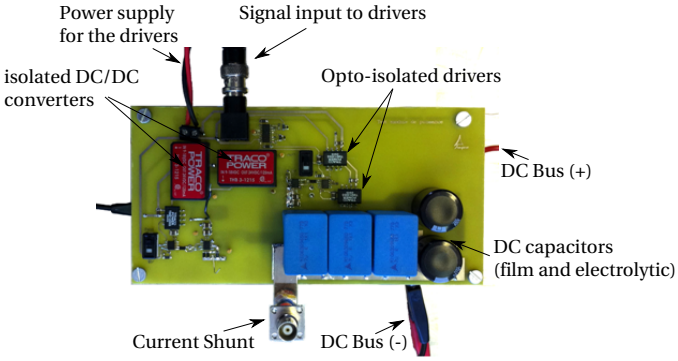

Fig. 7. *SiC-JFET* power module test board. The power module terminals were soldered directly onto the bottom layer of this board.

phase-leg inverter described in Fig. 6 was modeled from real elements, each of which is described in the following:

1) SiC-JFET: The 4x4 mm^2 *SiC-JFET* from Infineon was selected for this study. Its ratings are typically 1.2 kV and 15 A. Its on-state resistance is close to 80 $m\Omega$ at 25 °C, which is one of the lowest for this type of device. Its static and dynamic performances are evaluated in [9] and [20]. A multi-physics model of this device, described in [21], was used in the simulations. Parameter identification was based on its static electrical characteristics and capacitance measurements.

2) Gate Drive Circuit: A gate drive circuit was designed to meet the *SiC-JFET* requirements: in the off-state, the gate-to-source voltage, V_{gs}, must be lower than the pinch-off voltage, V_p, which is close to -18.5 V, and greater than the punch-through voltage, V_{pt}, which is nearly -27 V. With fast voltage transients at the middle point M, gate-drive interactions lead to voltage spikes on V_{gs} at the blocked *JFET*. As an example, if the upper *JFET* is off and the lower *JFET* is turning on, an interaction is observed on the upper V_{gs}. During turn-on, the spike is positive and the V_{gs} blocking voltage is increased, with the risk of a short-circuit occurring through the leg. In order to maintain V_{gs} in the off-state, between V_p and V_{pt}, the blocking voltage V_{gs} is set to -23.5 V and an additional 2.2 nF capacitor, C_g, is inserted between the gate and source potentials to prevent excessive interactions [22]. A 12 Ω-gate resistor, R_g, is chosen to limit gate-current spikes, whilst ensuring that fast switching speeds can still be achieved. The IXYS-IXDD09 Integrated Circuit (*IC*), designed for *IGBT* power modules, was used as a push-pull driver stage. Each gate drive circuit was supplied by an insulated *DC/DC* supply (the red blocks in Fig. 7). These DC/DC converters (Traco Power THB 3-1215) were selected for their low insulation capacitance (13 pF max.), which can be neglected when compared to the parasitic capacitances associated with the power circuit layout. The switching signals were transmitted to the gate drivers through Texas Instruments ISO721M high speed insulators, which also have a very low input-to-output capacitance (lower than 1 pF). In the model, the gate drive circuit was considered to be an ideal *PWM*-voltage source with a gate resistor, R_g and capacitor, C_g.

3) Power Module Layout: To take the influence of the coupling effects and stray elements associated with the conductors into account, a 3D model was built using the Par-

tial Element Equivalent Circuit (*PEEC*) technique [23] and the INCA3D® software. A perspective view of the layout is shown in Fig. 4. Potentials composed of phase inputs, transistor potentials, d, s and g, and the middle point M, are defined in the mesh. A matrix impedance, calculated at 1 MHz by the software, is provided by the model. The resistive and inductive components of the conductors (self and mutual inductances) were also modeled. The 3D model includes the wire bonds. The complete workflow, from the 3D description to the generation of a circuit model compatible with the Saber®software is described in detail in [24]. As this circuit model contains 32 ports (16 impedances and the coupling between any two of these), it is too large to be shown here. As an example, the stray inductance between the source terminal of JFET #2 and the DC(-) terminal (see fig. 4) was found to be 4.5 nH. None of the inductances exceeded a value of 9 nH.

4) Shunt: A 25 mΩ-coaxial shunt (T&M Research) was inserted in order to accurately measure the current across the lower *SiC-JFET*. Because of its low resistance compared to the on-state resistance of the *SiC-JFET*, and its low series inductance, measured at approximately 10 nH, the shunt has a very low influence on the dynamic response of the phase-leg. It can be modeled by an R-L equivalent circuit. All of the signals were referenced to the shunt during the time-domain acquisitions.

5) R-L Load: Adjustable speed drives are comprised essentially of a *VSI* and an actuator, which behaves like an inductive load. An 8 Ω power resistor and a 2.3 mH air inductor were used to test the phase-leg inverter. The air inductor is an excellent current source, which has linear characteristics since no magnetic material is used and it has a low parasitic capacitance. The latter were measured with an Agilent-4294A impedance analyzer, and the equivalent parasitic capacitances were estimated at respectively 9 pF and 17 pF, for the power resistor and the air inductor. Note that this constitutes a very simplified model of a machine, in which many phenomena have not been considered (non-linearity of the inductance, distributed parasitic capacitance…). This model was chosen for the purposes of comparison, since it can be more easily introduced into the circuit simulator.

6) Test Board: A test board was built in order to connect the various elements together, as shown in Fig. 7. The stray inductances resulting from the presence of the power leads and connections are modeled by the inductance, $Lconnect$, which was estimated to be 100 nH. This relatively large value is due to the position of the power module, which (for practical reasons) was installed approximately 20 mm below the test, resulting in a large switching loop. Decoupling capacitors, C_{dc}, were placed as close as possible to the power module, to limit the parasitic inductance of the commutation loop. Three 7 μF film capacitors were inserted in parallel. Using an impedance analyzer, the equivalent series resistance and series inductance were measured at respectively 10 mΩ and 10 nH. In addition, 450 V-100 μF electrolytic capacitors were inserted at the DC-link input, in order to filter the low frequency voltage ripple (these low-bandwidth capacitors were not taken into account in the dynamic modeling). Finally, a line inductor, Ldc, was inserted between the phase-leg and the power supply, to limit the current ripple. Ldc was rated at 500 μH when carrying a current of 5 A.

TABLE I
MEASUREMENT DEVICES AND SETTINGS

Device	*References*	*Settings*
Oscilloscope	Tektronix TDS744A	Average 30 acquisitions
Passive Probe x10	Tektronix 6139A	8 pF, calibrated
Diff. Probe x50/x500	Tektronix P5205	none
Current Probe 1 V/A	Tektronix TCP202	50 Ω, calibrated
Coaxial shunt 25 $m\Omega$	T&M Research SDN-414-025	50 Ω, 2 W

B. Model Validation

The operating point was chosen to be representative of an inverter functioning at a power level of a few kilowatts: the set points were thus 365 V and 4.2 A on the *DC* side and a switching frequency of 15 kHz, with a duty cycle of 36.6 %, was used at room temperature.

The instruments used during the tests are listed in Table I. A high-bandwidth oscilloscope and probes were chosen in order to measure the switching waveforms of the following signals: V_{ds}, V_{gs} and i_g. Only passive current and voltage probes were used for the acquisitions. The differential voltages computed from two voltage measurements using the P6139A, high-frequency probes were preferred. Because of its low *CM* immunity, the differential probe was used only to trigger the oscilloscope, or to measure differential voltages which were not subject to very fast and large voltage transients.

The results of the simulation and the experimental measurements, corresponding to the switching waveforms of the phase-leg inverter, are compared in Fig. 8 and can be seen to be in good agreement. The differences can be attributed mainly to errors introduced by the measurement devices themselves, and to parasitic effects such as parasitic capacitances, which are not included in the *PEEC* model. Some limitations also arise from the accuracy of the measurements carried out during the preliminary identification of the components. Nevertheless, the dynamic behavior of the converter can be seen to be well modeled. The commutation energy E, defined as the integral of V_{ds} x i_s during switching, is a good criterion for validation of the model. The energies E_{on} and E_{off}, measured at respectively 202 μJ and 164 μJ, and predicted as 206 μJ and 182 μJ by the simulations, are thus consistent. At this stage, the phase-leg inverter model is thus considered to be validated.

C. Addition of Common Mode Impedances

Following validation of the phase-leg inverter model, the simulations were extended to study the influence of the integrated *CM* capacitors. Realistic *CM* impedances were introduced into the model, and the influence of a range of *CM* capacitance values was studied. The full model, including the *CM* impedances, is shown in Fig. 2 and described in the following. The values of these elements are listed in Table II.

An important point to be considered is the modification of the (ground) reference. In a standard *EMC* setup, the reference

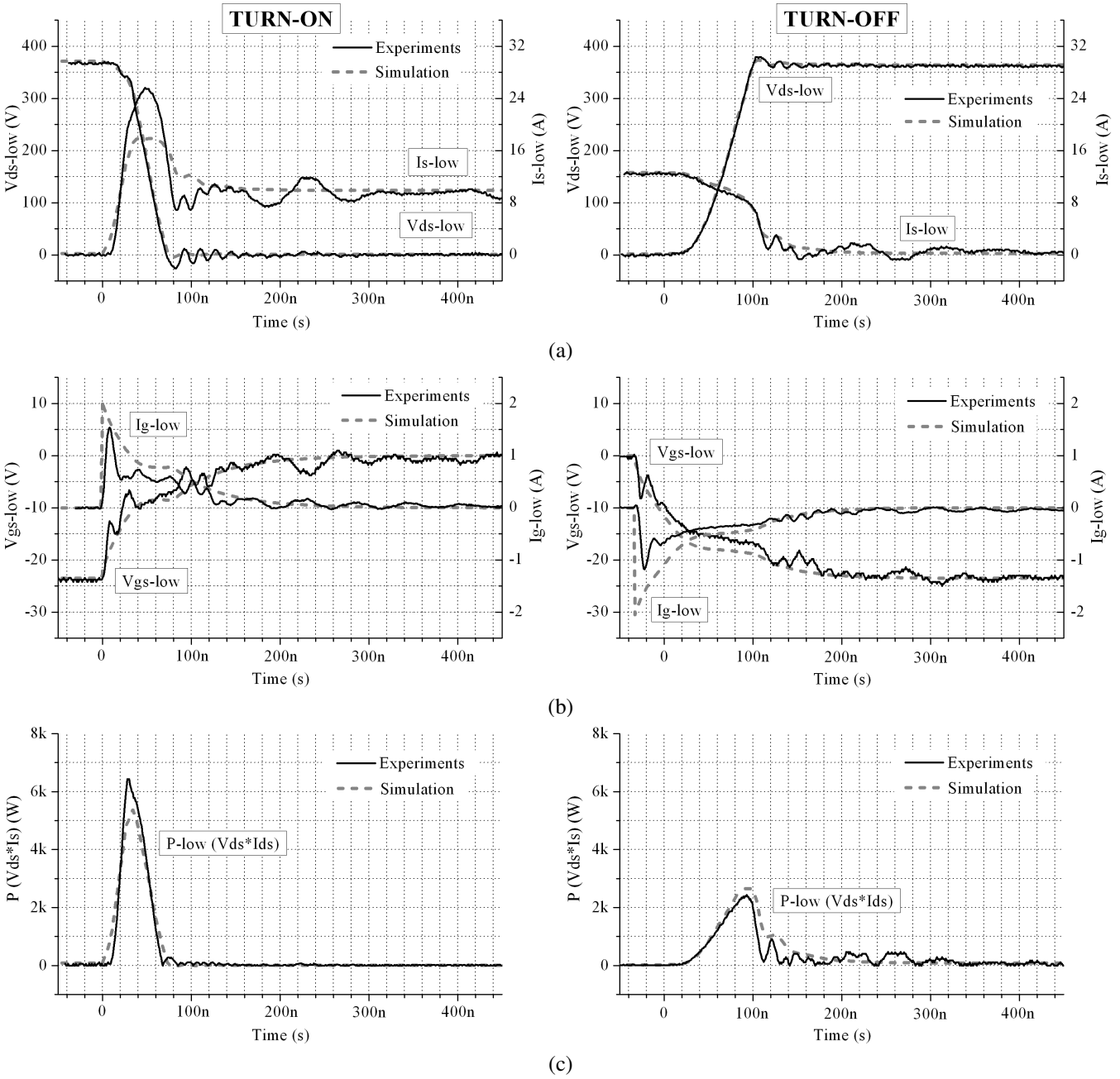

Fig. 8. Comparison between simulated and experimental switching waveforms at the lower *JFET* of the phase-leg inverter. (a) Drain-to-source voltage, V_{ds}, and source current I_s. (b) Gate-to-source voltage, V_{gs}, and gate current, I_g. (c) Instantaneous power, P.

is imposed by the Line Impedance Stabilization Network (*LISN*) and the copper ground plane. There is no particular difficulty with this in the simulation, since all of the signals can be accessed. However, in the experimental setup, the shunt is no longer the reference and it is not possible to accurately measure the source current. For example, at the lower *JFET*, i_s cannot be measured. The simulations are thus very useful when it comes to estimating the influence of the integrated capacitors, *CM*, on the losses.

1) Line Impedance Stabilization Network: EMI levels are defined by standards. Reproducible measurements are ensured by a *LISN* and a standard set-up for conducted emissions. The *LISN*, specified by the DO-160-F standard [25], was chosen.

TABLE II
PARAMETERS USED FOR THE CM-EQUIVALENT IMPEDANCES

$Parameters$	L	esr	epr	epc
Lcm	2.7 mH	50 $m\Omega$	9 $k\Omega$	30 pF
$Llisn$	5 μH	0.2 Ω	none	none
$Parameters$	C	esr	esl	$Damping$
$Cpara$	1 nF	1 Ω	none	none
$Ccm1$	1 to 10 nF	20 mΩ	10 nH	3 Ω
$Ccm2$	100 nF	50 mΩ	10 nH	none
$Clisn-HF$	280 nF	10 mΩ	60 nH	none
$Clisn-BF$	7 μF	100 mΩ	none	none

It was modeled with a realistic equivalent circuit, since at frequencies below 1 MHz its phase-to-ground impedance is

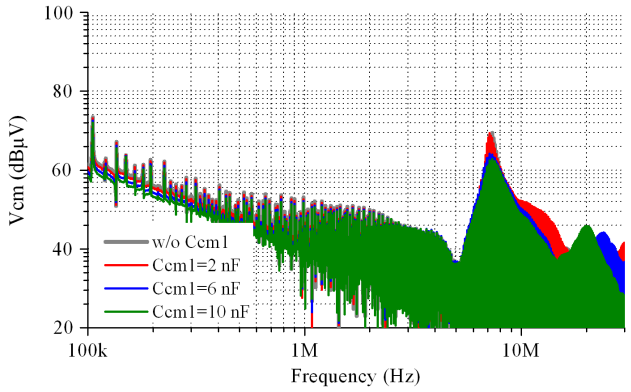

Fig. 9. Simulated *EMI* spectra for different values of the integrated *CM* capacitors.

less than 50 Ω. The frequency range to be considered was from 150 kHz to 30 MHz.

2) Discrete EMI Filter: The discrete *EMI* filter is a single-stage L-C filter. This filter was modeled by Lcm and $Ccm2$. Typical values for *CM* chokes, Lcm, are in the range of several mH. A 2.7 mH choke and two 50 nF ceramic capacitors were selected. The resulting cut-off frequency of the discrete filter was close to 10 kHz, i.e. below the switching frequency (15 kHz).

Because the *CM* emissions flow between the phases and ground, the overall capacitance is equal to the positive phase-to-ground capacitance plus the negative phase-to-ground capacitance. The *CM* capacitance values ($Ccm1$ or $Ccm2$) are thus twice as great as the physically implemented values. The integrated *CM* capacitance of 6 nF was physically composed of a 3 nF capacitance between the positive phase and ground, in addition to a 3 nF capacitance between the negative phase and ground.

3) Parasitic Common Mode Impedance: The parasitic *CM* impedance is mainly capacitive. In adjustable speed drives, this is created mainly by a long-shielded cable and/or the actuator, between the windings and the chassis. A typical value of 1 nF was chosen for the simulations.

4) Integrated Common Mode Capacitors: The integrated *CM* capacitance under investigation ranges between 1 nF and 10 nF. It was initially assumed that lower values would have no impact on the *EMI*. On the other hand, values greater than 10 nF would be difficult to integrate into the power module. The upper limit of the *CM* capacitance is also imposed by the required frequency range. In accordance with the aim of this study, the integrated capacitors must filter the high frequency noise. The bandwidth of larger capacitors, with larger values and larger parasitic capacitances, could also be a limitation. The parasitic capacitances chosen for the model were derived from real discrete and surface-mounted components. In addition, a damping resistor was inserted at the ground connection, in order to prevent excessive oscillations. Dissipation due to damping was considered to be negligible.

For the purposes of the simulations, the operating point and load and gate circuits were kept constant. Only $Ccm1$ was allowed to vary. In order to compare the *CM* emissions, the *CM* voltage at the *LISN*, defined in (1) by Vcm, was computed. $Vlisn1$ and $Vlisn2$ are the voltages across the 50 Ω termination impedances in Fig. 2. The *EMI* spectra of Vcm are plotted in Fig. 9 for $Ccm1$ equal to 2 nF, 6 nF and 10 nF. The frequency bandwidth under consideration ranges between 100 kHz and 30 MHz, since the range covered by the standards is 150 kHz-30 MHz [25]. The commutation energies are also compared in Table III. The simulation shows that there is no significant difference in the losses determined with the integrated *CM* capacitors.

TABLE III
COMMUTATION ENERGIES DETERMINED BY SIMULATION, FOR DIFFERENT INTEGRATED CM CAPACITOR VALUES

$Ccm1$	E_{on}	E_{off}	E_{total}
none	253 μJ	158 μJ	411 μJ
2 nF	246 μJ	162 μJ	408 μJ
6 nF	245 μJ	164 μJ	409 μJ
10 nF	242 μJ	162 μJ	404 μJ

$$Vcm(t) = \frac{Vlisn1(t) + Vlisn2(t)}{2} \quad (1)$$

The *EMI* spectrum is typical for an inverter. The *CM* noise is well filtered up to several megahertz, after which the attenuation of the discrete filter drops off, due to the presence of parasitic elements, whereas the noise is still high. Consequently, a spike appears with a significant amplitude. As initially assumed, the lowest value of $Ccm1$ (2 nF) does not lead to any decrease in the *EMI*, when compared to the case without integrated capacitors. When $Ccm1$ is equal to 6 nF, a 6 dBμV decrease is achieved for Vcm, at the highest spike, and a slight attenuation is observed over the whole frequency range. Up to a value of 10 nF, although Vcm is decreased by 1 to 2 dBμV, this is insufficient to compensate for the increase in capacitance, which is indirectly related to the footprint area. These results show that a capacitance of 6 nF provides a good trade-off between attenuation and the size of the integrated *CM* capacitors.

In Fig. 10, time-domain waveforms are compared for two different configurations: without the *CM* integrated capacitors, and with a 6 nF capacitance. The parasitic *CM* impedance produces source current oscillations at turn-on. These are reduced by the presence of the integrated *CM* capacitors, as a consequence of decoupling in *DM* mode. However, no significant difference is observed in the instantaneous power and control signals during commutation.

D. Conclusions on the simulations

The model was initially validated by measuring switching waveforms and losses, following which *CM* impedances were added. The simulations show that a value of 6 nF for the integrated *CM* capacitors provides a good trade-off between attenuation and the size and weight of the components. At high frequencies, close to 7 MHz, a 6 dBμV decrease in the *CM* voltage, Vcm, is achieved. This level of high frequency attenuation is useful, because the discrete filter is less effective

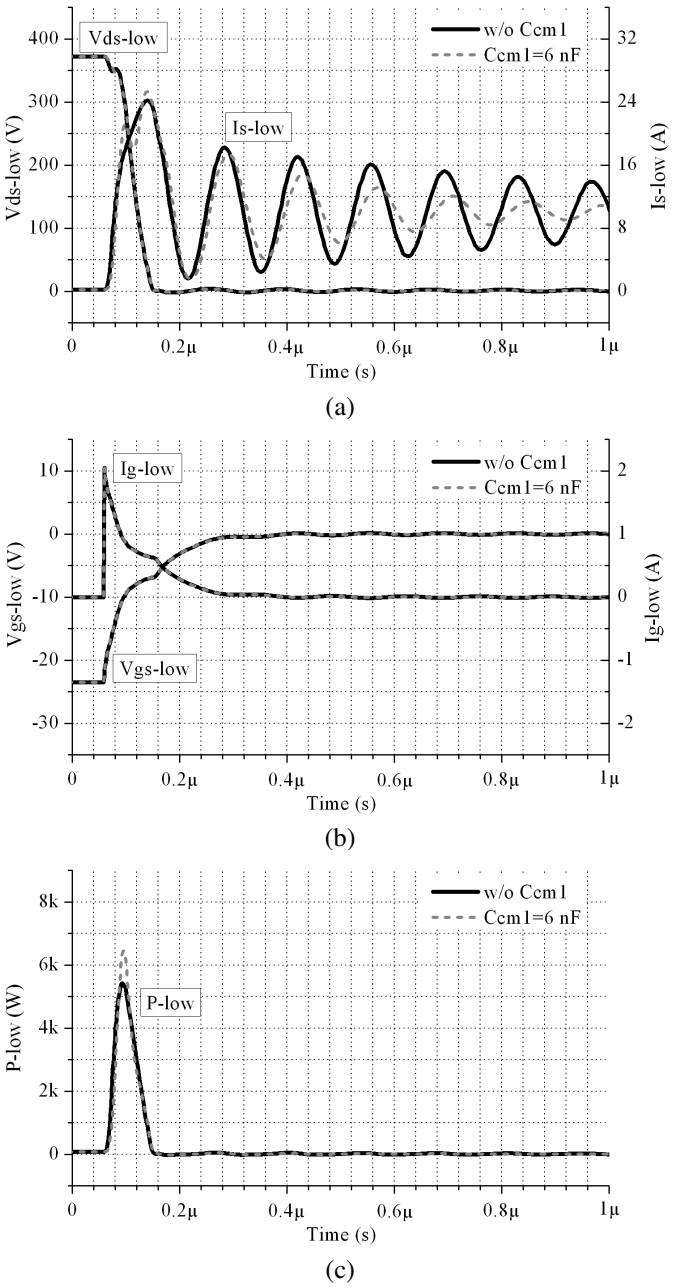

Fig. 10. Comparison between the simulated switching waveforms, during turn-on at the lower *JFET* of the phase-leg inverter, with no integrated *CM* capacitors, and using a 6 nF capacitance ($Ccm1$=6 nF). (a) Drain-to-source voltage, V_{ds}, and source current I_s. (b) Gate-to-source voltage, V_{gs}, and gate current, I_g. (c) Instantaneous power, P.

at high frequencies. The simulated switching waveforms also show that the integrated *CM* capacitors do not influence the switching losses and control signals. The concept of integrated *CM* capacitors is thus viable for implementation into a real power module.

IV. Experimental Validation

A. Prototype with integrated CM capacitors

In order to experimentally validate its simulated behavior, appropriate CM capacitors were integrated into the customized power module described in section II above. The resulting prototype layout is shown in Fig. 11. As described above (see section III-C-4), the value of 6 nF was selected for the integrated *CM* capacitors. These had to be placed as close as possible to the power devices, and connected to the ground. The ground potential was therefore introduced into the power module. High-temperature, NP0 Multilayer Ceramic Capacitors (*MLCC*), supplied by Presidio Components and rated at 500 V-1.5 nF, were selected. They were surface mounted and connected in parallel in order to obtain the required capacitance. The critical parameters of these capacitors, such as insulation resistance, capacitance and dissipation factor, are very stable over a wide range of temperatures, from -55 °C to 200 °C. It is interesting to note that capacitors with even higher temperature ratings (up to 260 °C) are available, and that technologies (film capacitors), which can be used at temperatures as high as 300 °C, are currently being developed [26].

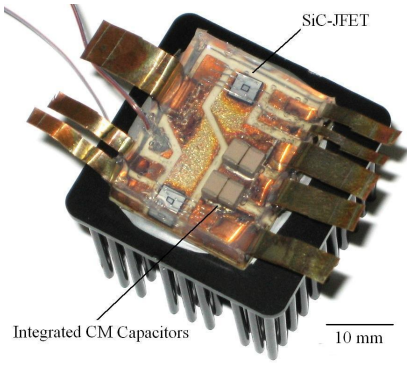

Fig. 11. *SiC-JFET* power module prototype with integrated *CM* capacitors.

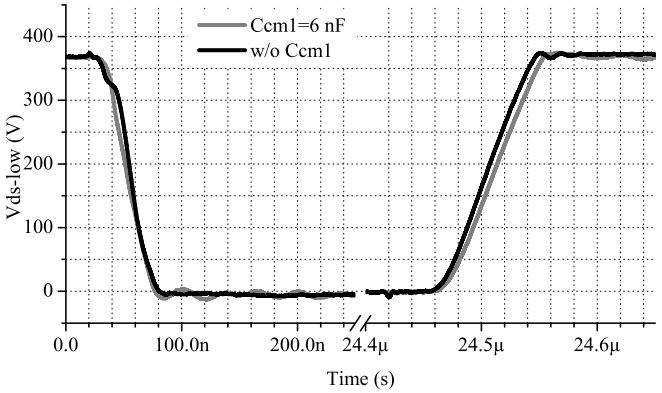

Fig. 12. V_{ds} at the lower *JFET* during turn-on and turn-off, for the two studied configurations.

B. Experimental Results

The experiments were carried out in a standard *EMC* setup (compliant with the DO-160-F standard) which consisted mainly in the *LISN*, provided by Solar Electronics (9403-5-PB-10-BNC), and the conductive ground plane. A 5-meter shielded cable, grounded at both ends, was used to introduce a parasitic *CM* impedance between the phase-leg and the load. For the purposes of comparison, the same operating point, set

TABLE IV
TEMPERATURE ELEVATION MEASURED INSIDE THE POWER MODULES AFTER 3MIN

	Ambient	w/o Ccm1	Ccm1=6 nF
Temperature	23 °C	37.7 °C	36.6 °C

to 365 V-1.7 A on the *DC* side, was used for all measurements and the converter was run continuously.

As shown in Fig. 4, two different cases were investigated: the standard configuration, without the integrated *CM* capacitors, and the *CM* configuration, with a 6 nF *CM* capacitance. The time domain waveforms were measured, to determine the influence of the integrated *CM* capacitors during switching. The drain-to-source voltages at the lower *JFET*, V_{ds}, were measured and compared during turn-on and turn-off, as shown in Fig. 12, in which the two measurements have been time shifted, to improve their readability.

As shown in Fig. 12, at turn-on the switching speed is increased by the presence of the integrated capacitors. The switching time was approximately 50 ns with the integrated capacitors, as opposed to 55 ns without them. It can also be noticed that in the absence of the capacitors, the V_{ds} waveform is disturbed by the parasitic inductance inside the commutation cell. This waveform is improved by the presence of the integrated capacitors, as a result of improved decoupling in the *DM* mode. This small change was predicted by the simulations, as shown in Fig 10-(a). At turn-off, no large over-voltage was measured on either of the V_{ds} waveforms. However, the switching speed was approximately 5 ns faster when these capacitors were not present. This result is consistent with the losses predicted by the simulations in Table III: the integrated *CM* capacitors reduce the losses at turn-on, but increase the losses at turn-off. This leads to equal losses for both configurations. The temperature measurements given in Table IV confirm this observation. The temperature increase inside the power module was measured with a thermocouple sensor, in order to compare the losses. Steady-state thermal conditions were achieved after three minutes.

Although the absolute increase in temperature was low, since the thermocouple did not measure the junction temperature directly, it provided a good means of comparing the losses with both configurations. In addition, the phase-leg inverter losses were very low, and the overall system-level efficiency was found to be nearly 98 %.

Fig. 13 compares V_{gs} and I_g, measured at the lower *JFET* during turn-on. Although the control signals were not strongly affected, it can be seen that I_g was slightly disturbed by the oscillations, and that V_{gs} followed almost identical curves in both cases.

The *CM EMI* emissions, defined in (1) by the term Vcm, were measured in the time domain at the *LISN*, and computed using a Fast Fourier Transform (*FFT*). When connected to the power module by means of coaxial cables, the oscilloscope served the purpose of a 50 Ω load. The time-domain variations of Vcm are plotted in Fig. 14, using two different time scales, and the frequency-domain spectra produced by the *FFT* computations are shown in Fig. 15. For the *FFT* calculations,

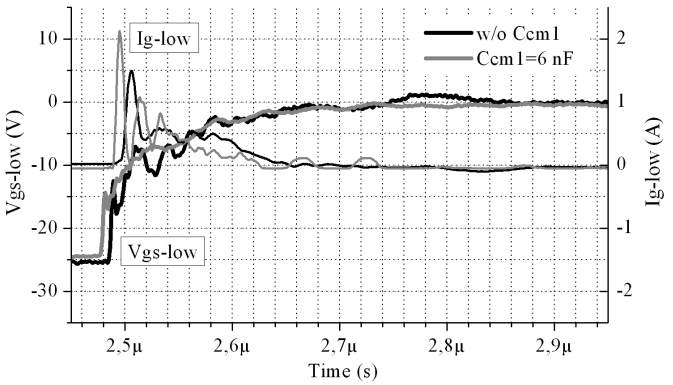

Fig. 13. V_{gs} and I_g at the lower *JFET* during turn-on, for the two studied configurations.

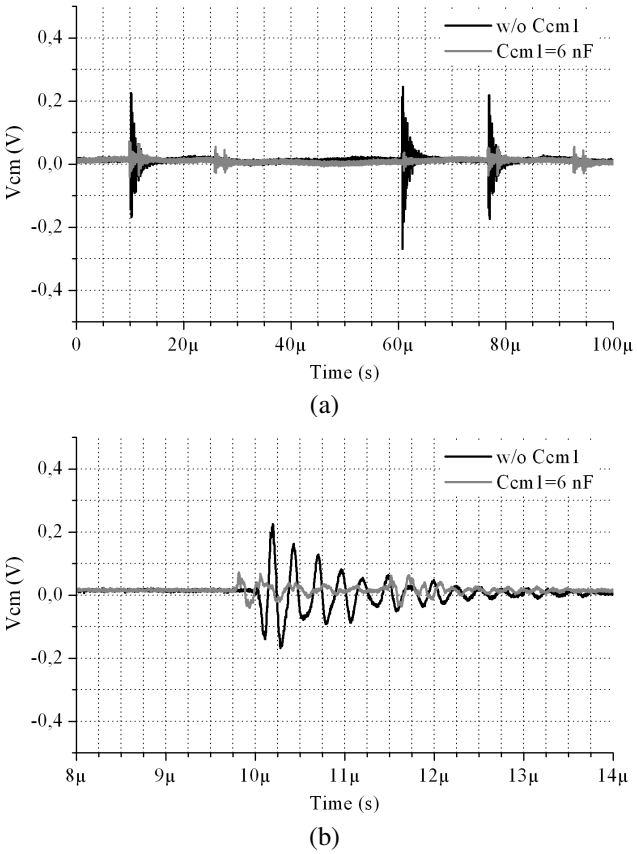

Fig. 14. Vcm(t) for the two studied configurations. (a) periodic time scale, (b) switching time scale at turn-on.

a total of 50,000 points were acquired by the oscilloscope, at 2 ns sampling intervals. The *FFT* was computed using a rectangular window. This approach led to an accurate determination of the harmonics present in the selected frequency range, between 100 kHz and 30 MHz.

In the time domain, a significant reduction in Vcm was achieved with the integrated capacitors. Fig. 14 shows that the spike amplitude was reduced by a factor of five, and the oscillation frequency was also reduced, as can be seen in Fig. 14-(b).

The same trends are reproduced in the frequency domain,

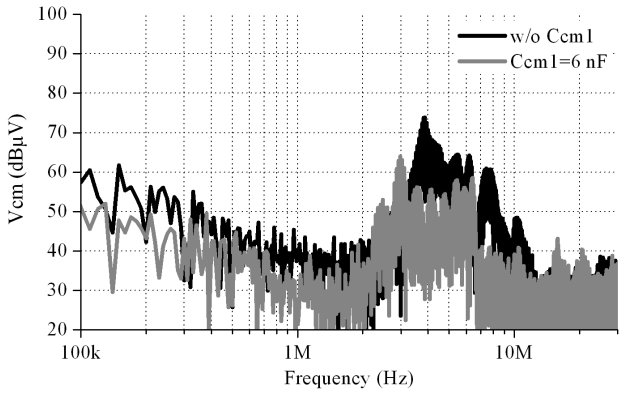

Fig. 15. *FFT* of Vcm(t), for the two studied configurations.

as shown in Fig. 15. The strongest spike observed with the integrated capacitors occurs at a lower frequency and a lower level, i.e. approximately 10 dBμV lower than the strongest spike observed without the capacitors. The additional high-frequency L-C stage, comprising the integrated capacitors and the stray inductance of the connections, also contributes towards improved attenuation at lower frequencies: a reduction of approximately 6 dBμV was measured between 100 kHz and 1 MHz. The measured *CM* attenuation was slightly greater than the value predicted by the simulations.

V. Conclusion

This study has demonstrated that a significant reduction in *CM* noise can be achieved at the *LISN*, by inserting *CM* capacitors directly inside the power module, as close as possible to the noise source. The design procedure, based on the use of simulation software, has been validated by experimental results. With appropriate modeling, such simulations can be used as an effective design tool.

The negative effects of the *CM* integrated capacitors on the system are very low, in terms of power switching waveforms, driver circuit, and power module losses. No prohibitive voltage spikes were measured during switching of the V_{ds} waveforms, the control signals were not disturbed, and the losses remained unchanged. Consequently, no additional constraints were added to the converter.

As initially expected, the concept of integrated *CM* capacitors makes it possible to achieve fast switching with low losses, and contained *EMI* at high frequencies. The use of additional integrated *CM* capacitors leads to an approximately 30 % increase in the size of the power module layout, when compared to a conventional design, and to the need for an additional copper grounding pad. However, in the case of a three-phase *VSI*, the overall impact of these modifications would be reduced, as a consequence of the greater surface area occupied by the dies. When compared to the alternative of adding a second L-C stage, the overall volume would nevertheless be reduced for a mid-power adjustable speed drive. This outcome is of considerable interest for aerospace applications.

Finally, the assembly technologies used to demonstrate this concept allow excellent performance to be achieved with *SiC-JFET* power devices. The authors are convinced that, in the near future, new generation converter packaging concepts, based on the use of wide-bandgap semi-conductors, will allow even greater benefits to be derived from the the concepts presented .

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