Physical Design Exploration of 3D Tree-based FPGA Architecture

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ABSTRACT

An innovative 3D physical design exploration methodology for Tree-based FPGA architecture is presented in this paper. In a Tree-based FPGA architecture, the interconnects are arranged in a mult-dimensional network with the logic unites and switch blocks placed at different levels, using a Butterfly-Fat Tree network topology. A 3D physical design exploration methodology leverage on Through Silicon Via (TSVs) using a horizontal break-point to re-distribute the Tree interconnects into multiple stacked active silicon layers proposed in this paper.

Categories and Subject Descriptors

B.7.1 [**INTEGRATED CIRCUITS**]: Types and Design Styles–*Advanced technologies*

Keywords

3D Integration Circuits, Tree-based FPGA, TSV

1. INTRODUCTION

Mesh is the most studied and used industrial topology. Considerable amount of research work [2] and industrial applications has already been implemented. One of the major disadvantage of Mesh-based FPGA architecture is, that the re-configurable interconnect consume almost 90% of the total die area [7]. The 3D integration technology has the potential to reduce the programmable interconnects length by bringing the logic components close together, which leads to significant improvement in performance and silicon die area. 3D integration is particularly useful to improve density and performance of FPGA systems. It can address problems pertaining to routing congestion, low resource utilization, long wire delays, thermal issues etc. This paper focus primarily on the development of physical design and exploration methodologies to develop 3D Tree-based FPGA, where the scope covers all activities of design and layout exploration.

2. RELATED WORK

A new FPGA creation is a challenging task because of the significant amount of time required for the design and validation. An automated layout design and verification tools for 2D Mesh-based FPGA reported in [4] shows that, a Mesh-based FPGA design process starting from design to tapeout is done with limited amount of time, however the tools reported to have a huge area penalty in cost of process automation. The electrical optimization of interconnect of an SRAM based 2D Mesh FPGA reported in [3] concludes that the best way to improve speed is to perform partial optimization on routing interconnect and remainder sections can be optimized for density. However this type of layout optimization leads to increase irregularity in interconnect design.

The interconnect and logic wiring requirements for 3D Mesh-based FPGA was reported in [7] and deals with 3D integration of Mesh-based FPGA with 3D switch blocks. However the vertical interconnections of switch box are assumed to be same as the wire length between two adjacent LUTs on the same layer may lead to unrealistic timing results. A design framework for 3D Mesh-based FPGA architecture level exploration methodology is presented in [8], to explore the vertical interconnect distribution, however this leads to usage of 2D and 3D switch blocks intermittently, which may lead to a number of design and manufacturing issues. In this paper, we present the issues associated to 2D physical design and propose a new 3D physical design exploration methodology for Tree-based FPGA in order to improve performance and density.

3. TREE-BASED FPGA ARCHITECTURE

A re-programmable Tree-based FPGA architecture is proposed in [5]. The main motivation for the Tree-based FPGA architecture is to achieve the best performance by balancing interconnect and logic block utilization, where logic blocks and routing resources are sparsely partitioned into a multilevel clustered structure [6]. In a Tree-based FPGA architecture, the LBs (Logic Blocks) are grouped into clusters located at different levels of the Tree. Each cluster contains a switch block to connect local LBs. A switch block is divided into MSBs (Mini switch Blocks). The Tree-based FPGA architecture unifies two unidirectional upward and downward interconnection networks using a *Butterfly-Fat-Tree* topology in order to connect DMSBs (Downward MSBs) and UMSBs (Upward MSBs) to LB's inputs and outputs.

4. PHYSICAL DESIGN EXPLORATION

The proposed methodology for physical design exploration of 3D Tree-based FPGA architecture is illustrated in Figure 1. The HDL generator is designed to generate VHDL

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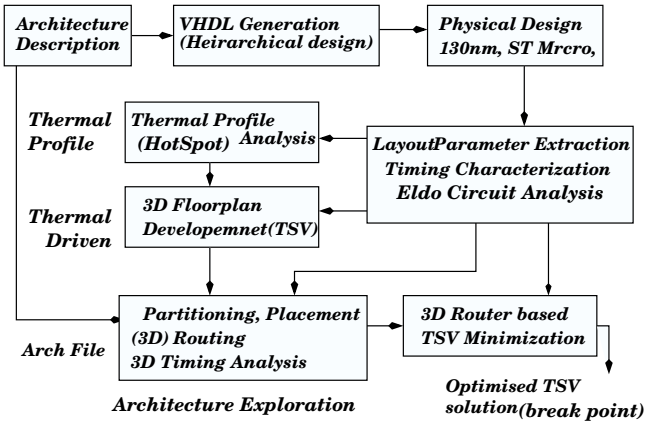

Figure 1: Physical Design exploration methodology

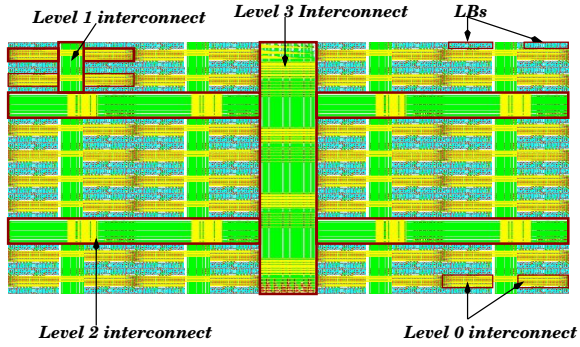

Figure 2: Tree-based FPGA with Arity 4: VLSI Layout of *3 level Tree*

code based on a hierarchical design approach that partitions the design into smaller sections, implement them separately and assemble them together at the final design phase. The physical design experiments are performed based on the layout generated using ST Micro's 130nm technology node. Figure 2 illustrates the layout of Tree-based FPGA with 3 tree levels. Mentor's circuit simulator *Eldo* is used to estimate the wire delay and power consumption of switches and interconnection networks at different tree levels. The thermal model presented in [1] is used to extract the thermal profile of the multi-layer chip based on layout geometrical features and power consumption of the functional unites.

To evaluate the performance of the proposed 3D Tree-based FPGA architecture, we place and route the largest set of MCNC[1] benchmark circuits, and compare with the 3D Mesh-based FPGA [8]. The performance analysis of 2D Tree-based FPGA layout versus 3D Tree-based FPGA with TSV design is presented in figure 3. The vertical axis shows the critical path delay measured for each MCNC benchmark design. It is evident from the graph presented in Figure 3, that for all designs the 3D implementation of Tree-based FPGA outperformed compared to the 2D counterpart. An average speed improvement of 68.7% is recorded in this experiment compared to our 2D design. The gain obtained in performance is due to the optimized wire delay at higher levels of the Tree interconnect by re-arranging them in the 2

[1]http://er.cs.ucla.edu/benchmarks/ibm-place.

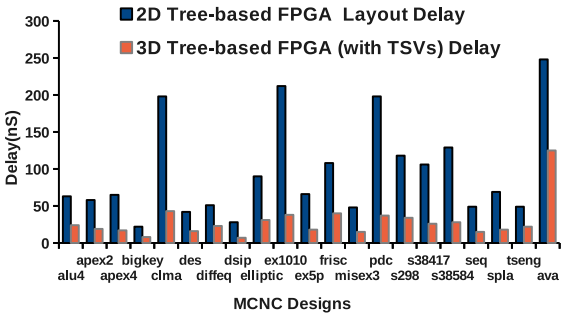

Figure 3: Performance analysis of 2D vs 3D Tree-based FPGA

layer 3D chip and using TSVs to connect *level 3 and 4*. The multidimensional nature of Tree interconnect offers more flexibility in 3D design compared to rigid nature of Mesh-based interconnect. This is the main reason for Tree-based FPGA to outperform in 3D implementation. Based on Figure 3, it is evident that the Tree-based FPGA is a consistent architecture for building 3D re-configurable systems.

5. CONCLUSION

A systematic physical design implementation methodology for 3D Tree-based FPGA is presented. The performance analysis reveals the 3D Tree-based FPGA has 68.7% advantage in performance compared to 2D Tree-based FPGA. This places 3D Tree-based FPGA as a viable alternative to build 3D re-configurable systems compared to 3D Meash-based FPGA.

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