

Designing 3D Tree-based FPGA TSV Count Minimization

V. Pangracious, Z. Marrakchi, H. Mehrez
UPMC Sorbonne University Paris VI, France



Presentation Outlook

Introduction : 3D Tree-based FPGA Architecture

- 1 Mesh-based and Tree-based FPGA architecture
- 2 Tree-based FPGA interconnect organization
- 3 3D Interconnect (TSV), Where to Add and How many ?

3D Tree-based FPGA Design and Optimization

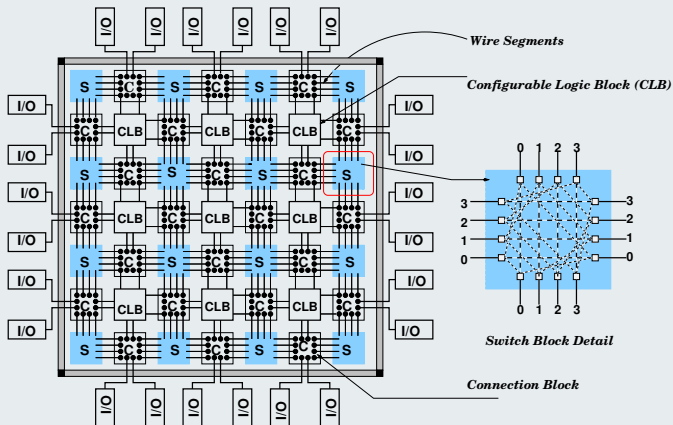
- 1 3D Design and TSV Count Optimization Methodology
- 2 3D Floorplan development, Timing Analysis

3D Tree-based FPGA Experimental Analysis

- 1 TSV Count Reduction and Performance Analysis
- 2 3D Tree-based FPGA Architecture Optimization
- 3 Interconnect Power Estimation

Industrial FPGA Architecture

Mesh-based FPGA : Industrial Architecture



- Most common Academic and Industrial Architecture

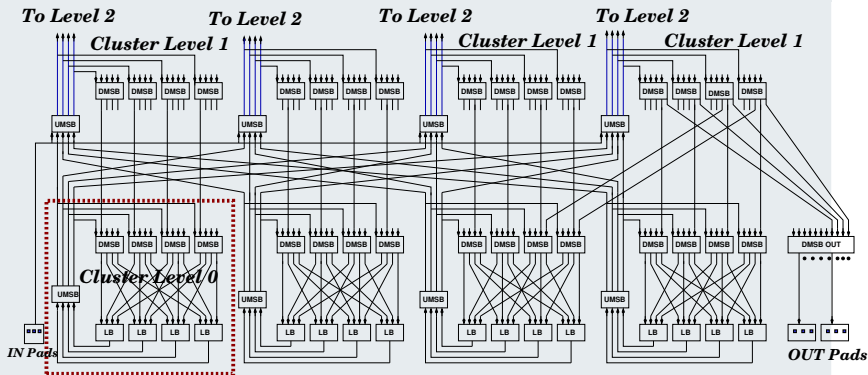
2D FPGA Statistics

2-Dimensional Mesh-based FPGA Statistics

- 1 Programmable Interconnects occupy 90% of the FPGA Area.
- 2 Contributes roughly 80% of the total path delay.
- 3 Contributes more than 60% of the total dynamic power consumption.
- 4 As a result, FPGA performance is significantly worse in terms of logic density, delay and power consumption compared to cell based ASICs.
- 5 Research studies have estimated FPGAs to be more than 10 times less efficient in logic density, 3 times larger in delay and 3 times higher in power consumption compared ASICs

FPGA Architecture

A Novel High Density Tree-based FPGA Architecture



An integrated upward and downward unidirectional programmable interconnect network using *Butterfly-fat-tree* network topology

Tree-Based FPGA Interconnect Network Organization

Upward Interconnection

- Upward Mini Switch Blocks
- Full crossbar switch

$$nbUMSB(\ell) = N_{in}(\ell - 1)$$

Downward Interconnection

- Downward Mini Switch Blocks
- Full crossbar switch

$$nbDMSB(\ell) = N_{in}(\ell - 1)$$

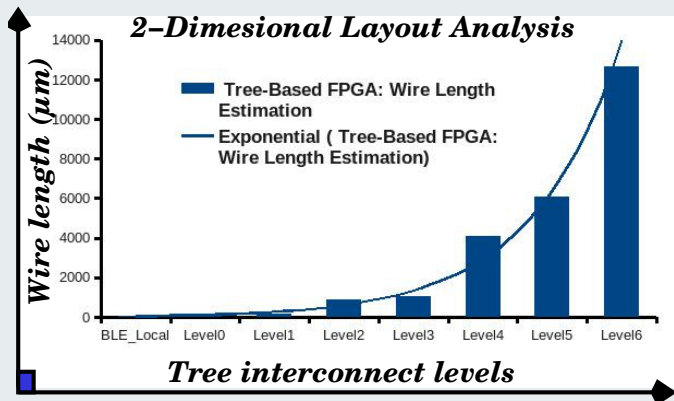
$$N_{switch}(down) = N \times (k^p c_{in} + k c_{out}) \times \sum_{\ell=1}^{\log_k(N)} k^{(p-1)(\ell-1)}$$

$$N_{switch}(up) = N \times k \times c_{out} \times \sum_{\ell=1}^{\log_k(N)} k^{(p-1)(\ell-1)}$$

N is the total number of logic blocks, c_{in} and c_{out} are the number of inputs and outputs of logic blocks, k is the arity, and p and ℓ are the Rent's parameter and level.

Tree-based Interconnect Length

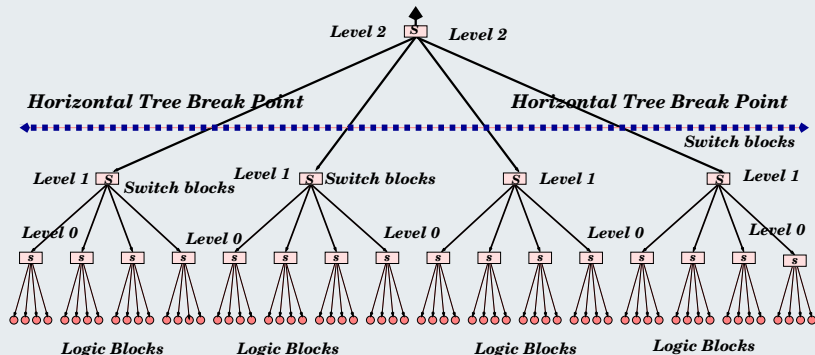
Wire length estimation of 2D Tree-based FPGA layout



Wire length increases exponentially as Tree grows to higher levels

3D Stacked Tree-based FPGA

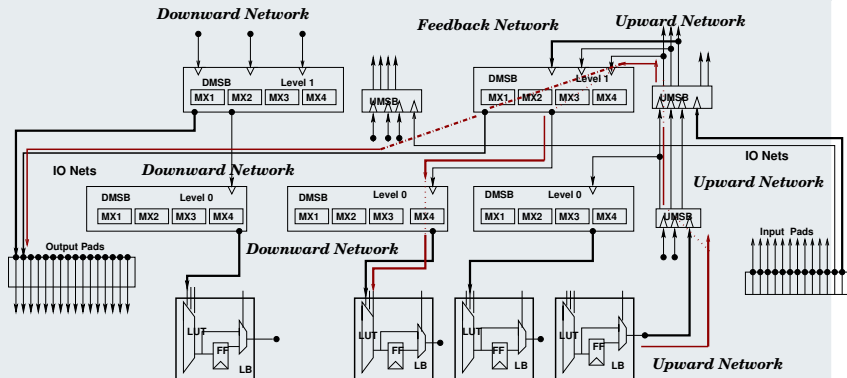
Horizontal Partitioning of Tree Interconnect



The network partitioning and location of the break-point is decided based on interconnect delay optimization.

3-Dimensional Layout Analysis

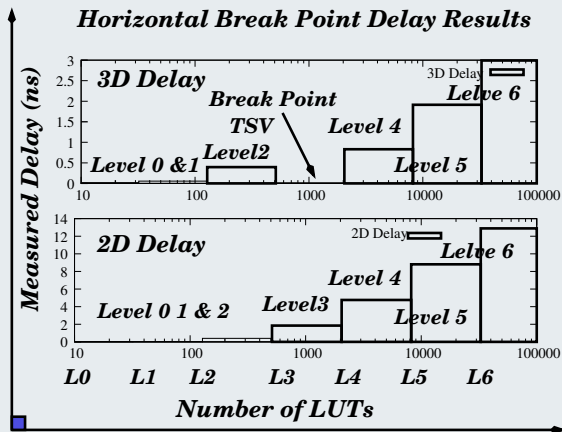
3D Layout Delay estimation



- ① Mentor's SPICE accurate circuit simulator *Eldo*.
- ② ST Micro's 130nm technology transistor models

3-Dimensional Layout Analysis

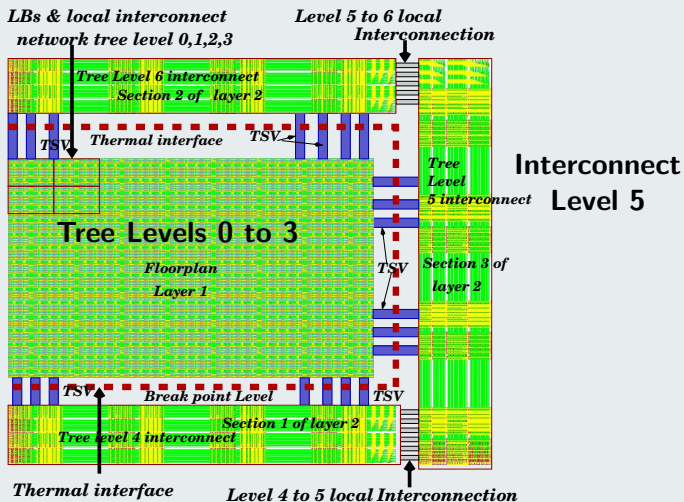
3D Layout Delay measurement setup



Re-organized active layer 2 (TSV placement) to optimize delay

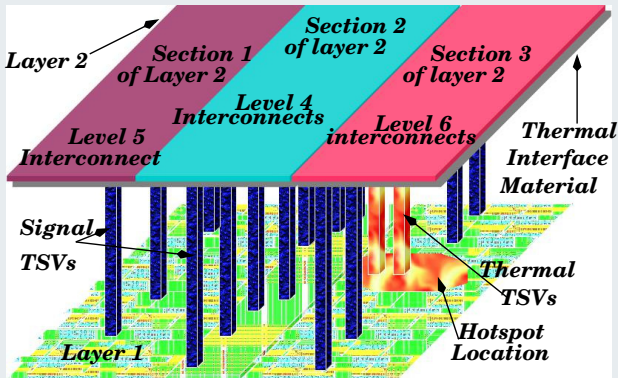
3-Dimensional Layout Design

3D compatible Tree-based FPGA Floorplan arrangement



3-Dimensional Layout Design

3D compatible Layout Design



2 layer 3D stacked Tree-based FPGA chip : Logic Units are placed in Layer 1 and Programmable Interconnects placed in active layer 2

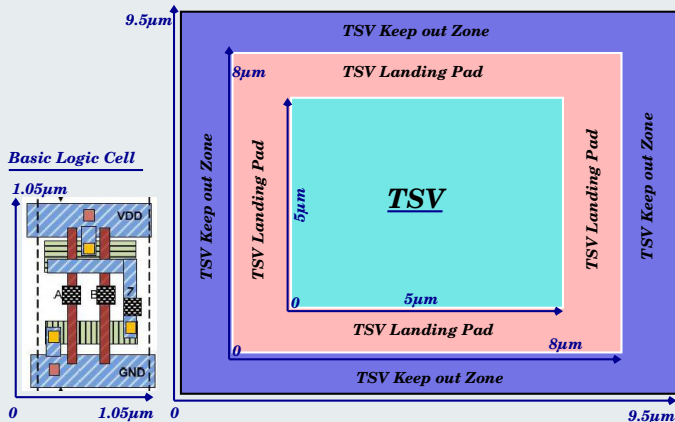
3D Physical Design, TSV Management

Where to Add and How Many?

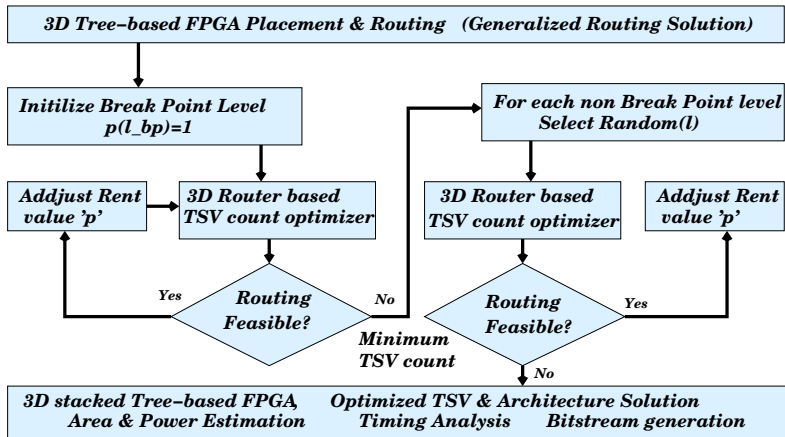
- 1 TSVs are huge and cause coupling
- 2 TSV count is crucial (Design, Manufacturing, cost) How Many?
- 3 TSV location is crucial (Design, Device, Performance) Where to place?
- 4 TSVs require design-for-testing, Power and Clock Delivery
- 5 TSVs require design-for-manufacturability/reliability
- 6 TSV Area and Power consumption Optimization
- 7 TSV density and impact of TSVs to local vias.

TSV Vs Logic Cells

TSV area Comparison with Logic Cells



TSV & Programmable Interconnect Optimization Flow



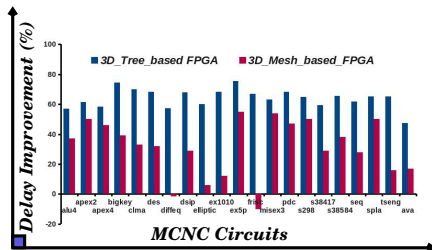
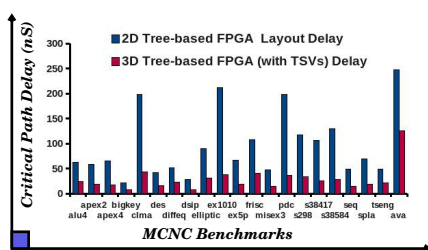
TSV & Architecture Optimization

Optimization Results

Tree Levels=7	Arity=4, Arch=4x4x4x4x4x4x4			
Architecture Levels	3D Chip Layer	Optimized Rent 'p'	Int/TSV Gain(%)	Optimized Area μm^2
Logic Blocks	Layer 1	–	–	93635273
Switch Level 0	Layer 1	0.67	33(Int)	2412
Switch Level 1	Layer 1	0.54	46(Int)	10800
Switch Level 2	Layer 1	0.66	34(Int)	37496
Switch Level 3	Layer 1	0.59	41(TSV)	232128
<i>BreakPoint_{Hori}</i>	Horizontal Break Point			
Level 3 to 4	TSV Area=40192 μm^2			
Switch Level 4	Layer 2	0.67	33(Int)	6072770
Switch Level 5	Layer 2	0.66	34(Int)	45553499
Switch Level 6	Layer 2	0.65	35(Int)	42139683
Average		63.42	36.57	

Rent=1 : Performance Analysis

Tree Levels=7, Arity=4, Arch=4x4x4x4x4x4x4					
		Delay ($\times 10^{-9}$ sec)		Performance Gain (%)	
circuits	$2D_{Tree}$	$3D_{Tree}$	$2D_{Tree}$	3D Mesh Gain	
MCNC	Tree-based	With TSV	$3D_{with-TSV}$	Vs 2D	
average(21)	96.06ns	28.76ns	68.7%	32%	



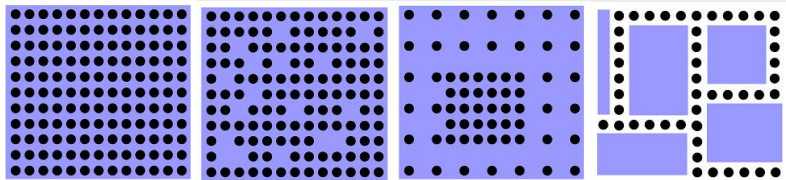
21 MCNC¹ benchmark circuits

¹<http://er.cs.ucla.edu/benchmarks/ibm-place>.

TSV Distribution and Placement

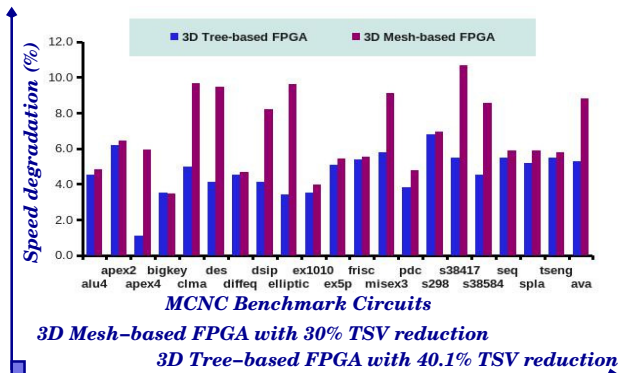
3D Tree-based FPGA, TSV Placement

- ① Impact of TSV reduction on Performance
- ② The count and location of TSVs have significant impact performance of 3D stacked chip
- ③ Tradeoff studies performed with **Tree interconnect level partitioning** across the dies in the 3D stack.
- ④ Simulations used **regular and non-regular TSV placement**.



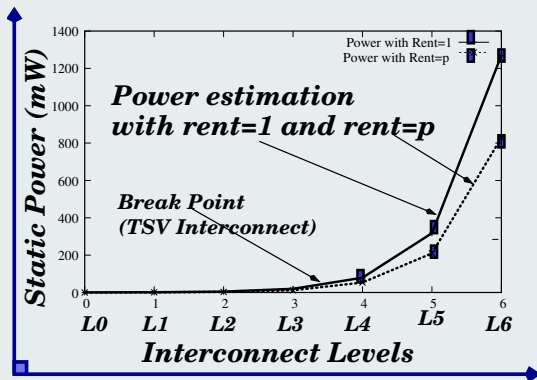
Speed Degradation

Tree Levels=7, Arity=4, Arch=4x4x4x4x4x4x4					
		TSV Reduction(%)		Speed Degradation(%)	
MCNC(21)	Tree-based	Mesh-based	Tree-based	Mesh-based	
average	40.1	30	4.7	6.8	



Static Power Consumption

3D Tree level Power Optimization



- 1 37% reduction is programmable interconnect network
- 2 28% reduction is total power consumption.

3D FPGA Statistics

3D Tree-based FPGA Vs 3D Mesh-based FPGA

- 1 TSV Count reduced by 40%
- 2 Programmable Interconnect area reduced by 37%.
- 3 Path delay (performance) improved by 53%.
- 4 Programmable interconnect power reduced by 28%.

Presentation Summary

- 1 Developed a software supported design and optimization flow for 3D Tree-based FPGA
- 2 Physical design challenges of Tree-based programmable interconnect networks identified
- 3 A horizontal partitioning methodology for Tree-based programmable interconnect network to enable 3D integration.
- 4 3D integration enables improvements in performance, power conception and area of 3D stacked Tree-based FPGA.
- 5 An architecture and TSV count optimization flow introduced
- 6 3D Tree-based FPGA demonstrator



CoolChip :3D Tree-based FPGA

Vinod Pangracious <vinod.pangracious@etu.upmc.fr>