

P9 : ARC-2013

Performance Analysis And Optimization of High Density Tree-based 3D Multilevel FPGA

V. Pangracious, Z. Marrakchi, E. Amouri, H. Mehrez



Presentation Outlook

Introduction : FPGA Architecture

- 1 Mesh-based and Tree-based FPGA architecture
- 2 Tree-based FPGA interconnect organization
- 3 Why 3D FPGA ? Why 3D Tree-based FPGA ?

3D Tree-based FPGA Design and Exploration

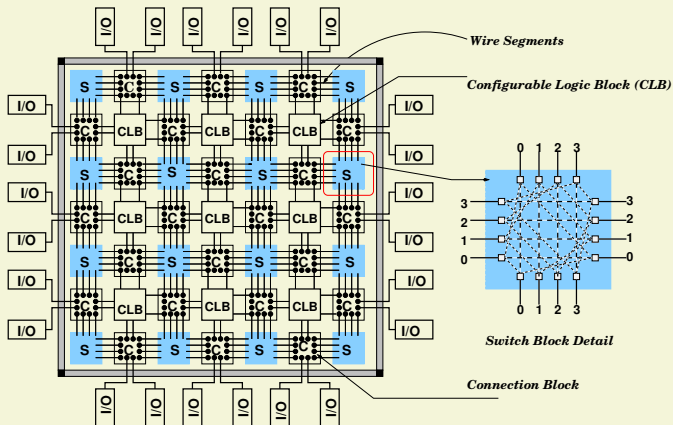
- 1 Design and Exploration Methodology
- 2 3D Floorplan development.
- 3 Layout characterization, Timing Analysis

3D Tree-based FPGA Experimental Analysis

- 1 Performance analysis
- 2 Architecture optimization & Thermal analysis

FPGA Architecture

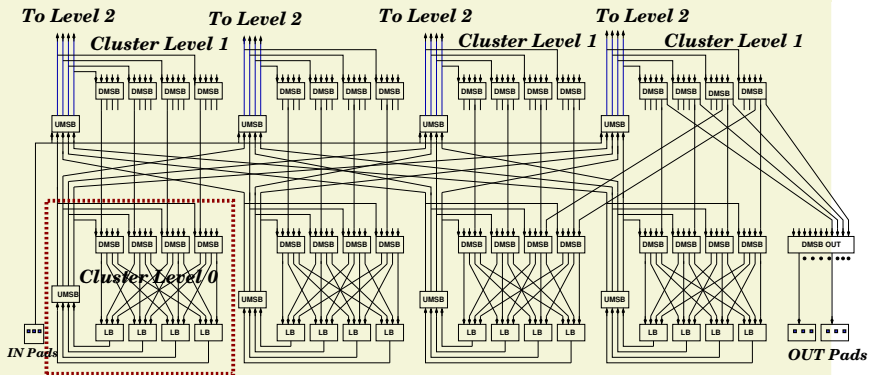
Mesh-based FPGA : Industrial Architecture



- Most common Academic and Industrial Architecture

FPGA Architecture

A Novel High Density Tree-based FPGA Architecture



An integrated upward and downward unidirectional programmable interconnect network using *Butterfly-fat-tree* network topology

Tree-Based FPGA Interconnect Network Organization

Upward Interconnection

- Upward Mini Switch Blocks
- Full crossbar switch

$$nbUMSB(\ell) = N_{in}(\ell - 1)$$

Downward Interconnection

- Downward Mini Switch Blocks
- Full crossbar switch

$$nbDMSB(\ell) = N_{in}(\ell - 1)$$

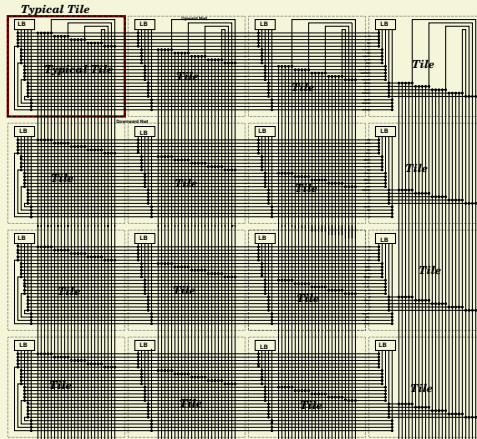
$$N_{switch}(down) = N \times (k^p c_{in} + k c_{out}) \times \sum_{\ell=1}^{\log_k(N)} k^{(p-1)(\ell-1)}$$

$$N_{switch}(up) = N \times k \times c_{out} \times \sum_{\ell=1}^{\log_k(N)} k^{(p-1)(\ell-1)}$$

N is the total number of logic blocks, c_{in} and c_{out} are the number of inputs and outputs of logic blocks, k is the arity, and p and ℓ are the Rent's parameter and level.

2-Dimensional Floorplan

2D Floorplan of Tree-based FPGA



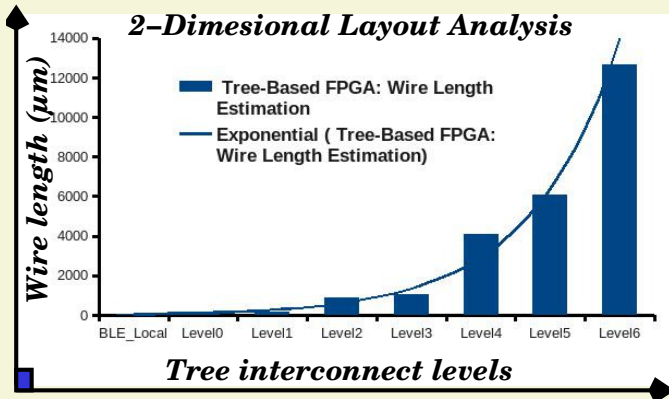
Flattened Tree-based FPGA layout plan : topologically equivalent of Tree-based FPGA architecture

V. Pangracious, Z. Marrakchi, E. Amouri, H. Mehrez — 3D Tree-based FPGA — 4 avril 2013

6/27

2-Dimensional Tree-based FPGA

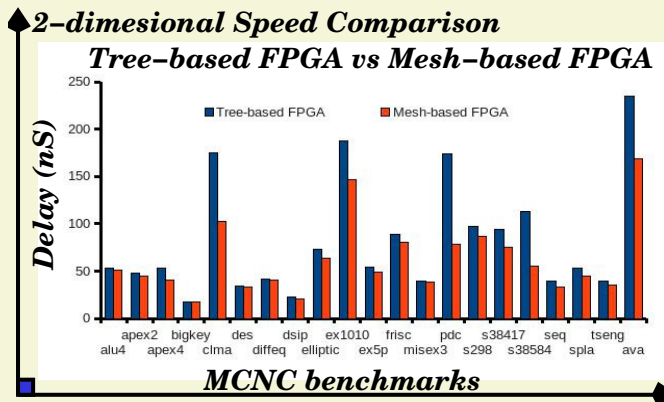
Delay estimation of 2D Tree-based FPGA layout



Wire length increases exponentially as Tree grows to higher levels

2-Dimensional Tree-based FPGA Vs Mesh-based FPGA

Performance : 2D Tree-based FPGA Vs Mesh-based FPGA



Mesh is 20% better compared to Tree-based FPGA

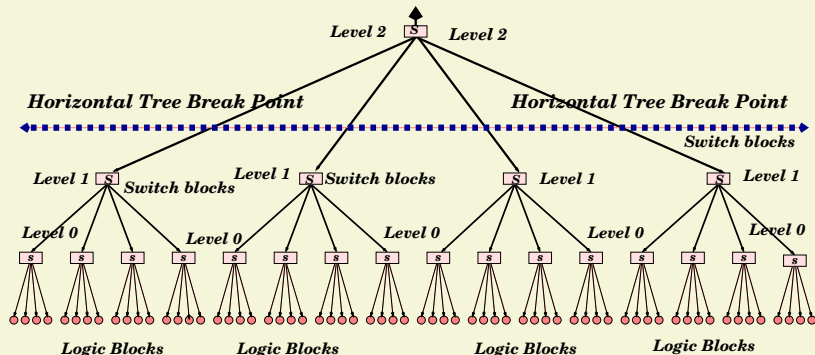
Can 3D Integration Help to improve Performance of Tree-based FPGA ?

State of the Art : 3D FPGA

- 1 Many recent publication on 3D Mesh-based FPGA & performance improvement.
- 2 FPGA an interconnect dominated device : 3D integration can address problems pertaining to routing congestion, limited I/O connections, low resource utilization, long wire delays and thermal issues.
- 3 Optimization of programmable interconnect overhead of Tree-based FPGA is a major challenge.

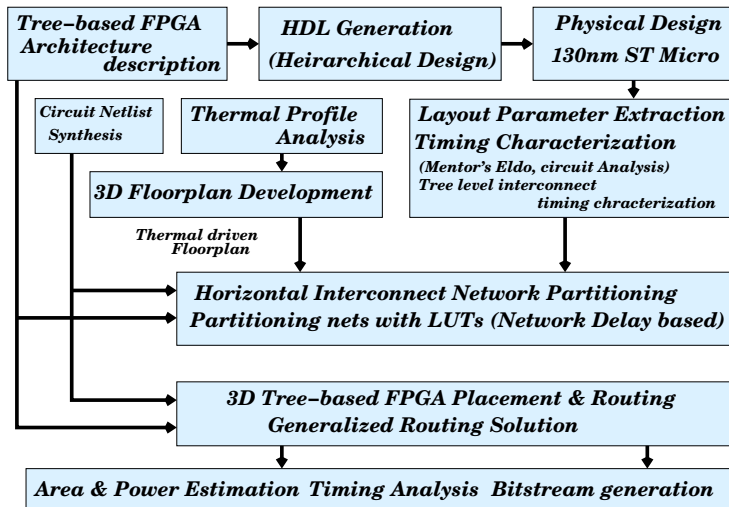
3D Stacked Tree-based FPGA

Horizontal Partitioning of Tree Interconnect



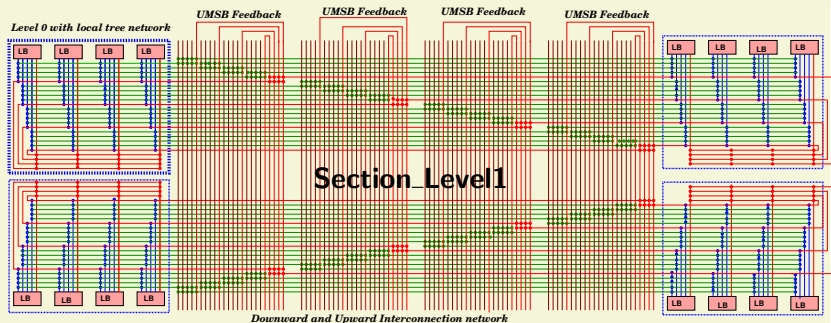
The network partitioning and location of the break-point is decided based delay optimization of different tree levels.

3D Design and Exploration



3D Tree-based FPGA : Physical Design and Development

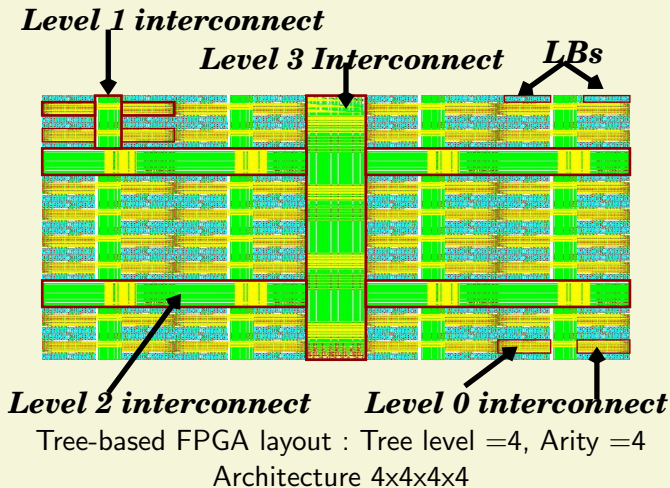
3D compatible Layout Design



The layout is done in a way to bring together every cluster and its corresponding tree level interconnects to form section_level0, section_level1 etc.

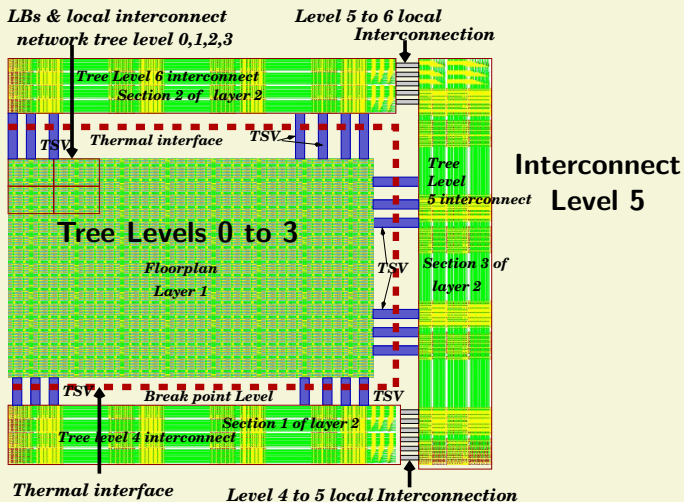
3-Dimensional Layout Design

3D compatible Layout Design



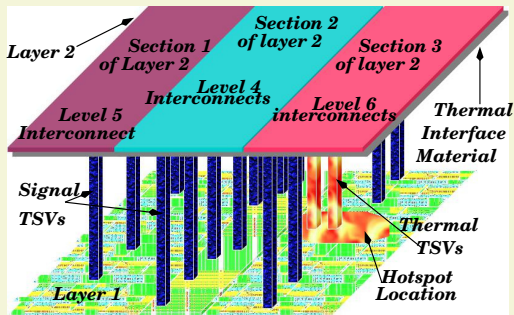
3-Dimensional Layout Design

3D compatible Tree-based FPGA Floorplan arrangement



3-Dimensional Layout Design

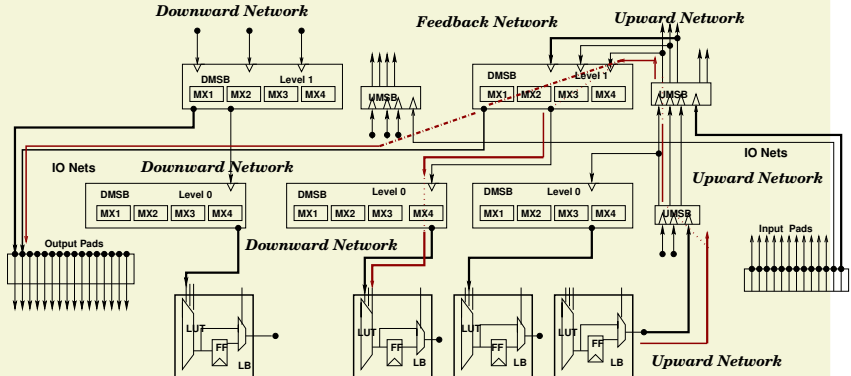
3D compatible Layout Design



The horizontal break point will place the total logic density of Tree-based FPGA in active layer 1 and programmable interconnect networks above the break-point will be placed in Layer 2 of the 3D stacked chip.

3-Dimensional Layout Analysis

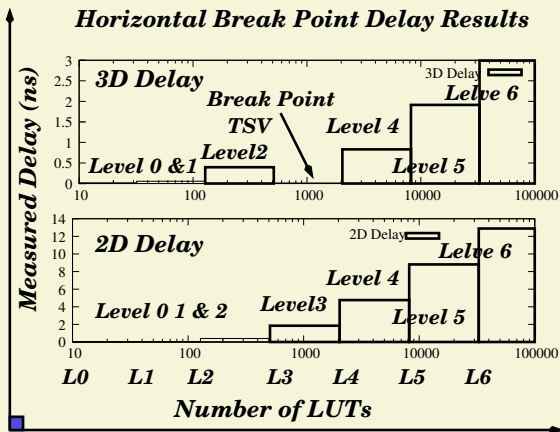
3D Layout Delay estimation



Used Mentor's SPICE accurate circuit simulator *Eldo* to measure the wire delay between different tree levels. ST Micro's 130nm technology models used for analysis.

3-Dimensional Layout Analysis

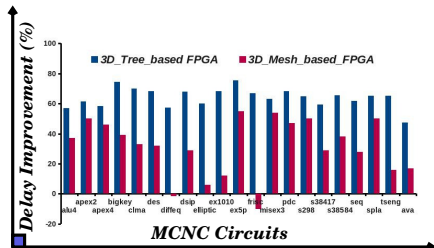
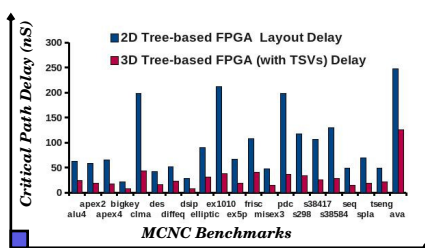
3D Layout Delay measurement setup



The higher level programmable interconnects are rearranged in layer 2 to optimize the delay

3D FPGA Performance Analysis

Tree Levels=7, Arity=4, Arch=4x4x4x4x4x4x4				
	Delay ($\times 10^{-9} \text{sec}$)		Performance Gain (%)	
circuits	$2D_{Tree}$	$3D_{Tree}$	$2D_{Tree}$	3D Mesh Gain
MCNC	Tree-based	With TSV	$3D_{with-TSV}$	Vs 2D
average(21)	96.06ns	28.76ns	68.7%	32%



The largest set of 21 MCNC¹ benchmark circuits are used to evaluate the performance of 3D Tree-based and Mesh-based FPGA

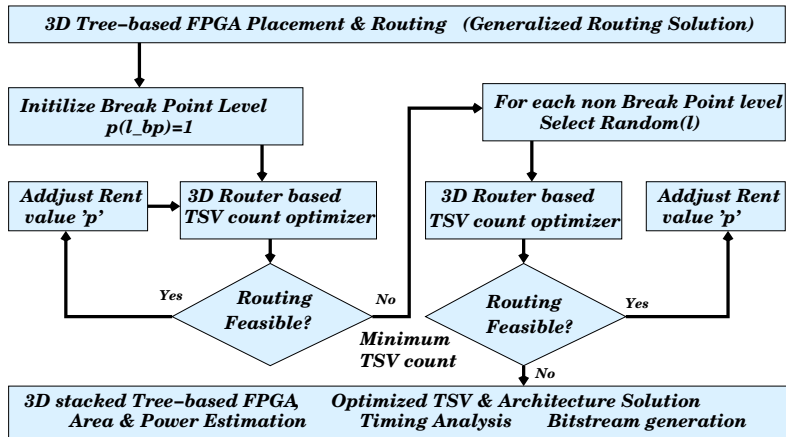
¹<http://er.cs.ucla.edu/benchmarks/ibm-place>.

3D Tree-based FPGA : TSV & Architecture Optimization

Programmable Interconnect Optimization

- TSVs are huge and cause coupling
- TSV count is crucial (Design, Manufacturing, cost) How Many?
- TSV location is crucial (Design, Device, Performance) Where?
- TSVs require design-for-testing, Power and Clock Delivery
- TSVs require design-for-manufacturability/reliability
- Area and Power consumption Optimization

3D Tree-based FPGA TSV & Architecture Optimization Flow



TSV & Architecture Optimization

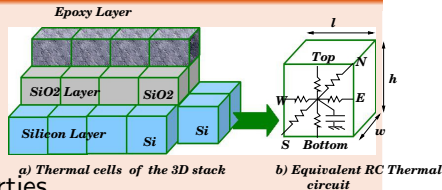
Optimization Results

Tree Levels=7	Arity=4, Arch=4x4x4x4x4x4x4		
Architecture Levels	3D Chip Layer	Optimized Rent 'p'	Optimized Area μm^2
Logic Blocks	Layer 1	–	93635273
Switch Level 0	Layer 1	0.67	2412
Switch Level 1	Layer 1	0.54	10800
Switch Level 2	Layer 1	0.66	37496
Switch Level 3	Layer 1	0.59	232128
<i>BreakPoint_{Hori}</i>	Horizontal Break Point		
Level 3 to 4	TSV Area=40192 μm^2		
Swit Level 4	Layer 2	0.67	6072770
Swit Level 5	Layer 2	0.66	45553499
Swit Level 6	Layer 2	0.62	42139683

FPGA : Thermal Analysis

3D Thermal Modeling & Analysis

- n tier 3D thermal model
- High-order RC-level heat flow models
- power model of tier components, geometrical properties
- Heat flow \sim Electrical current, Temperature \sim Voltage
- Metal and Si layers composed of elementary blocks
- Tree-based FPGA components like considered separately.
- Effective thermal conductivity of active and intermediate layers.



$$k_{eff} = k_{cu} \times (TSV_{Area}) + K_{th} \times (Level_{BPA_{Area}} - TSV_{Area})$$

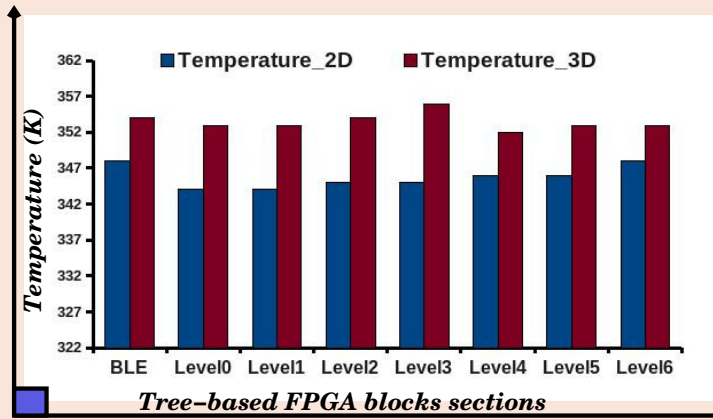
FPGA : Thermal Analysis

3D Thermal Modeling & Analysis

Tree-based FPGA Block Type	3D Chip # Layer	Block Area in μm^2	Power mW
CLB Units	1	93635273	0.15
Switch box Level 0	1	2412	0.25
Switch box Level 1	1	10800	0.83
Switch box Level 2	1	37496	2.70
Switch box Level 3	1	232128	15.13
Break Point Level	TSV Area	= 40192	-
Switch box Level 4	2	6072770	62.46
Switch box Level 5	2	45553499	214.05
Switch box Level 6	2	42139683	838.97

FPGA Thermal Analysis

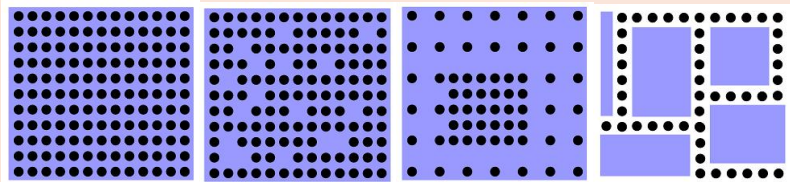
Experimental Results



3D Tree-based FPGA Thermal Management

3D Thermal Profile, Thermal TSV How Many and Where?

- 1 The count and location of TSVs have significant impact performance of 3D stacked chip
- 2 Tradeoff studies performed with **Tree interconnect block-level partitioning** across the dies in the 3D stack.
- 3 Simulations used **regular and non-regular TSV placement**.



Presentation Summary

- Comparison of Mesh-based and Tree-based FPGA
- Developed a software supported design and exploration flow for 3D Tree-based FPGA
- Physical design challenges of Tree-based programmable interconnect networks identified
- A horizontal partitioning methodology for Tree-based programmable interconnect network to enable 3D integration.
- 3D integration enables improvements in performance, power conception and area of 3D stacked Tree-based FPGA.
- An architecture and TSV count optimization flow introduced
- Thermal analysis module for 3D Tree-based FPGA
- 3D Tree-based FPGA demonstrator



3D Tree-based FPGA

Vinod Pangracious <vinod.pangracious@etu.upmc.fr>