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A voltage polarity dependent, voltage-induced wetting transition is demonstrated using a liquid metal-oxide-semiconductor (MOS) junction. A droplet of mercury can be made to spread out on an oxidized silicon wafer upon the application of a voltage. The wetting is seen to depend on the doping type and doping density of the silicon—a voltage polarity related asymmetrical electrowetting is observed. Impedance measurements on Al-SiO_2-Si MOS capacitors link the space-charge effects with the electrowetting on the Hg-SiO_2-Si MOS junction. A modified Young-Lippmann equation for electrowetting at a MOS junction is derived—the model agrees with the experiments. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4822308]

The liquid-insulator-semiconductor junction has many applications including *inter alia* semiconductor profiling,[1,2] chemical sensing,[3,4] energy harvesting,[5] molecular biology,[6] solar water splitting,[7] and microelectromechanical systems (MEMS).[8] Here, asymmetrical voltage polarity dependent electrowetting[9–11] is observed using a liquid metal-oxide semiconductor (MOS) junction[12–14]—such wetting transitions involving liquids and semiconductors[15,16] could be useful for applications in miniaturized chemistry and biology,[10] optofluidics,[17] and microfluidic electronics.[18]

Fig. 1 shows the MOS junction which is formed by placing a mercury droplet onto an oxidized silicon wafer.[19,20] The electrical impedance of a MOS junction is well documented[12–14] and can be divided in four main cases: (i) accumulation, (ii) depletion, (iii) inversion, and (iv) deep depletion. If we consider a p-type uniformly doped silicon wafer [Fig. 1]: A negative voltage—applied to the mercury droplet—will result in carrier accumulation at the silicon dioxide-silicon interface whereas a positive potential can result in carrier depletion, inversion and deep depletion.[12–14] It is well known that observation of carrier accumulation, depletion, inversion, and deep depletion are voltage-polarity, small-signal frequency (AC) and—in the case of deep depletion—applied DC voltage ramp-rate dependent.[12–14]

Electrowetting is dependent on the capacitance at the liquid-solid interface.[9] In the case of electrowetting-on-dielectric (EWOD),[9] the *areal* capacitance is considered to be constant with voltage—this leads to the well-known Young-Lippmann EWOD electrowetting equation[21] where the contact angle of a droplet varies with the square of the applied voltage.[9] However, for electrolyte-silicon[22] and electrolyte-oxide-silicon[23] junctions, the areal capacitance is not constant with applied voltage and electrowetting at such junctions[15,16] requires a modified Young-Lippmann equation to describe their behavior. Using this property, the author has previously demonstrated an optically-induced wetting transition using an electrolyte-insulator-semiconductor junction.[15]

Oxidized silicon wafers were prepared in a class ISO 5/7 cleanroom ($T = 20\,°C \pm 0.5\,°C$; $RH = 45\% \pm 2\%$) environment using polished, 3 in. diameter, (100) silicon wafers (Siltronix, France); p-type (5–10 Ω cm) and n-type (5–10 Ω cm) were used for the study. A silicon dioxide layer was grown onto each wafer using standard wet oxidation at 850 °C for 10 min in an O_2 (1.5 l min^{-1})-H_2 (2.5 l min^{-1}) gas mixture at atmospheric pressure. The thickness of the silicon dioxide layers d_{ox} was measured to be 23 (±0.3) nm (p-type) and 22.5 (±0.1) nm (n-type) using an UVISEL ellipsometer (Horiba, France). Following removal of the silicon dioxide from the rear surface of the silicon wafers using front-side masking (photoresist) and a hydrofluoric acid (50%) etch, ohmic contacts were formed on the backs of the silicon wafers using boron ion implantation (nominal doping = 10^{20} cm^{-3} over a depth of 100 nm), aluminum evaporation (200 nm) and rapid thermal annealing (450 °C/30s)—this temperature step also has the effect of reducing the silicon dioxide-silicon interface trap density.[24] The average doping densities N of the p-type and n-type wafers were measured using impedance measurements to be 2.12×10^{15} (±0.06) cm^{-3} and 5.2×10^{14}

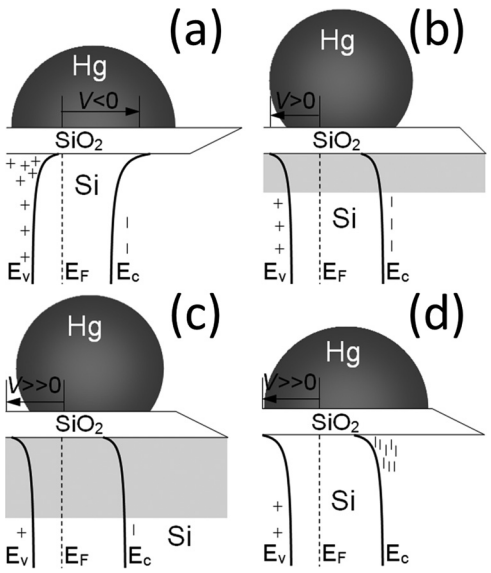

FIG. 1. Possible voltage-induced wetting transitions of a liquid metal using an Hg-SiO_2-Si (p-type) MOS capacitor. (a) Carrier accumulation (applied voltage $V < 0$), (b) depletion ($V > 0$), (c) deep depletion ($V \gg 0$), and (d) inversion ($V \gg 0$).

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(± 0.3) cm^{-3}, respectively, using evaporated aluminum Schottky diodes.

The electrowetting experiments were performed in a class ISO 5/7 cleanroom. The contact angle data was gathered using a commercial Contact Angle Meter (GBX Scientific Instruments, France). A voltage was applied using an E3634A DC power supply (Agilent, USA). Small mercury droplets (diameter ~ 1 mm, volume ~ 0.5 μl) were carefully placed on the surface of the oxidized silicon wafers using a pipette. Mercury has been previously used in the context of EWOD systems for MEMS applications.[25] A steel needle having a diameter equal to 200 μm was used to contact the droplet. The contact angle was extracted using an ellipsoid model[26,27] and a freeware software.[28] Several measurements were performed per data point—the average standard deviation of the data points is 0.6°.

Fig. 2 shows photographic evidence for electrowetting using an Hg-SiO_2-Si MOS junction using an n-type silicon wafer. The zero-bias contact angle is modified upon applications of a voltage of ± 10 V. Under forward bias (+10 V) the contact angle reduces by ~6° [Fig. 2(c)] whereas under reverse bias the contact angle reduces by ~1° [Fig. 2(d)]. Fig. 3 shows plots of the measured contact angle of the mercury droplet as a function of applied voltage for p-type [Fig. 3(a)] and n-type [Fig. 3(b)] oxidized silicon. There are several observations which can be noted from these figures. First, the zero-bias contact angle of Hg on SiO_2 is 140.4 (0.8)°, i.e., SiO_2 is a relatively non-wetting surface to mercury.[26,29] Second, both a reverse and a forward bias voltage cause the contact angle of the mercury droplet to reduce, i.e., typical electrowetting behaviour.[9] Third, a forward bias voltage (positive for n-type silicon and negative for p-type silicon) leads to a greater change in the apparent contact angle of the droplet than a reverse bias voltage—for a given voltage, i.e., the electrowetting is voltage polarity dependent. A voltage polarity dependent electrowetting using an EWOD setup was reported[30] using a silicon wafer coated with a thin layer (100 nm) of amorphous fluoropolymer—unexplained at the time but most likely due to the presence of the space-charge layer in the silicon.[15] The presence of the electrical double layer in the liquid can also create a voltage-polarity dependent electrowetting effect.[31] More recently, such voltage polarity depended electrowetting effects—produced via the introduction of an electrochemical diode into an EWOD circuit[32] or using a negative photoresist[33] (SU-8)—have been used for actuation applications. The asymmetry is more apparent for the n-type material [Fig. 3(b)]. Contact angle saturation (CAS)[34] is apparent under forward bias voltages. CAS occurs at low voltages in forward bias for both n-type

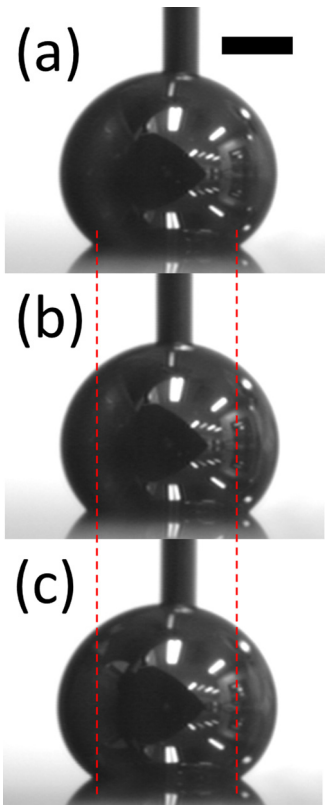

FIG. 2. Evidence for a voltage polarity dependent, voltage-induced wetting transition using an Hg-SiO_2-Si MOS junction. (a) zero-bias, (b) +10 V, and (c) −10 V. The silicon wafer is n-type—substrate doping level is 5.2×10^{14} (± 0.3) cm^{-3}, the silicon dioxide thickness is 22.5 (0.1) nm. Scale bar = 400 μm.

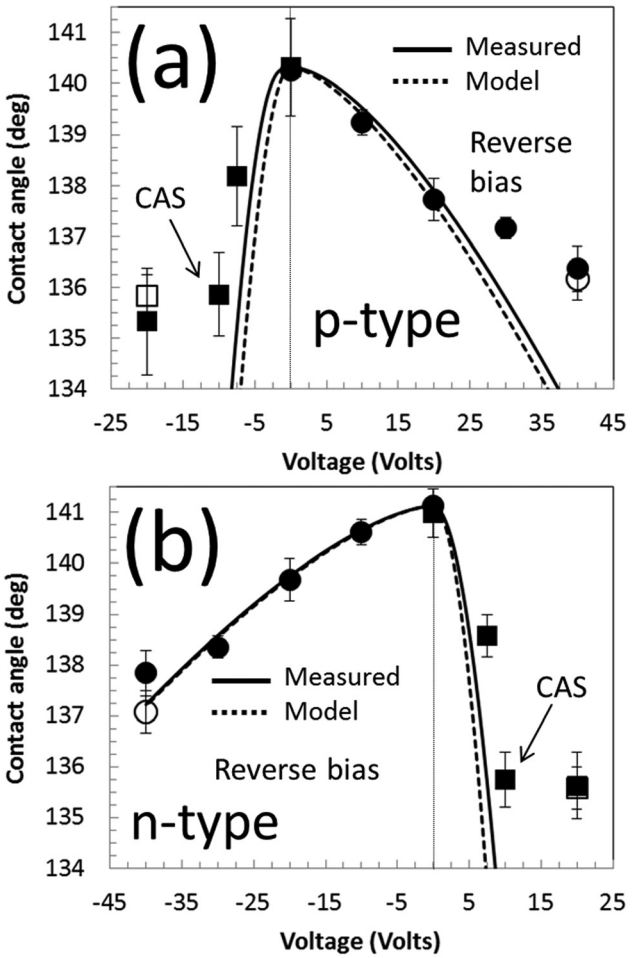

FIG. 3. Plots of the measured contact angle θ of the mercury droplet versus applied voltage V for an Hg-SiO_2-Si MOS junction: (a) p-type silicon and (b) n-type silicon under forward bias (squares) and reverse bias (circles). Filled shapes correspond to data gathered using a voltage ramp (5 V s^{-1}), open shapes correspond to data gathered using a voltage step. The solid lines correspond to the calculated contact angle using the C-V measurements; the dashed lines correspond to the modified Young-Lippmann equations—Eqs. (3) and (4). CAS indicates the contact angle saturation.

and p-type material and the saturation angle is comparable—between 135°–136° occurring between 10 V to 20 V. Under reverse bias, the data indicate the apparent onset of CAS >20 V in the p-type material and >30 V in n-type material. The voltage was applied as a ramp (solid data points) and as a step (open data points)—it can be observed that ramping the voltage (2–5 V s^{-1}) leads to the same contact angle change (in reverse and forward bias) as does stepping the voltage to the final value—within the standard error of the measurement. By filming the evolution of the contact angle—the reaction to a voltage step—the contact angle switching times were evaluated to be 76.2 (0.9) ms and 72.3 (1.3) ms (p-type—forward and reverse) and 66.9 (0.4) ms and 70.7 (3.5) ms (n-type—forward and reverse). In order to gain a better understanding of these electrowetting observations, electrical measurements were conducted.

Electrical impedance measurements were conducted on MOS capacitors made by evaporation of aluminum (250 nm) via a shadow mask onto quarter wafers of the same oxidized silicon wafers which had been prepared for the electrowetting experiments. The surface area of the MOS capacitors was 9.86×10^{-7} m^2—purposely comparable with the liquid-solid interface area of the mercury droplets during the electrowetting experiments. The measurements were carried out using a 4294A impedance analyzer (Agilent, USA). A calibration (open circuit—load (200 Ω)—short circuit) was performed using a P/N101-190 S/N33994 Impedance Standard Substrate (Cascade Microtech, USA) over the frequency range (500 Hz–10 MHz) prior to the measurements. The capacitance-voltage (*C-V*) measurements were performed at different small-signal frequencies f_{ss} and different DC voltage ramp rates. The measurements were also performed beginning and finishing in reverse bias. The DC voltage was applied using steps—the DC voltage ramp rate was varied by changing the delay time between voltage steps—f_{ss} was varied from 1 kHz to 10 MHz and the ramp rate was varied from 0.56 V s^{-1} to 90 V s^{-1}.

Fig. 4 shows the measured areal junction capacitance—measured at $f_{ss} = 1$ MHz and a ramp rate of 5 V s^{-1}—plotted against the applied DC voltage value for the Al-SiO_2-Si MOS junctions made using the p-type [Fig. 4(a)] and n-type [Fig. 4(b)] silicon. First, the resulting *C-V* profile does not depend on applied polarity of *V*, e.g., in the case of the n-type sample the *C-V* plot is the same when *V* is varied from +10 V to −40 V as from −40 V to +10 V—for a given f_{ss}. Second, the ramp rate of *V* is seen to have very little influence on the resulting *C-V* profile for a given f_{ss}. Third, the *C-V* profile evolves as f_{ss} is varied (data not shown here)—this is a very well documented effect.[12–14] The *C-V* measurements (in reverse bias) indicate depletion and deep depletion[12–14] [Fig. 4]—the areal capacitance is reducing as the applied voltage is increased. Deep depletion occurs when the MOS capacitor is not in thermal equilibrium due to a high voltage sweep rate for the doping levels used here, e.g., deep depletion is observed at the lowest voltage sweep rate (0.56 V s^{-1}) for both wafers. Under forward bias, the capacitance corresponds to the value of the silicon dioxide layer.

The spreading resistance—due to the finite resistivity of the substrate—can be obtained from the impedance measurements and compared to a model.[35] For the mercury

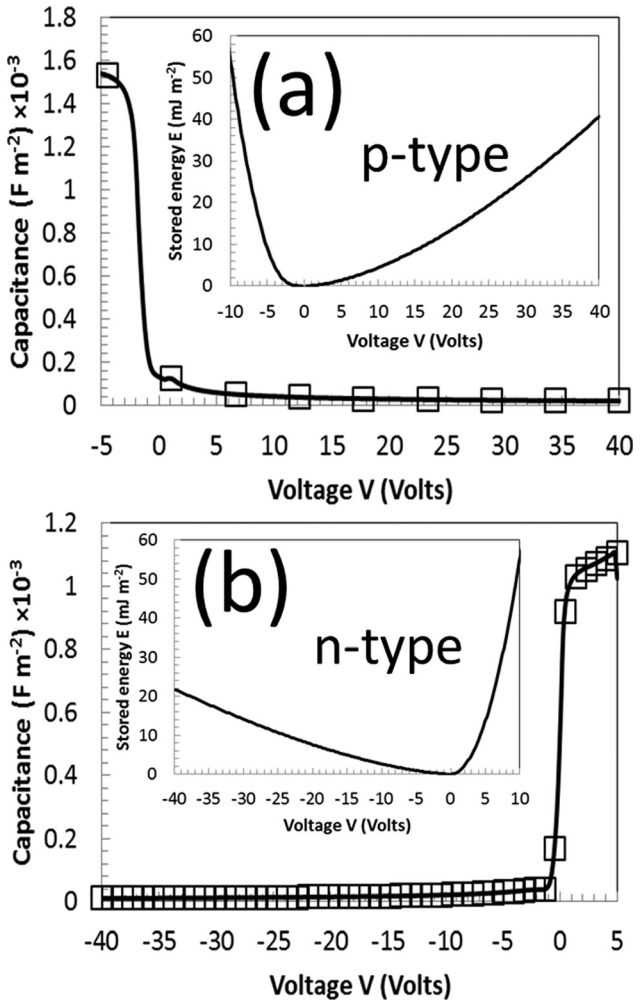

FIG. 4. Electrical impedance measurements obtained using Al-SiO_2-Si MOS capacitors using (a) p-type silicon and (b) n-type silicon. The solid curves correspond to a sweep rate of 0.56 V s^{-1} (p-type and n-type), open squares correspond to a sweep rate of 90 V s^{-1} (p-type) and 18 V s^{-1} (n-type)—small-signal frequency = 1 MHz. The insets show the variation of stored electrical energy (J m^{-2}) as a function of the applied voltage.

droplets—base diameter ~1 mm—the maximum capacitance (C_m) is of the order of ~1 nF. The measured spreading resistance (R_s) is <1 k Ω for both wafers, this yields an electrical time constant (R_sC_m) of <1 μs. Note that this value is much smaller than contact angle switching times which were evaluated during the electrowetting experiments. Indeed, MOS structures are used for fast switching applications[36]—hence it is reasonable to assume that hydrodynamic effects (electrowetting switching speeds ~ tens of microseconds to tens of milliseconds[9]) are due to the liquid properties of mercury and not the electrical circuit.

The *C-V* results can be used to predict the contact angle variation during electrowetting for the liquid MOS junction using the following reasoning. The Young-Lippmann equation[9] is given by

$$\cos\theta(V) = \cos\theta_0 + \frac{E(V)}{\gamma}, \tag{1}$$

where $\theta(V)$ is the variation of the contact angle with voltage, θ_0 is the contact angle at zero bias, $E(V)$ is the variation of the stored energy (J m^{-2}) of the system with voltage *V*, and γ

is the surface tension of the liquid. The evolution of the stored charge $Q(V)$ can be calculated from the C-V data using $Q = \int CdV$ and the stored energy $E(V)$ can be calculated using $E = \int QdV$—the stored electrical energy of the MOS capacitors is shown in the insets to Fig. 4. By taking the surface tension of mercury to be 486.5 mJ cm^{-2} and θ_0 (determined from the wetting experiments), the predicted contact angle variation $\theta(V)$ can be plotted against voltage—these are the solid lines in Fig. 3—using the C-V data measured at 1 MHz.

In addition, a simple MOS junction capacitance model[12] can be used to derive a modified Young-Lippmann equation for electrowetting at a MOS junction in reverse bias. The reverse bias voltage dependent capacitance $C(V)$ of a MOS junction can be approximated by[12]

$$C(V) = \frac{\alpha}{\sqrt{1 + \left(\frac{2\alpha^2 V}{\beta}\right)}}, \quad (2)$$

where $\alpha = C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{d_{ox}}$ and $\beta = \varepsilon_{Si}\varepsilon_0 qN$. By integrating Eq. (2) (as explained above) and inserting the result into Eq. (1), we obtain Eq. (3) which is a modified Young-Lippmann equation for electrowetting at a reverse biased MOS junction,

$$\cos\theta(V) = \cos\theta_0 + \frac{\beta^2}{3\alpha^3\gamma}\left(\frac{2\alpha^2 V}{\beta} + 1\right)^{\frac{3}{2}} - \frac{\beta}{\alpha\gamma}V - \frac{\beta^2}{3\alpha^3\gamma}, \quad (3)$$

and in forward bias we have

$$\cos\theta(V) = \cos\theta_0 + \frac{\alpha}{2\gamma}V^2. \quad (4)$$

Equation (3) is an approximate solution and the following assumptions are made in order to write it down—at $V = 0$, $C = C_{ox}$, the stored charge $Q = 0$ and the stored energy $E = 0$. In a first approximation, the model also considers that the surface state contribution to the junction capacitance is negligible and that the junction is a perfect capacitance. These assumptions enable one to determine the two constants of integration. By using the experimentally derived doping densities and the oxide thicknesses (see above) together with following relative permittivities[13] for silicon dioxide ($\varepsilon_{ox} = 3.9$) and silicon ($\varepsilon_{Si} = 11.9$), one can plot Eqs. (3) and (4) onto Fig. 3—these are the dashed lines. It can be seen that the simple model fits relatively well with the contact angle data. Although it should be noted that under forward bias, the measured contact angle does not diminish as rapidly as that suggested by the measured capacitance (solid line) or the model (dashed line) [Eq. (4)]—this is a common observation.[30,37]

Current-voltage measurements were carried out on the MOS capacitors using a 2612 System SourceMeter® (Keithley, USA). The current-voltage measurements were carried out on three MOS capacitor surface areas: 8.83×10^{-9} m^2, 8.68×10^{-8} m^2, and 9.86×10^{-7} m^2. The breakdown voltages—in forward and reverse bias—are given in Table I. For both p-type and n-type material, the measured breakdown voltage (forward and reverse bias) is seen to increase with reducing device area of the MOS capacitors. The breakdown voltage of MOS capacitors is known to depend on the device area[38–41]—the results here are in agreement with these findings. The reverse bias breakdown voltages of the large area devices are in good agreement with established data for lowly doped silicon MOS capacitors in deep depletion.[13,42] For the largest area device area measured—which is comparable with the electrowetting experiments—the results indicate that electrical breakdown may have a role in the CAS during the electrowetting experiments using the n-type material [Fig. 3(b)]—indeed, the possible role of electrical breakdown in electrowetting at a liquid metal-semiconductor junction has previously been discussed by the author.[16] In contrast, the forward bias breakdown voltage for the p-type material is double the voltage where CAS occurs during electrowetting [Fig. 3(a)] implying that breakdown is not playing a role for CAS during electrowetting on the p-type material. The measured reverse bias breakdown voltages [Table I]—for an Al-SiO_2-Si MOS device area comparable with the Hg-SiO_2 liquid-surface interface area—also indicate that electrical breakdown is not playing a role in CAS under reverse bias for either p-type or n-type.

TABLE I. Measured breakdown voltage under forward (f) and reverse (r) bias for p-type and n-type Al-SiO_2-Si MOS capacitors of different device areas.

Area	Breakdown voltage (V)			
$\times 10^{-7}$(m^2)	p-type (f)	n-type (f)	p-type (r)	n-type (r)
0.09	−27.5 (0.4)	23.3 (1.6)	91.6 (3.2)	−130 (5)
0.87	−24.8 (1.4)	18.1 (1.9)	74.7 (2.5)	−108.8 (2.5)
9.86	−23.4 (1)	13.7 (0.9)	62.1 (3.7)	−79 (1.4)

Comparison of the electrowetting data obtained using a Hg-SiO_2-Si MOS junction with the C-V data obtained using an Al-SiO_2-Si MOS junction can be supported by: (i) both mercury[19,20] and aluminum[12–14] form good quality MOS junctions and (ii) the work functions of mercury (~4.5 eV) (Ref. 13) and aluminum (~4.4 eV) (Ref. 13) are comparable. Also, using aluminum as the gate material—as opposed to the use of mercury—ensures that no errors in contact area are incurred during the electrical measurements.[16]

The solid curves (based on the C-V measurements) and the dashed curves (based on the MOS capacitance model[12]) in Fig. 3 fit reasonably well with the electrowetting data points—for both p-type and n-type silicon. Both solid and dashed curves predict an electrowetting asymmetry with voltage polarity and that this asymmetry should be more apparent a lower doped material (n-type silicon here) [Fig. 3(b)]. With reference to Fig. 1—the scenarios given in Fig. 1(a) (carrier accumulation), Fig. 1(b) (carrier depletion), and Fig. 1(c) (deep depletion) are observed here (10^{14}–10^{15} cm^{-3}). One can conclude that the electrowetting behavior—under reverse bias and a voltage sweep rate >0.5 V s^{-1}—is determined by the deep depletion capacitance (measured at high f_{ss}). The electrowetting experiments did not reveal evidence for the scenario shown in Fig. 1(d),

i.e., due to carrier inversion. The relatively low doping levels of the silicon here—required to observe a voltage polarity dependent wetting transition—implies that inversion is difficult to observe in such MOS capacitors.[12–14] Indeed, this hypothesis is supported by the *C-V* measurements where no inversion effects are observed for the MOS capacitors studied.

The choice of the semiconductor doping density and the silicon dioxide layer is critical to observing the voltage polarity dependent voltage-induced wetting transition—if the doping density is large ($>10^{16}\,\mathrm{cm}^{-3}$) the underlying semiconductor will be too conducting and EWOD-like voltage-polarity symmetrical electrowetting will be observed irrespective of the silicon dioxide thickness. At lower doping levels ($<10^{16}\,\mathrm{cm}^{-3}$)—as used here—and larger silicon dioxide layer thicknesses ($>100\,\mathrm{nm}$), the low capacitance of the latter layer will dominate the overall oxide-semiconductor capacitance—resulting in EWOD-like voltage polarity symmetrical electrowetting.

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