



HAL
open science

Bio-inspired stochastic computing using binary CBRAM synapses

Manan Suri, Damien Querlioz, Olivier Bichler, Giorgio Palma, Elisa Vianello, Dominique Vuillaume, Christian Gamrat, Barbara de Salvo

► To cite this version:

Manan Suri, Damien Querlioz, Olivier Bichler, Giorgio Palma, Elisa Vianello, et al.. Bio-inspired stochastic computing using binary CBRAM synapses. IEEE Transactions on Electron Devices, 2013, 60, pp.2402-2408. 10.1109/TED.2013.2263000 . hal-00871918

HAL Id: hal-00871918

<https://hal.science/hal-00871918v1>

Submitted on 25 Jun 2018

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Bio-Inspired Stochastic Computing Using Binary CBRAM Synapses

Manan Suri, *Student Member, IEEE*, Damien Querlioz, *Member, IEEE*, Olivier Bichler, Giorgio Palma, Elisa Vianello, Dominique Vuillaume, Christian Gamrat, and Barbara DeSalvo

Abstract—In this paper, we present an alternative approach to neuromorphic systems based on multi-level resistive memory (RRAM) synapses and deterministic learning rules. We demonstrate an original methodology to use conductive-bridge RAM (CBRAM) devices as, easy to program and low-power, binary synapses with stochastic learning rules. New circuit architecture, programming strategy and probabilistic STDP learning rule for two different CBRAM configurations ‘with-selector (1T-1R)’ and ‘without-selector (1R)’ are proposed. We show two methods (intrinsic and extrinsic) for implementing probabilistic STDP rules. Fully unsupervised learning with binary synapses is illustrated with the help of two example applications: (i) real-time auditory pattern extraction (inspired from a 64-channel silicon cochlea emulator) and (ii) visual pattern extraction (inspired from the processing inside visual cortex). High accuracy (audio pattern sensitivity >2 , video detection rate $>95\%$) and low synaptic-power dissipation (audio $0.55\mu\text{W}$, video $74.2\mu\text{W}$) are shown. The robustness and impact of synaptic parameter variability on system performance is also analyzed.

Index Terms—Stochastic Neuromorphic System, CBRAM Synapse, STDP, Auditory Learning, Visual Pattern Extraction.

I. INTRODUCTION

NEUROMORPHIC and cognitive computing research is gaining importance in recent years. With potential application in fields such as robotics, large-scale data analysis and intelligent autonomous systems, bio-inspired computing paradigms are being investigated as next generation (post-moore) ultra-low power computing solutions. While emulation of spiking neural networks (SNN) in software and Von-Neumann type hardware (such as DSPs, GPUs and FPGAs) has been around for a while, they fail to realize the true potential of bio-inspired computing in terms of low power-dissipation, scalability, reconfigurability and low instruction-execution redundancy [1]. One of the main limitations of Von-Neumann type architectures, while emulating massively parallel asynchronous SNN is the need for very high bandwidths (GHz) to effectively transmit spikes between the memory and the processor, thus leading to high power dissipation and limiting the scalability. The true potential of bio-inspired learning

rules can be realized if they are implemented on optimized special purpose hardware which can provide direct one-to-one mapping with the learning algorithms running on it [2]. Several research groups are actively working on implementing bio-inspired synaptic behavior directly in hardware [3],[4].

Emerging non-volatile resistive memory (RRAM) technologies such as phase-change memory (PCM), conductive-bridge memory (CBRAM) and oxide based memory (OxRAM) have been shown as good candidates for emulation of synaptic plasticity and learning rules like spike-timing dependent plasticity (STDP) [5],[6],[7],[8],[9]. Most recent demonstrations of RRAM based synaptic emulation treat the synapse as a deterministic multi-valued programmable non-volatile resistor. Although such treatment is desirable, it is challenging in terms of actual implementation. Programming schemes for multi-level operation in RRAM devices are more complicated compared to binary operation. Gradual multi-level resistance modulation of RRAM synapses may require generation of successive non-identical neuron spikes (pulses with changing amplitude or width or a combination of both), thus increasing the complexity of the peripheral CMOS neuron circuits which drive the synapses. Pulse trains with increasing amplitude lead to higher power dissipation and parasitic effects on large crossbars. In our previous work we provided a solution (called ‘2-PCM Synapse’) to address the issue of non-identical neuron spikes for multi-valued neuromorphic systems based on PCM synapses [10]. Another issue is that aggressive scaling leads to increased intrinsic device variability. Unavoidable variability complicates the definition and reproducibility of intermediate resistance states in the synaptic devices. In this paper, we present an alternative approach to multi-level synapses. We show a neuromorphic system which uses CBRAM devices as binary synapses with a stochastic-STDP learning rule. At the system level, a functional equivalence [11] exists between deterministic multi-level and stochastic-binary synapses. In the case of supervised NN, several works have exploited this concept [12],[13],[14]. In this work, we use a similar approach for a fully unsupervised SNN. Our approach is also motivated by some works from biology [15], which suggest that STDP learning might be a partially stochastic process in nature.

Section II describes the basics of our CBRAM technology. Experiments of multi-level and stochastic programming are discussed. Section III discusses our simplified STDP learning rule and the synaptic programming methodology. Finally in section IV we present two examples of fully unsupervised learning from complex asynchronous auditory and visual data streams. In the following sections, we use the terms strong-

M. Suri, G. Palma, E. Vianello and B. DeSalvo are with CEA-LETI, Grenoble, France. (e-mail: manan.suri@cea.fr), (barbara.desalvo@cea.fr). The PhD of M.Suri is co-financed by DGA-France. The authors would like to thank Altis Semiconductors for providing CBRAM devices and CNRS/PEPS for financial support.

O. Bichler and C. Gamrat are with CEA, LIST, 91191 Gif-sur-Yvette Cedex, France (e-mail: olivier.bichler@cea.fr)

D. Querlioz is with IEF, Univ. Paris-Sud, CNRS, 91405, Orsay, France.

D. Vuillaume is with IEMN, CNRS, F-59652 Villeneuve d’Ascq, France.

Manuscript received January 08, 2013.

and weak- programming conditions. However these have a relative definition with respect to the technology and materials used for fabricating the CBRAM devices. For the devices presented here, a weak-condition refers to a short pulse width ($<10\mu\text{s}$), usually $1\mu\text{s}$ or 500ns , with a voltage $<2.5\text{V}$ applied at the anode or the bit-line. A strong condition corresponds to a pulse width $>10\mu\text{s}$.

II. CBRAM TECHNOLOGY

1T-1R CBRAM devices (both isolated and in 8×8 matrix), integrated in standard CMOS platform [16], were tested (Fig. 1). A Tungsten (W) plug was used as bottom electrode. The solid electrolyte consisted of a 30nm thick GeS_2 layer deposited by RF-PVD and a 3nm thick layer of Ag deposited by a DC PVD process. The 3nm thick Ag layer is dissolved into the GeS_2 using the photo-diffusion process [17]. Then a 2nd layer of Ag about 75nm thick was deposited to act as top electrode.

CBRAM operating principle relies on the reversible transition from high (reset) to low (set) resistive states owing to the formation and dissolution of a conductive filament in the electrolyte layer. In particular, applying a positive voltage at the Ag electrode results in the drift of Ag^+ ions in the GeS_2 and discharge at the inert counter electrode (W), leading to the growth of Ag dendrites that eventually shunt the top and the bottom electrodes. Upon reversal of voltage polarity, an electrochemical dissolution of the conductive bridge occurs, resetting the system to the OFF (reset) state (Fig. 2). No forming step is required for this device stack. Simple fabrication, CMOS compatibility, high scalability, low power dissipation, and low operating-voltages [18] make CBRAM devices a good choice for the design of synapses in dense neuromorphic systems.

A. Limitations of Multi-level CBRAM Synapses

In literature, CBRAM devices have been proposed to emulate biological synaptic-plasticity by programming the devices in: multiple low-resistance states for emulating long term potentiation (LTP) and multiple high-resistance states for long term depression (LTD) [19],[20]. We demonstrate LTP-like behavior (i.e. gradual ON-state resistance decrease) in our GeS_2 based samples by applying a positive bias at the anode and gradually increasing the select transistor gate voltage (V_g)

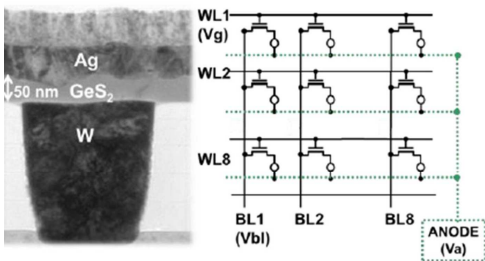


Fig. 1. (Left) TEM of the CBRAM resistor element. (Right) Circuit schematic of the 8×8 1T-1R CBRAM matrix. (note: the devices used in this study had a GeS_2 layer thickness of 30nm . The 50nm TEM is for illustrative purpose only.)

(Fig. 2a). This phenomenon of gradual resistance decrease can be explained with our model [21], assuming a gradual increase in the radius of the conductive filament formed during the set process. Larger gate voltages supply more metal ions leading to the formation of a larger conductive filament during the set process [22].

Nevertheless, this approach implies that each neuron must generate pulses with increasing amplitude while keeping a history of the previous state of the synaptic device, thus leading to additional overhead in the neuron circuitry. Moreover, we found it difficult to reproducibly emulate a gradual LTD-like effect using CBRAM. Fig. 2b shows the abrupt nature of the set-to-reset transition in our devices. Precisely controlling the dissolution of the conductive filament was not possible during the pulsed reset process. Note that for emulating a spiking neural network (SNN) it is essential that both LTP and LTD be implemented by pulse-mode programming of the synaptic devices. Pulse based synaptic programming is an analogue for the neuron spikes or action-potentials.

B. Deterministic and Probabilistic Switching

Fig. 3 shows the On/Off resistance distributions of an isolated 1T-1R CBRAM (during repeated cycles with strong set/reset conditions). The OFF state presents a larger dispersion compared to the ON state. This can be interpreted in terms of non-uniform breaking of the filament during the reset process, due to the unavoidable defects [23],[24] close to the filament which act as preferential sites for dissolution. By fitting the Roff-spread data with our physical model [21], the distribution of the left-over filament-height was computed. Using the computed distribution of the left-over filament height and the equations in [21] we estimated the spread on the voltage (V_{set}) and time (T_{set}) needed for a successful consecutive set operation (Fig. 4). Moreover, when weak-set programming conditions are used immediately after a reset, a probabilistic switching of the device may appear as seen in fig. 5. In fig. 5 the set operation fails in several cycles as the set-programming conditions are not strong enough to switch the device in those cycles.

In a large-scale system, such stochastic switching behavior at weak conditions will get compounded with the inclusion of 'device-to-device' variations. To take into account the device-to-device variability, we performed similar analysis on the matrix devices. Fig. 6 shows the On/Off resistance distributions for all devices cycled 20 times with strong conditions. As expected, the spread on Roff values is larger compared to the Roff spread for a single device shown in fig. 3.

To quantify the trend of probabilistic switching (both set/reset) we designed two simple experiments: a cycling procedure with a strong-set condition and progressively weakening-reset condition was used to determine reset probability (fig. 7a) while a strong-reset condition and progressively weakening set condition was used to determine the set-probability (fig. 7b). As shown in fig. 7, the overall switching probability (criterion for successful switch: $R_{\text{off}}/R_{\text{on}} > 10$), for 64 device matrix, increases with stronger programming conditions. It is thus conceivable to tune the CBRAM device

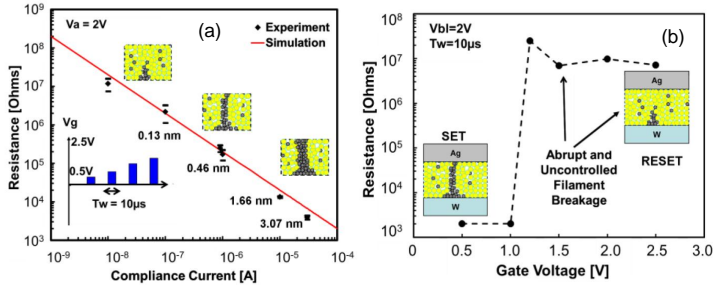


Fig. 2. (a) On-state resistance modulation using current compliance. Fitting using model [21] is also shown (extracted filament radius are indicated). (b) Resistance dependence on gate voltage during the set-to-reset transition.

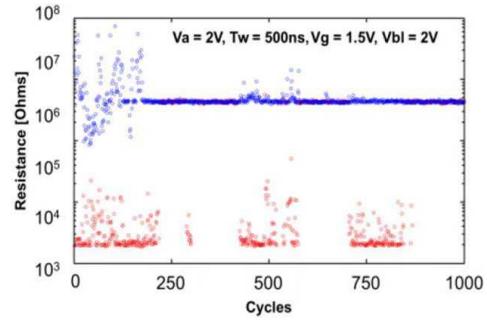


Fig. 5. Stochastic switching of 1T-1R device during 1000 cycles using weak-conditions (switch-probability=0.49).

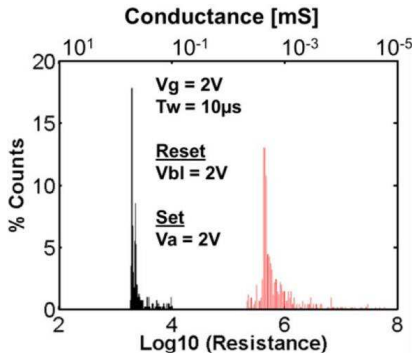


Fig. 3. On/Off resistance distribution of an isolated 1T-1R device during 400 cycles when strong programming is used.

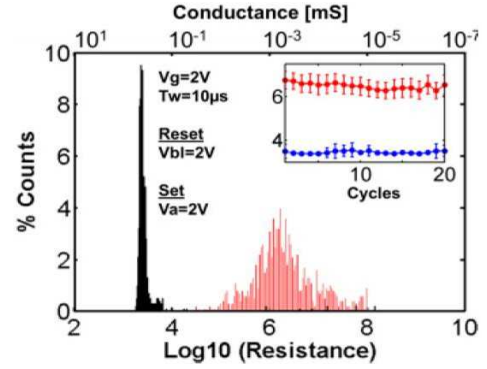


Fig. 6. On/Off resistance distributions of the 64 devices of the 8x8 matrix cycled 20 times. Inset shows Ron and Roff values in log scale with dispersion for each cycle.

switching probability by using the right combination of programming conditions.

III. STOCHASTIC STDP AND PROGRAMMING METHODOLOGY

Fig. 8 shows the core circuit of our architecture. It is similar to the one that we proposed for deterministic synapses in [10],[25] but is adapted for bipolar-devices and stochastic learning rule. The core consists of three main blocks- (i) Input/Output CMOS-neuron circuits (ii) CBRAM synapse-crossbar connecting the neurons. This may be implemented without (1R) or with (1T-1R) selector devices (Fig. 8(a) and (b), respectively), and (iii) Pseudo-random number generator

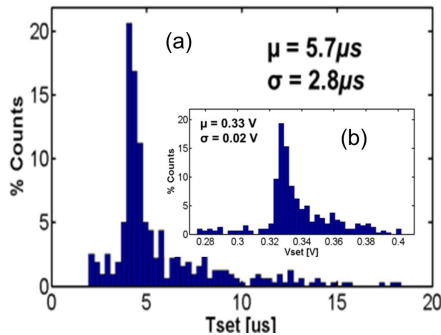


Fig. 4. Computed distributions (generated using Roff data from fig. 3 and model [21], of: (a) Tset and (b) Vset (Inset) values for consecutive successful set operation (mean and sigma are indicated). For computing (a) the applied voltage is 1V and for (b) a ramp rate of 1V/s is used in the quasi-static mode.

(PRNG) circuit. The PRNG block is only used for implementing optional extrinsic stochasticity as explained later. All neurons are modeled as leaky-integrate and fire (LIF) type.

Our stochastic-STDP rule (Fig. 9) is a simplified version of the deterministic biological STDP rule [26]. The optimization of the LTP window and neuron parameters is performed using genetic-evolution algorithm [27]. The STDP rule functions as follows: when an output neuron fires, if the input neuron was active recently (within the LTP time window) the corresponding CBRAM synapse connecting the two neurons, has a given probability to switch into the ON-state (probabilistic LTP). If not, the CBRAM has a given probability to switch to the OFF-state (probabilistic LTD).

Synaptic programming can be implemented using specific voltage pulses. The case without selector device is straightfor-

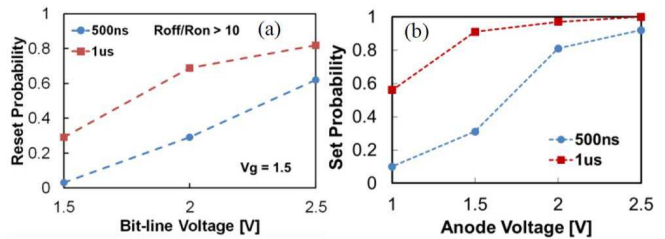


Fig. 7. Overall switching probability for the 64 devices of the matrix (switching being considered successful if Roff/Ron > 10) using (a) weak-reset conditions and (b) weak-set conditions. Vg of 1.5V was used in both experiments.

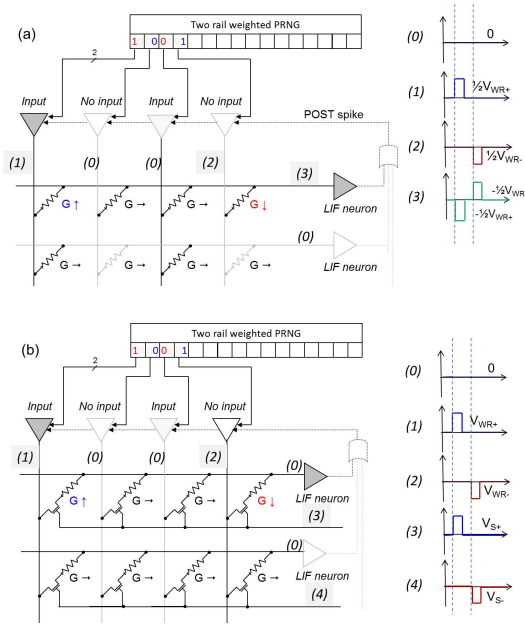


Fig. 8. (a) Circuit schematic with CBRAM synapses without selector devices, LIF neurons, in the external probability case. (b) Circuit schematic with CBRAM synapses with selector devices, LIF neurons, in the external probability case. In both cases, the presented voltages waveforms implement the simplified STDP learning rule for the CBRAMs.

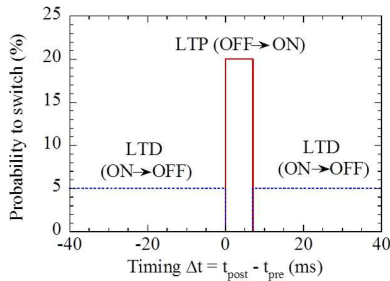


Fig. 9. Probabilistic STDP learning rule (used for audio application). X-axis shows the time difference of post-and pre-neuron spike.

ward (Fig. 8(a)). After an output neuron spikes, it generates a specific voltage waveform (signal (3)). Additionally, the input neurons apply signal (1) if they were active recently (within the LTP time window), else they apply signal (2). The conjunction of the input and output waveforms implements STDP. In the case with selector devices (Fig. 8(b)), the gates are connected to the output neurons as shown. When an output neurons spikes (fires), it applies a specific voltage waveform to the gates of the selector devices (signal (3)), while non-spiking

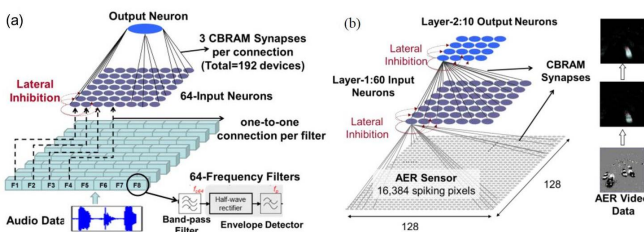


Fig. 10. (a) Single-layer SNN simulated for auditory processing.(b) 2-layer SNN for visual processing.(Right) AER video data snapshot with neuron sensitivity maps.

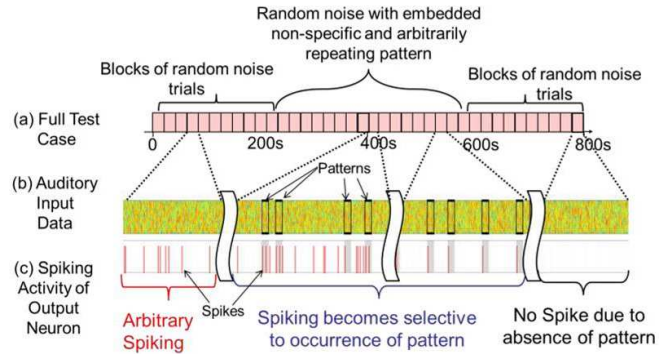


Fig. 11. (a) Full auditory-data test case with noise and embedded repeated patterns. (b) Auditory input data and (c) spiking activity for selected time intervals of the full test case of the output neuron (shown in Fig.16b).

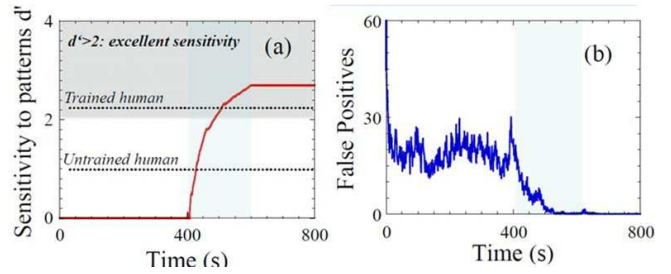


Fig. 12. (a) Pattern Sensitivity (d') for the test case shown in fig. 11. The system reaches a very high sensitivity ($d' > 2$). (b) Number of false detections by the output neuron during the auditory learning.

output neurons will apply signal (4) on the corresponding gates. The input neurons apply pulses similar to the case without selector devices (i.e. signals (1) and (2)). The above described signaling mechanism leads to change in synaptic conductance but does not account for probabilistic or stochastic switching. Probabilistic switching can be implemented in two ways:

- Extrinsically, by multiplying the signal of the input spiking neuron with the PRNG output, whose signal probability can be tuned by combining with logical AND and OR operations several independent PRNGs, that can be implemented for example with linear feedback shift registers (LFSR) [28]. This approach is illustrated in Fig. 8. The PRNG output allows or blocks the input neuron signals according to the defined probability levels.
- Intrinsically, by using weak programming conditions (Figures 5 and 7). In this case, the input neuron applies a weak programming signal, which leads to probabilistic

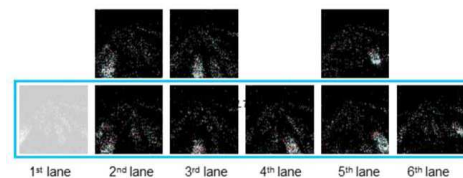


Fig. 13. Final sensitivity map of 9 output neurons from the 1st layer of the neural network shown in Fig.17b. Average detection rate for 5 lanes was 95%.

switching in the CBRAM devices.

Exploiting the intrinsic CBRAM switching probability avoids the presence of the PRNG circuits, thus saving important silicon footprint. It also reduces the programming power, as the programming pulses are weaker compared to the ones used for deterministic switching. However it might be difficult to precisely control the switching probability of individual synapses using weak-conditions in a large-scale system. When weak programming conditions are used, both 'device-to-device' and 'cycle-to-cycle' variations contribute to probabilistic switching. Decoupling the effect of the two types of variations is not straightforward in filamentary type of devices (due to the spread on left-over filament height post-reset). In order to precisely control the switching probability a better understanding and modeling of the device phenomena at weak programming conditions is required. If precise values of switching probability are desired then extrinsic PRNG circuits should be used. For instance a 2-bit PRNG control signal as shown in Fig. 8 can be used to separately tune the LTP and LTD probability. The core with and without selector devices are equivalent from a functional point of view. Selector-free configuration is the most compact ($4F^2$) and highest CBRAM integration density can be obtained with it. Although adding selector element consumes more area ($>4F^2$), it helps to reduce the sneak-path leakage and unwanted device disturbs during the STDP operation which are difficult to control with just 1R devices. Since we did not fabricate a full test chip to measure the leakage and disturb effects in the 1R case, the simulations described in Section IV are based on synaptic programming methodology with-selector devices (1T-1R).

IV. AUDITORY AND VISUAL PROCESSING SIMULATIONS

We performed full system-level simulations with our special purpose event-based Xnet simulator tool [10],[27],[25]. The neuron circuits are modeled with behavioral equations as in [25],[27]. The synapses are modeled by fitting data of Fig. 3 and Fig. 6 with a log-normal distribution, in order to take into account the experimental spread in the conductance parameters. Effect of both 'device-to-device' and 'cycle to cycle' variations are captured in the synapse model. Two different SNN were used to process auditory and visual data. Fig. 10a shows the network designed to learn, extract, and recognize hidden patterns in auditory data. Temporally encoded auditory data is filtered and processed using a 64-channel silicon cochlea emulator (similar to [29], simulated within Xnet). The processed data is then presented to a single layer feed-forward SNN with 192-CBRAM synapses (i.e. every channel of the cochlea is connected to the output neuron by 3 CBRAM synapses). Initially (from 0 to 400s), gaussian audio noise is used as input to the system, and the firing pattern of the output neuron is completely random (as seen in Fig. 11). Then (from 400 to 600s), an arbitrarily created pattern is embedded in the input noise data and repeated at random intervals. Within this time frame, the output neuron starts to spike predominantly when the pattern occurs, before becoming entirely selective to it at the end of the sequence. This is well seen on the sensitivity d' (a standard measurement in signal

detection theory) presented in Fig. 12a, which grows from 0 to 2.7. By comparison, a trained human on the same problem achieves a sensitivity of approximately 2 [30]. During the same period, the number of false positives also decreases to nearly 0 (Fig. 12b). At the end of the test case (from 600 to 800s), pure noise (without embedded patterns) is again presented to the system. As expected, the output neuron does not activate at all, i.e. no false positive is seen (Fig. 11,12). The total synaptic learning power consumption (i.e. the power required to read, write and erase the CBRAMs) was extremely low ($0.55 \mu\text{W}$ in the extrinsic probability case, $0.15 \mu\text{W}$ in the intrinsic probability case). The estimation of synaptic learning power is described in detail in Tab.1[6], following equations were used:

$$E_{\text{set/reset}} = V_{\text{set/reset}} \times I_{\text{set/reset}} \times t_{\text{pulse}}$$

$$E_{\text{total}} = (E_{\text{set}} \times \text{total set events}) + (E_{\text{reset}} \times \text{total reset events})$$

$$\text{Power}_{\text{synaptic learning}} = E_{\text{total}} / \text{Duration}_{\text{learning}}$$

In the extrinsic probability case, about 90% of the energy was used to program the CBRAM devices, and about 10% to read them (while in the case of intrinsic probability it was about 81% and 19% respectively). The sound pattern extraction example can act as a prototype for implementing more complex applications such as speech recognition and sound-source localization. Fig. 10b shows the network simulated to process temporally encoded video data, recorded directly from an artificial silicon retina [31]. A video of cars passing on a freeway recorded in address-event-representation (AER) format by the authors of [31] is presented to a 2-layered SNN. In each layer, every input is connected to every output by a single CBRAM synapse. The CBRAM based system learns to recognize the driving lanes, extract car-shapes (Fig. 13) and orientations, with more than 95% average detection rate. The total synaptic-power dissipation was $74.2 \mu\text{W}$, in the extrinsic probability case and $21 \mu\text{W}$ in the intrinsic probability case. This detection rate is similar to the one that we simulated on the same video test case with a deterministic system based on multi-level PCM synapses [10],[32],[33]. The example SNN on visual pattern extraction, shown here, can be used as a prototype to realize more complex functions such as image classification [34],[25], position detection and target-tracking. We tested the two test applications with both extrinsic and intrinsic probability programming methodologies. Sensitivity and detection rates were nearly identical in both cases, which suggests a relative equivalence of the two approaches. Total synaptic power consumption was lower when the intrinsic probability methodology was used. This suggests that the power saved by using weak programming pulses is greater than the power dissipated due to the extra programming pulses required to implement the intrinsic probability. Additionally, we performed simulations without any intrinsic or extrinsic conductance spreads (ideal or non-variable synapses). These gave sensitivity values and detection rates similar to the ones when the spread was considered, suggesting that the experimentally measured variability in our devices had no significant impact on the overall system learning performance. This is consistent with variability-tolerance of STDP-based networks [25].

V. CONCLUSION

We proposed for the very first time a bio-inspired system with binary CBRAM synapses and stochastic STDP learning rule able to process asynchronous analog data streams for recognition and extraction of repetitive patterns in a fully unsupervised way. The demonstrated applications exhibit very high performance (auditory pattern sensitivity >2.5 , video detection rate $>95\%$) and ultra-low synaptic power dissipation (audio $0.55\mu\text{W}$, video $74.2\mu\text{W}$) in the learning mode. We show different programming strategies for 1R and 1T-1R based CBRAM configurations. Intrinsic and extrinsic programming methodology for CBRAM synapses is also discussed.

REFERENCES

- [1] A. Muthuramalingam, S. Himavathi, and E. Srinivasan, "Neural network implementation using fpga: issues and application," *International journal of information technology*, vol. 4, no. 2, pp. 86–92, 2008.
- [2] J. Arthur, P. Merolla, F. Akopyan, R. Alvarez, A. Cassidy, S. Chandra, S. Esser, N. Imam, W. Risk, D. Rubin, R. Manohar, and D. Modha, "Building block of a programmable neuromorphic substrate: A digital neurosynaptic core," in *Neural Networks (IJCNN), The 2012 International Joint Conference on*, June 2012, pp. 1–8.
- [3] G. Snider, "Spike-timing-dependent learning in memristive nanodevices," in *Prof. of IEEE International Symposium on Nanoscale Architectures 2008 (NANOARCH)*, 2008, pp. 85–92.
- [4] C. Zamarreno-Ramos, L. A. Camunas-Mesa, J. A. Perez-Carrasco, T. Masquelier, T. Serrano-Gotarredona, and B. Linares-Barranco, "On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex," *Front. Neurosci.*, vol. 5, 2011.
- [5] D. Kuzum, R. Jeyasingh, and H.-S. Wong, "Energy Efficient Programming of Nanoelectronic Synaptic Devices for Large-Scale Implementation of Associative and Temporal Sequence Learning," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011.
- [6] M. Suri, O. Bichler, D. Querlioz, G. Palma, E. Vianello, D. Vuillaume, C. Gamrat, and B. DeSalvo, "CBRAM Devices as Binary Synapses for Low-Power Stochastic Neuromorphic Systems: Auditory (Cochlea) and Visual (Retina) Cognitive Processing Applications," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, p. 10.3.
- [7] S. Park, H. Kim, M. Choo, J. Noh, A. Sheri, C. Park, S. Jung, K. Seo, J. Park, S. Kim, W. Lee, J. Shin, D. Lee, G. Choi, J. Woo, E. Cha, Y. Kim, C. Kim, U. Chung, M. Jeon, B. Lee, B. Lee, and H. Hwang, "RRAM-based Synapse for Neuromorphic System with Pattern Recognition Function," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, p. 10.2.
- [8] S. Yu, B. Gao, Z. Fang, H. Yu, J. Kang, and H. Wong, "A Neuromorphic Visual System Using RRAM Synaptic Devices with Sub-pJ Energy and Tolerance to Variability: Experimental Characterization and Large-Scale Modeling," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, p. 10.4.
- [9] M. Suri, O. Bichler, Q. Hubert, L. Perniola, V. Sousa, C. Jahan, D. Vuillaume, C. Gamrat, and B. DeSalvo, "Interface engineering of pcm for improved synaptic performance in neuromorphic systems," in *Memory Workshop (IMW), 2012 4th IEEE International*, 2012, pp. 1–4.
- [10] M. Suri, O. Bichler, D. Querlioz, O. Cueto, L. Perniola, V. Sousa, D. Vuillaume, C. Gamrat, and B. DeSalvo, "Phase Change Memory as Synapse for Ultra-Dense Neuromorphic Systems: Application to Complex Visual Pattern Extraction," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011.
- [11] D. H. Goldberg, G. Cauwenberghs, and A. G. Andreou, "Probabilistic synaptic weighting in a reconfigurable network of vlsi integrate-and-fire neurons," *Neural Networks*, vol. 14, no. 6-7, pp. 781–793, 2001.
- [12] W. Senn and S. Fusi, "Convergence of stochastic learning in perceptrons with binary synapses," *Phys. Rev. E*, vol. 71, p. 061907, Jun 2005.
- [13] J. H. Lee and K. K. Likharev, "Defect-tolerant nanoelectronic pattern classifiers," *Int. J. Circuit Theory Appl.*, vol. 35, no. 3, pp. 239–264, May 2007.
- [14] Y. Kondo and Y. Sawada, "Functional abilities of a stochastic logic neural network," *Neural Networks, IEEE Transactions on*, vol. 3, no. 3, pp. 434–443, May 1992.
- [15] P. Appleby and T. Elliott, "Stable competitive dynamics emerge from multispike interactions in a stochastic model of spike-timing-dependent plasticity," *Neural computation*, vol. 18, no. 10, pp. 2414–2464, 2006.
- [16] C. Gopalan, Y. Ma, T. Gallo, J. Wang, E. Runnion, J. Saenz, F. Koushan, P. Blanchard, and S. Hollmer, "Demonstration of conductive bridging random access memory (cbram) in logic cmos process," *Solid-State Electronics*, vol. 58, no. 1, pp. 54–61, 2011.
- [17] E. Vianello, C. Cagli, G. Molas, E. Souchier, P. Blaise, C. Carabasse, G. Rodriguez, V. Jousseau, B. De Salvo, F. Longnos, F. Dahmani, P. Verrier, D. Bretegnier, and J. Liebault, "On the impact of ag doping on performance and reliability of ges2-based conductive bridge memories," in *Solid-State Device Research Conference (ESSDERC), 2012 Proceedings of the European*, Sept. 2012, pp. 278–281.
- [18] M. Kund, G. Beitel, C.-U. Pinnow, T. Rohr, J. Schumann, R. Symanczyk, K.-D. Ufert, and G. Muller, "Conductive bridging ram (cbram): an emerging non-volatile memory technology scalable to sub 20nm," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, Dec. 2005, pp. 754–757.
- [19] S. Yu and H.-S. Wong, "Modeling the switching dynamics of programmable-metallization-cell (PMC) memory and its application as synapse device for a neuromorphic computation system," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, pp. 22.1.1–22.1.4.
- [20] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale Memristor Device as Synapse in Neuromorphic Systems," *Nano Letters*, vol. 10, no. 4, pp. 1297–1301, 2010.
- [21] G. Palma, E. Vianello, C. Cagli, G. Molas, M. Reyboz, P. Blaise, B. De Salvo, F. Longnos, and F. Dahmani, "Experimental investigation and empirical modeling of the set and reset kinetics of ag-ges2 conductive bridging memories," in *Memory Workshop (IMW), 2012 4th IEEE International*, 2012, pp. 1–4.
- [22] S. Yu and H.-S. Wong, "Compact modeling of conducting-bridge random-access memory (cbram)," *Electron Devices, IEEE Transactions on*, vol. 58, no. 5, pp. 1352–1360, May 2011.
- [23] S. Choi, S. Ambrogio, S. Balatti, F. Nardi, and D. Ielmini, "Resistance drift model for conductive-bridge (cb) ram by filament surface relaxation," in *Memory Workshop (IMW), 2012 4th IEEE International*, 2012, pp. 1–4.
- [24] D. Ielmini, F. Nardi, and C. Cagli, "Resistance-dependent amplitude of random telegraph-signal noise in resistive switching memories," *Applied Physics Letters*, vol. 96, no. 5, p. 053503, 2010.
- [25] D. Querlioz, O. Bichler, and C. Gamrat, "Simulation of a memristor-based spiking neural network immune to device variations," *Proc. of the Int. Joint Conf. on Neural Networks (IJCNN)*, pp. 1775–1781, 2011.
- [26] G.-Q. Bi and M.-M. Poo, "Synaptic modifications in cultured hippocampal neurons: Dependence on spike timing, synaptic strength, and postsynaptic cell type," *Journal of Neuroscience*, vol. 18, pp. 10464–10472, 1998.
- [27] O. Bichler, D. Querlioz, S. J. Thorpe, J.-P. Bourgoin, and C. Gamrat, "Extraction of temporally correlated features from dynamic vision sensors with spike-timing-dependent plasticity," *Neural Networks*, vol. 32, pp. 339–348, 2012.
- [28] F. Brglez, C. Gloster, and G. Kedem, "Hardware-based weighted random pattern generation for boundary scan," in *Test Conference, 1989. Proceedings. Meeting the Tests of Time., International*, 1989, pp. 264–274.
- [29] V. Chan, S.-C. Liu, and A. van Schaik, "Aer ear: A matched silicon cochlea pair with address event representation interface," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 54, no. 1, pp. 48–59, 2007.
- [30] T. R. Agus, S. J. Thorpe, and D. Pressnitzer, "Rapid formation of robust auditory memories: Insights from noise," *Neuron*, vol. 66, no. 4, pp. 610–618, 2010.
- [31] P. Lichtsteiner, C. Posch, and T. Delbruck, "A 128 x 128 120 dB 15 μs Latency Asynchronous Temporal Contrast Vision Sensor," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 2, pp. 566–576, 2008.
- [32] M. Suri, O. Bichler, D. Querlioz, B. Traore, O. Cueto, L. Perniola, V. Sousa, D. Vuillaume, C. Gamrat, and B. DeSalvo, "Physical aspects of low power synapses based on phase change memory devices," *Journal of Applied Physics*, vol. 112, no. 5, pp. 054904–10, Sep 2012.
- [33] O. Bichler, M. Suri, D. Querlioz, D. Vuillaume, B. DeSalvo, and C. Gamrat, "Visual pattern extraction using energy-efficient 2-pcm synapse neuromorphic architecture," *Electron Devices, IEEE Transactions on*, vol. 59, no. 8, pp. 2206–2214, Aug 2012.
- [34] T. Masquelier and S. J. Thorpe, "Unsupervised learning of visual features through spike timing dependent plasticity," *PLoS Comput Biol*, vol. 3, no. 2, p. e31, 2007.



Manan Suri received the M.Eng. and B.S. degrees in electrical and computer engineering from Cornell University, Ithaca, USA, in 2010 and 2009 respectively. He is currently working toward the Ph.D. degree in the Advanced Memory Technology Laboratory, CEA-LETI, Grenoble, France. He works on emerging NV memory technology and neuromorphic computing.



Dominique Vuillaume received the Habilitation diploma in solid-state physics from the University of Lille, Lille, in 1992. He is a Research Director with the Centre National de la Recherche Scientifique, Paris, France. He is working on molecular electronics.



Damien Querlioz received the Ph.D. degree from the Université Paris-Sud, Orsay, France, in 2008. He is a CNRS Research Scientist with the Université Paris-Sud. He develops new concepts in nanoelectronics relying on bioinspiration.



Olivier Bichler received the M.S. degree in embedded systems from the Ecole Normale Supérieure de Cachan, France, in 2009 and the Ph. D. degree from the Université Paris-Sud, Orsay, France, in 2012. He is now a Research Engineer at CEA LIST, France, and develops novel architectures based on nanoelectronics and bio-inspired neuromorphic computing.



Christian Gamrat received the M.S. degree in information processing from École Nationale Supérieure d'Électronique et de Radioélectricité, Grenoble, in 1993. He is a Senior Expert with the CEA-LIST, Gif-sur-Yvette, France, where he is a Chief Scientist.



Giorgio Palma received the M.S. degree in materials science and engineering from University di Milano-Bicocca, Milano, Italy, in 2010. He is currently working toward the Ph.D degree in the Advanced Memory Technology Laboratory, CEA-LETI, Grenoble, France.



Barbara DeSalvo received the Ph.D. degree in microelectronics from the Polytechnic Institute of Grenoble, France. Since 1999, she has been a Scientist with the CEA-LETI, Grenoble, France where she currently heads the CMOS and memory labs.



Elisa Vianello Elisa Vianello received the Ph.D. degree in microelectronics from the University of Udine, Italy, and Polytechnic Institute of Grenoble, France, in 2009. Since 2011, she has been a Scientist with the CEA-LETI, Grenoble, France.