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Giuseppe Moschetti [a,*], Eric Lefebvre [a,c], Martin Fagerlind [a,d], Per-Åke Nilsson [a], Ludovic Desplanque [b], Xavier Wallart [b], Jan Grahn [a]

[a] *Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-412 96 Göteborg, Sweden*
[b] *Institute of Electronics, Microelectronics and Nanotechnology, IEMN/CNRS UMR 8520, University of Lille, Av. Poincaré, 59652 Villeneuve d'Ascq, France*
[c] *OSRAM Opto Semiconductors GmbH, 93055 Regensburg, Germany*
[d] *NXP Semiconductors, Gerstweg 2, 6534 AE Nijmegen, Netherlands*

A new method for avoiding air exposure of the mesa-floor during processing of shallow-mesa InAs/AlSb HEMTs is reported. The method is based on the *in situ* chemical vapor deposition (CVD) of a SiN_x-film, right after the shallow-mesa dry-etch process. The *in situ* CVD method allows also growing a dielectric film up to five times thicker than in previous reports of similar early-protection approach. Devices featur-ing a 25 nm SiN_x-film enabled by the *in situ* CVD method are compared to devices based on a previously developed process, where the mesa floor is protected by a 2 nm SiN_x-film deposited by *ex situ* reactive sputtering (RS). Microscopy observations revealed that the new process is more robust, ensuring a long-term stability against oxidation. DC, RF and noise performance were measured for 110 nm gate-length HEMTs. Devices based on the CVD process demonstrated higher peak transconductance (+13%), elevated I_{on}/I_{off} ratio (factor 4.7) and one order of magnitude lower gate current leakage. The cut-off fre-quency f_T and the maximum oscillation frequency f_{max} at a drain–source voltage of 0.3 V increased up to 175 GHz (+20%) and 130 GHz (+18%), respectively. Moreover, the extracted minimum noise figure for the InAs/AlSb HEMT using the *in situ* CVD early-protection was 1.4 dB at 6 GHz, instead of 2.3 dB for the RS based devices.

1. Introduction

The high electron mobility and peak velocity of the pure InAs channel, combined with a very large conduction band discontinuity between InAs and AlSb, make the InAs/AlSb high electron mobility transistor (HEMT) suitable for high-frequency and low-noise applications [1]. In addition, thanks to the low bandgap of the InAs channel, the InAs/AlSb HEMT can exhibit performance comparable to the InP HEMT, but at one fourth of its power consumption [2–4]. However, the lack of an insulating substrate material lattice matched to InAs makes it necessary to grow the active HEMT structure on a metamorphic, relatively thick (1–2 μm) buffer of AlSb on the GaAs or InP substrate [5]. Since the AlSb compound is extremely prone to oxidation, the presence of such a thick AlSb buffer poses huge challenges during any device processing of InAs/AlSb HEMTs [6]. To mitigate this, a more chemically stable AlGaSb buffer layer is normally grown on top of the AlSb buffer hence preventing its oxidation [7]. Transistor isolation is carried out by dry etching of a shallow-mesa down to the AlGaSb buffer layer [8,9]. However, the long term stability of the devices still presents a problem, as AlGaSb oxidation was for instance observed during device reliability investigations [10]. As a solution, an early-protection approach was proposed by depositing a thin dielectric film on the AlGaSb mesa-floor immediately after the etching of the shallow-mesa, but leaving the HEMT active areas uncovered to not modify the other process steps [11–13]. Lin et al. utilized a 5 nm SiO_2-film deposited by electron beam evaporation. Lefebvre et al. utilized a 2 nm SiN_x-film (hereafter denoted as SiN-film) deposited by reactive sputtering (RS). Even though improved device characteristics were reported, both approaches implied air exposure of the AlGaSb surface prior to the deposition of a thin protective layer. As a result, unavoidable oxidation of the HEMTs may occur during processing, acting detrimental to long-term device stability.

Here we report a fabrication process for shallow-mesa InAs/AlSb HEMTs with an early-protection having a better reproducibility than the RS-SiN method. By utilizing a dual chamber RIE/CVD system, the shallow AlGaSb mesa-floor can be protected by a SiN film directly after etch without breaking vacuum, in other words

* Corresponding author. Tel.: +46 31 7725049; fax: +46 31 16 45 13.
E-mail address: giuseppe.moschetti@chalmers.se (G. Moschetti).

in situ. The early-protection is carried out by chemical vapor deposition (CVD) of a 25 nm thick SiN-film, i.e. at least 5 times thicker than earlier reported values. InAs/AlSb HEMTs with 110 nm recessed gates were fabricated in parallel using the previous *ex situ* RS-SiN method and the new CVD-SiN method. Comparison of the two approaches through DC, RF and noise measurements demonstrated that the new process largely enhanced performance of the InAs/AlSb HEMTs.

2. Device fabrication and related observation

The InAs/AlSb HEMT epitaxial structure was grown by molecular beam epitaxy on an InP substrate. After an initial 100 nm thick $In_{50}Al_{50}As$ smoothing layer, a metamorphic buffer formed by a 700 nm AlSb layer and a 250 nm $Al_{80}Ga_{20}Sb$ layer was grown to accommodate the lattice mismatch (3.2%) between the InP substrate and the InAs channel. The HEMT structure started with a 50 nm AlSb bottom barrier and a 15 nm InAs channel, followed by a 5 nm AlSb spacer and a 8 nm AlSb Schottky layer, with a 4×10^{12} cm^{-2} Te doping-plane in between. A 4 nm $In_{50}Al_{50}As$ layer was then added to protect the AlSb Schottky layer during the gate-recess etch process [14], before a 5 nm Si-doped InAs cap layer was finally grown. A schematic of the epitaxial structure is shown in Fig. 1. Hall measurements at 300 K showed an electron mobility of 19,700 cm^2/V s and an electron concentration of 2.6×10^{12} cm^{-2}.

The fabrication of the CVD-SiN InAs/AlSb HEMTs started by patterning a 1 μm thick photo-resist etch mask. The shallow-mesas were then defined in one of the chambers of a dual chamber Oxford Plasmalab ICP/CVD system, using a Cl_2:Ar dry etching process stopped in the AlGaSb buffer layer. Without breaking vacuum, the chip was transferred into the second chamber, where the chemical vapor deposition of a 25 nm SiN-film was performed. Then the photo-resist etch mask was dissolved in acetone with ultra-sonic assistance, hence removing the SiN-film from the mesa, while leaving the AlGaSb mesa-floor protected. Pd/Pt/Au ohmic contacts with a source–drain distance of 2 μm were subsequently defined by optical lithography, deposited by evaporation and annealed in a H_2/Ar (1:9) ambient at 275° C for 15 min. Ti/Pt/Au T-shaped gates with a 110 nm length were evaporated on the $In_{50}Al_{50}As$ layer after gate-recess wet-etching, using a two-layer resist mask defined by e-beam lithography. Probing contacts were then defined by optical lithography and sputtering of Ti/Au. Finally, an 80 nm thick SiN-film was deposited by reactive sputtering.

The afore-mentioned InAs/AlSb HEMTs were compared with transistors fabricated on the same epitaxial material and in an identical way, except for the early-protection of the mesa-floor. After the dry etching step, the sample was immediately transferred into the load-lock of a sputtering system, for the *ex situ* deposition of the SiN-film. Its thickness was limited to 2 nm to ensure successful subsequent lift-off of the film, as issues of resist encapsulation with thicker RS-SiN films have been observed [13]. An issue with such a thin film is that it may not offer a complete protection against oxidation of the AlGaSb mesa-floor, especially considering the previously observed cracks on the surface of InAs/AlSb HEMT epitaxial wafers [15]. These cracks may act as a preferential etching place during the shallow-mesa dry etching, leading to cavities in the exposed AlGaSb buffer layer, as observed by scanning electron microscopy (SEM) and shown in Fig. 2. As a result, due to a shadowing effect, the wall and the floor of these cavities (possibly reaching the underlying AlSb buffer) may not be covered by a too thin early-protection film. From monitoring by optical microscopy, local oxidation was observed when using the RS-SiN process. This was not the case for InAs/AlSb HEMTs fabricated with the *in situ* CVD method, which permits a better coverage by an increased SiN-film thickness, without subsequent lift-off issue. This, combined with the non-exposure to air of the AlGaSb mesa-floor prior to early-protection, makes the *in situ* CVD method more robust than the RS method: *in situ* CVD protected samples have been monitored for more than two and a half years after fabrication without detecting any oxidation.

InAs cap	50 Å
$In_{50}Al_{50}As$ protection	40 Å
AlSb Schottky layer	80 Å
Te -doping	4x10^{12} cm^{-2}
AlSb buffer	50 Å
InAs Channel	150 Å
AlSb buffer	500 Å
$Al_{80}Ga_{20}Sb$ buffer	2500 Å
AlSb buffer	7000 Å
$In_{50}Al_{50}As$	1000 Å
S.I. InP Substrate	

Fig. 1. Schematic cross section of the InAs/AlSb HEMT epitaxial structure.

3. DC characterization

On-wafer DC measurements have been performed using an HP4156B semiconductor parameter analyzer. InAs/AlSb HEMTs with 110 nm gate length and 2×50 μm gate width were characterized. All the transistor measurements have been limited to a drain–source bias up to 0.3 V as we observed that higher values will result in irreversible device degradation detrimental for low-noise application. The degradation is likely caused by impact ionization and is observed independently of fabrication process, also for devices without SiN film protection. On both chips, a low contact resistivity of about $0.04 \pm 0.003\ \Omega$ mm was extracted from measurements on transfer length method structures.

In Fig. 3, the drain–source current I_{DS} versus V_{DS} is shown. For InAs/AlSb HEMTs protected by RS-SiN and CVD-SiN, the maximum I_{DS} at $V_{DS} = 0.3$ V and $V_{GS} = 0$ V is 510 mA/mm and 580 mA/mm, respectively. For both devices, a relatively large output conductance g_{DS} (i.e. non-saturated I_{DS}) for a gate–source bias V_{GS} close

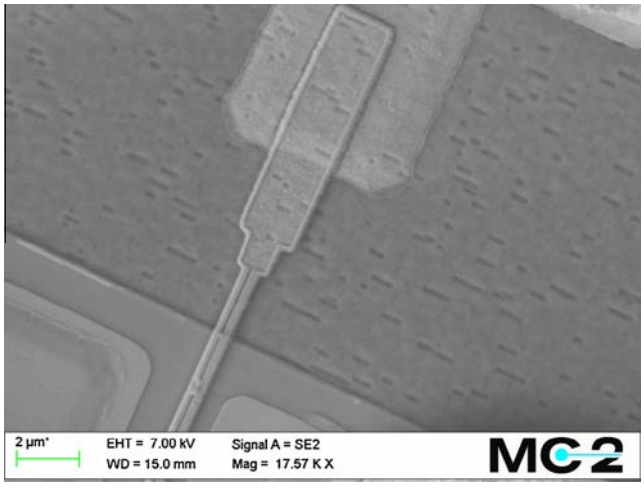

Fig. 2. Scanning electron microscopy view of the extrinsic region of a InAs/AlSb HEMT showing cracks on the AlGaSb mesa-floor. The depicted device is protected with a 25 nm *in situ* CVD-SiN film.

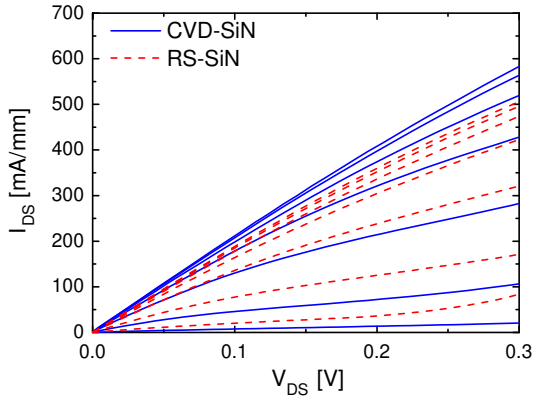

Fig. 3. $I_{DS}(V_{DS})$ with V_{GS} ranging from 0 V to −1.2 V in steps of 0.2 V.

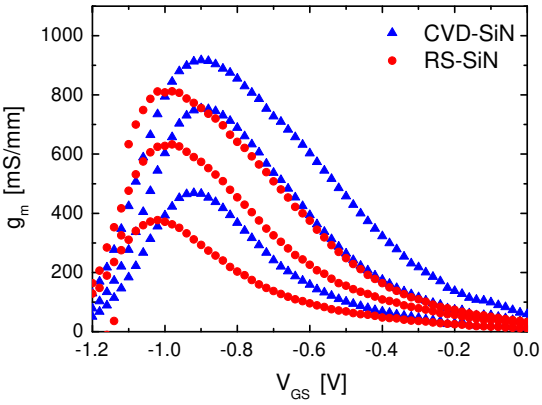

Fig. 4. $g_m(V_{GS})$ with V_{DS} ranging from 0.1 V to 0.3 V in steps of 0.1 V.

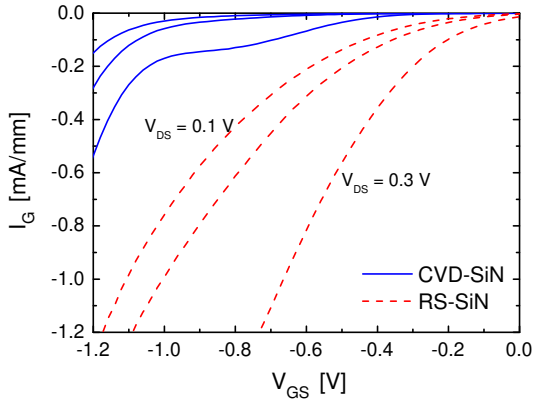

Fig. 5. $I_G(V_{GS})$ with V_{DS} ranging from 0.1 V to 0.3 V in steps of 0.1 V.

to 0 V can be observed. The pinch-off of the current is however better for the CVD-SiN device, with an I_{on}/I_{off} ratio at V_{DS} = 0.3 V of 28 instead of 6 for its RS-SiN counterpart. The transconductance g_m as a function of V_{GS} is shown in Fig. 4. The shift of the g_m peaks for the CVD-SiN process toward less negative V_{GS} values can be related to the relatively lower g_{DS} observed in Fig. 3. Moreover, the g_m peak shift is also associated with the shift in the threshold voltage, V_{th}, from −1.38 V (RS-SiN) to −1.25 V (CVD-SiN). Peak values of g_m are 23%, 19% and 13% higher for the CVD-SiN based device than the RS-SiN HEMT at drain biases of 0.1 V, 0.2 V and 0.3 V, respectively. The evolutions of the gate current leakage I_G versus V_{GS}, depicted in Fig. 5, reveals a larger difference between the RS-SiN and the CVD-SiN devices, with I_G being up to one order of magnitude reduced in the latter case. In Fig. 6, I_{DS} and I_G are plotted versus

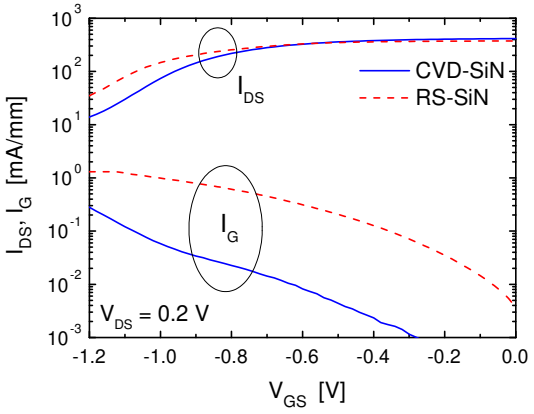

Fig. 6. Subthreshold gate and drain current characteristics at V_{DS} = 0.2 V.

V_{GS} on logarithmic scale for a V_{DS} bias of 0.2 V. The improvement on I_G when using the CVD-SiN process is confirmed. Moreover, the subthreshold slope extracted from the I_{DS} versus V_{GS} curve is reduced to 260 mV/dec instead of 300 mV/dec for the RS-SiN device.

The overall better DC behavior of the CVD-SiN devices is ascribed to the better electrical isolation provided by the thicker SiN-film. Basically, the use of a SiN-film as early protection does not only prevent the AlGaSb mesa-floor oxidation, it also improves the electrical isolation between the extrinsic part of the gate and the source/drain probing pads deposited on it, which otherwise depends on the remaining thickness of the AlGaSb layer [9]. Similarly, a thicker SiN-film does not only prevent local oxidation by efficiently covering the cavities on the AlGaSb mesa-floor, it also avoids any electrical contact between the gate or pads metals and the underlying AlGaSb alloy, likely to happen in uncovered cavities. As a result, for a CVD-SiN device, the electrical isolation around the device mesa is improved, I_G is reduced and the pinching-behavior improved thanks to a more efficient gate control.

4. RF and Noise characterization

S-parameter measurements have been performed on-wafer up to a frequency of 50 GHz using an Agilent vector network analyzer.

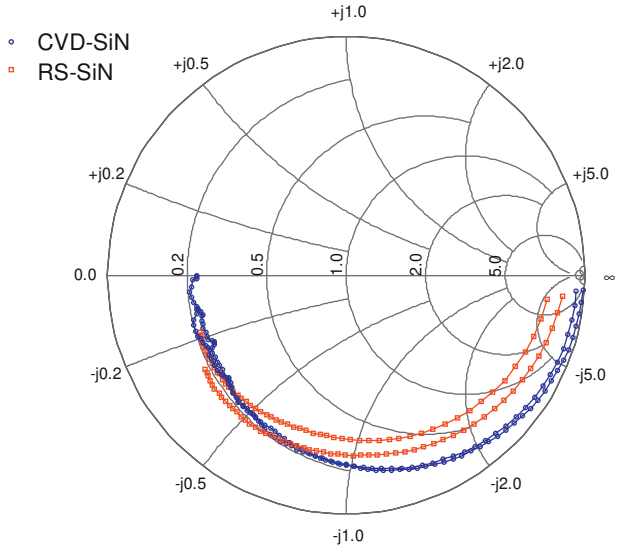

Fig. 7. Input reflection coefficient S_{11} at a drain bias V_{DS} of 0.1 V and 0.3 V at frequency ranging from 1 to 55 GHz.

Table 1
Small-signal parameters at V_{DS} = 0.3 V for the RS-SiN and CVD-SiN devices.

V_{DS} (V)	RS-SiN	CVD-SiN	Factor
R_{gs} (kΩ)	4.3	55	13
R_{gd} (kΩ)	1.8	20	11
C_{pg} (fF)	10	15	1.5
C_{pd} (fF)	10	15	1.5
R_d (Ω)	2.3	1.9	0.8
R_s (Ω)	1.7	1.2	0.7
C_{gs} (fF)	50	55	1.1
C_{gd} (fF)	28	50	1.8
g_{ds} (mS)	36	24	0.7
g_m (mS)	89	101	1.1

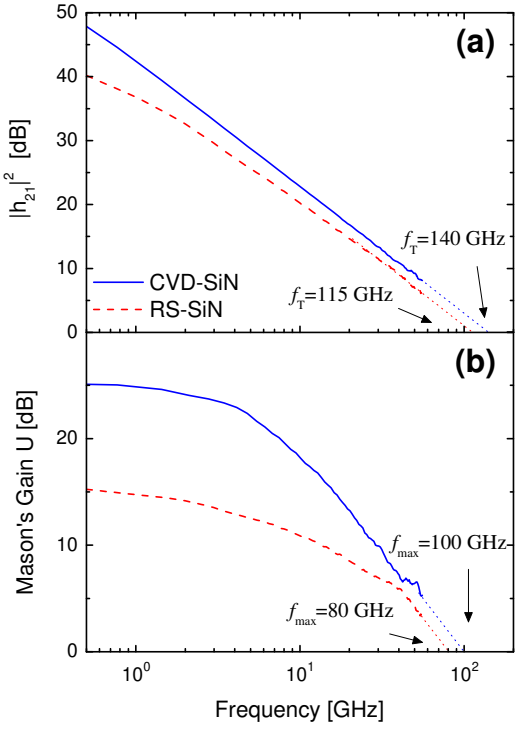

Fig. 8. Evolution versus frequency at V_{DS} = 0.2 V of (a) the current gain $|h_{21}|^2$ and (b) the Mason's gain U.

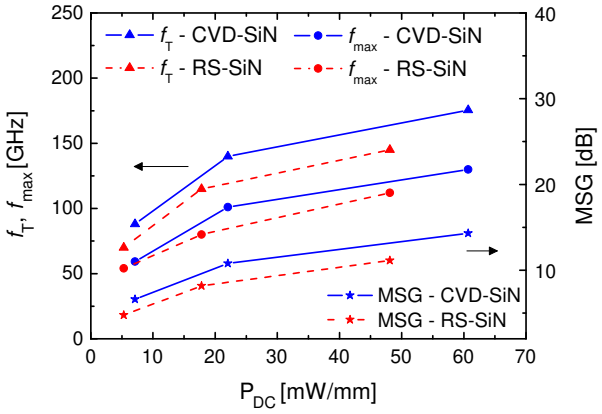

Fig. 9. f_T, f_{max} and MSG versus DC power consumption with V_{DS} swept from 0.1 to 0.3 V in steps of 0.1 V. The MSG is measured at 40 GHz.

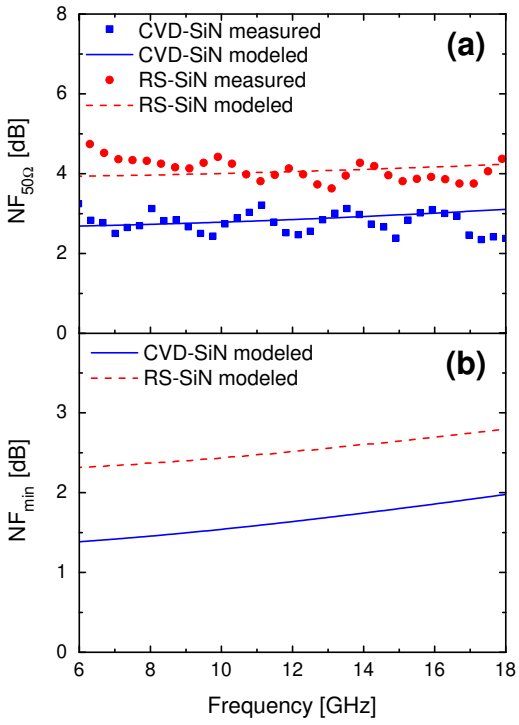

Fig. 10. Evolution versus frequency at V_{DS} = 0.2 V of (a) the measured and modeled $NF_{50Ω}$ and (b) the modeled NF_{min}. The standing wave pattern in the measurements is due to the not optimal matching to 50 Ω of the 2 × 50 μm device layout at the measured frequencies.

An off-wafer Line–Reflect–Reflect–Match (LRRM) calibration technique on an impedance standard substrate was used. Noise measurements at 50 Ω have been performed using an Agilent N9030A noise figure analyzer.

In Fig. 7, the input reflection coefficient S_{11} at V_{DS} of 0.1 V and 0.3 V is shown for both devices. Compared to the RS-SiN device, the CVD-SiN HEMT shows at 1 GHz higher input impedance already at a drain bias of 0.1 V, and a much smaller variation of the input impedance when increasing V_{DS} up to 0.3 V. The input impedance lowering with increasing drain bias has been modeled in [16,17] using the R_{gs} and R_{gd} resistors in parallel to the C_{gs} and C_{gd} intrinsic capacitances, respectively. At V_{DS} = 0.3 V, the CVD-SiN device exhibits R_{gs} and R_{gd} values of 55 kΩ and 20 kΩ, respectively. This reveals a much better electrical isolation than for the RS-SiN based device, which demonstrates corresponding R_{gs} and R_{gd} values of 4.3 kΩ and 1.8 kΩ, respectively (see Table 1). The small-signal model is extracted for both devices from the S-parameter measurements using a direct extraction method [18,19]. The extracted small-signal parameters are summarized in Table 1.

The CVD-SiN device exhibits 50% larger pad capacitances C_{pg} and C_{pd} and a 78% larger gate–drain capacitance C_{gd} in comparison to the RS-SiN one. This might be due to the use of a thicker SiN-film which implies the drawback of a larger horizontal capacitance in the probing pads area. This also explains the reduced difference in S_{11} at high frequency observed in Fig. 7 between the two types of devices. However, considering the results of the RF measurements depicted in Fig. 8 and Fig. 9, it appears that the CVD-SiN HEMT demonstrates an overall better RF behavior. In Fig. 8, the current gain $|h_{21}|^2$ and the Mason's gain U are plotted versus frequency after de-embedding the parasitic pad capacitances at a drain bias of 0.2 V. The values of cut-off frequency f_T and maximum oscillation frequency f_{max} are extracted from $|h_{21}|^2$ and U, respectively, using a −20 dB/decade slope. Compared to the RS-SiN device, the CVD-SiN transistor exhibits a 22% higher value of f_T (140 GHz instead of 115 GHz) and a 25% higher value of f_{max}

(100 GHz instead of 80 GHz). In Fig. 9, the extrapolated values of f_T and f_{max}, as well as the maximum stable gain *MSG* at 40 GHz, are plotted versus the DC power consumption for V_{DS} of 0.1 V, 0.2 V and 0.3 V. The two types of devices demonstrate quite similar evolutions in terms of f_T, f_{max} and *MSG*. Nevertheless, the CVD-SiN device shows higher performance than the RS-SiN based InAs/AlSb HEMT in the whole range of the dissipated power.

For the low-noise measurements, a drain bias of 0.2 V was selected since the impact ionization phenomenon, occurring at higher V_{DS} values, is detrimental to noise performance [20]. The measured noise figure at 50 Ω, $NF_{50\Omega}$, is shown in Fig. 10 (a) in the frequency range 6 GHz to 18 GHz and for V_{DS} = 0.2 V. By combining the $NF_{50\Omega}$ measurements with the small-signal model, a noise model for each device has been obtained using the Pospieszalski method [21]. At V_{DS} = 0.2 V and 12 GHz, the modeled $NF_{50\Omega}$ for the RS-SiN device is 4 dB whereas the CVD-SiN device shows, at the same drain bias and frequency, a reduced $NF_{50\Omega}$ of 2.8 dB. In Fig. 10 (b) the minimum noise figure NF_{min}, obtained by fitting the measured $NF_{50\Omega}$, is plotted between 6 GHz and 18 GHz. The NF_{min} values at V_{DS} = 0.2 V are in the 2.3–2.8 dB and 1.4–2 dB ranges for the RS-SiN and CVD-SiN devices, respectively.

The improved RF performance measured on InAs/AlSb HEMTs with early-protection by a thicker SiN-film demonstrated that the consequent drawback of larger horizontal capacitances is overcome by the provided better DC behavior. The enhanced f_T and f_{max} values are ascribed to the better electrical isolation under the extrinsic gate, which leads to higher I_{on}/I_{off} ratio, reduced output conductance and lower gate current leakage. This direct benefit of a thicker film, enabled by the use of CVD method, is related to the evolution of S_{11} as well. With the 25 nm CVD-SiN film, the dominant mechanism for the input impedance lowering is mainly ascribed to the gate leakage current between gate and channel in the active region, where I_G results from a Schottky and an impact ionization component. With a 2 nm RS-SiN film, the input impedance lowering is partly related to these two components of I_G, but the main contribution is due to the leakage around the device mesa, through the AlGaSb layer. The lower total gate current, the better pinch-off behavior and the lower g_{DS} of the CVD-SiN device also explain the up to 40% improvement in $NF_{50\Omega}$ and NF_{min}. As a result, InAs/AlSb HEMTs based on the CVD-SiN method have been tested in a hybrid low-noise amplifier (LNA) [22], showing the suitability of the *in situ* early-protection for cryogenic applications.

5. Conclusion

The physical stability and the electrical behavior of shallow-mesa InAs/AlSb HEMTs based on a SiN-film early-protection deposited either *in situ* by CVD or *ex situ* by reactive sputtering have been studied. The *in situ* CVD method avoids any exposure to ambient of the AlGaSb mesa floor before its protection. In addition, it allows using a thicker SiN-film without issues during the subsequent critical lift-off procedure. InAs/AlSb HEMTs having a 25 nm *in situ* CVD SiN-film and devices based on the *ex situ* RS process with a 2 nm thin SiN-film have been compared. The *in situ* CVD-based transistors demonstrated enhanced stability against oxidation over the time. Moreover, improved DC behavior in terms of gate leakage current (up to one order of magnitude) and current pinch-off was observed. The *in situ* CVD InAs/AlSb HEMTs also exhibited, at V_{DS} = 0.3 V, increased values of f_T and f_{max} of 175 GHz (+20%) and 130 GHz (+18%), respectively. Furthermore, a noise model for the two HEMT technologies was extracted, showing a reduction of NF_{min} from 2.3 dB to 1.4 dB at 6 GHz when using the *in situ* CVD SiN film protection.

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