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Power Cycling Test Circuit for Thermal Fatigue Resistance Analysis of Solder Joints in IGBT

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Abstract : The paper will give a detailed presentation of an active power cycling test bench in high temperature conditions developed to ageing the solder between the Direct Copper Bonding (DCB) and the base of IGBT devices. The average junction temperature measurement protocol, the temperature regulation of the base plate, the acquisition of all the electrical signals, and the performance of the test circuit will be presented and discussed. Moreover, a thermal modelling presentation has been used to define the power cycling test parameters. The paper will present results of long time power cycling tests in server working conditions in the case of a base plate temperature equal to 90 °C, for a power injection of 300 W/cm² during 10 s.

1. Introduction

The reliability of power IGBT modules related to thermal fatigue have been investigated since more than 10 years and many papers have been published in this topic. Concerning experimental aspects, several works may be mentioned in a non-exhaustive list [1, 2, 3, 4]. Theoretical papers based on numerical simulations with experimental verifications have been published as well [5, 6, 7]. Consequently, the technology of these electronic devices has been significantly improved these last years against thermal fatigue. Nevertheless, the high power integration needed for example in hybrid vehicle applications (several hundreds W/cm²) and the high level of ambient temperature (until 120°C), make the power modules subjected to high power cycling constraints. One of the remaining and most frequently observed failure mode, due to thermal fatigue, is the solder cracks between the copper base plate and the Direct Copper Bonding (DCB) substrate. This make the thermo-mechanical behavior analysis necessary to understand the failures mechanisms of the power electronic packages and to assess the device lifetime related to power cycling. So, in order to validate an ageing model of the solder layer due to thermal fatigue, a lot of experimental results, in several experimental conditions are needed. The temperature level and temperature variations of the silicon chips are of the main factors that accelerate the package ageing. The paper will present the first test workbench of a particular cycling test circuit developed at the SATIE⁽¹⁾ laboratory and the first results obtained from reliability tests. Then, some preliminary thermal simulations, based on Finite Element Method, are presented in order to confirm the experimental results. Finally, the paper will discuss on the alteration we have to make in order to improve this power cycling test bench.

2 Power cycling test circuit

2.1 Principle

The tested devices are mounted on a massive duraluminium plate which acts as a large thermal capacitance and allows to keep the base plate of the devices at a constant temperature due to a thermal regulation whatever the power losses in the device under test (DUT) during all the test (Cf. **Fig. 1**). Two IGBT devices are simultaneously tested on the power cycling bench by an alternate power injection. The device ageing is monitored by a computer associated with an acquisition card which carries out the physical measurements necessary to this study. The main measured parameter is the thermal resistance between junction and case of the DUT which is the most pertinent ageing indicator test in the case of solders degradations.

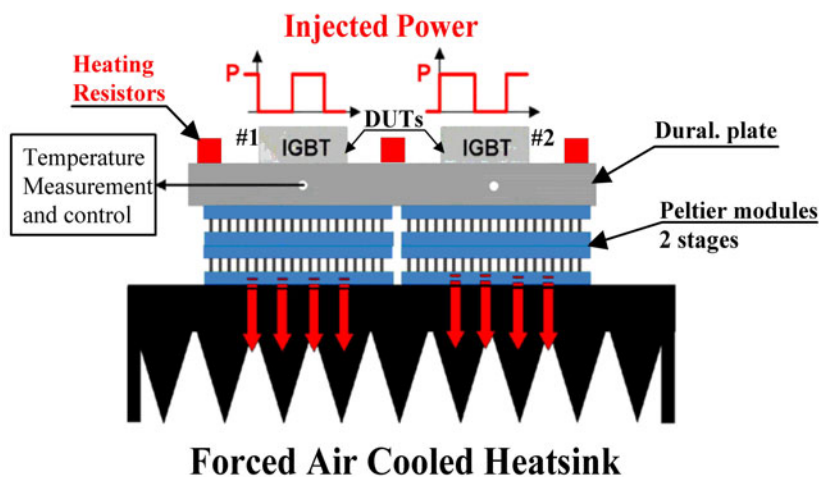


Fig. 1 : Temperature control of the base plate.

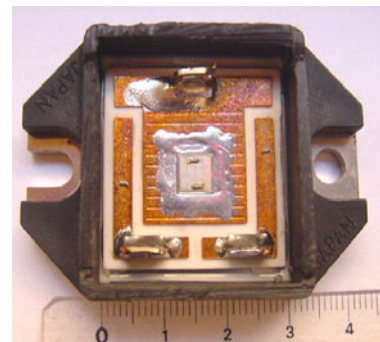


Fig. 2 : IGBT MG25J1BS11
(600 V – 25 A).

The duraluminium plate temperature can be controlled between 30 and 100 °C (representative of automotive applications) by means of :

- 8 heating resistors which ensure the compensation of the heat losses by free thermal convection during a high temperature operation.
- 16 Peltier modules (MELCOR / HT6-12-40) which ensure the evacuation of the excess heat through a forced air heat sink (especially at low case temperature).

The datasheet of the Peltier modules specifies a maximum difference of 63 °C between the hot and cold faces. Their assembly mode (serial connected like shown in **Fig. 1**) makes possible to reduce the temperature difference between the cold and hot faces of the Peltier modules in order to ensure an operation below this limit. As the duraluminium plate temperature is controlled during the power cycling tests, the difference in temperature between cold and hot faces of the Peltier modules remains constant, so they are not submitted to power cycling constraints, and their reliability is not altered by the power injection in the IGBTs. To date, these devices had worked during more than 2000 hours without failure.

The plate temperature control is characterized by a temperature oscillation less than ± 3 °C. The temperature measurements are carried out by a thermistor (HONEYWELL / HEL-705), with an analogical amplification towards the acquisition card.

The tested devices are low power IGBT modules (Toshiba 600V-25A / MG25J1BS11) (Cf. **Fig. 2**). The simultaneous test of the two components imposes a synchronization of various actions : power injection, plate temperature control, physical measurements and ON/OFF power cycle durations. This function is fulfilled by a conditioning device of the signals which leads to an action chronogram as presented below for a single device (Cf. **Fig. 3**)

The thermal cycling of the DUTs is obtained by a periodic power injection in each devices during a cycling period defined by the user. The power cycling parameters are chosen in order to focused on the thermal fatigue of the solder between the base plate and the ceramic substrate. So, the power is injected through the DUTs, which are working in their linear zone, with a low injected current (2 A). This low injection current and the high enough power cycle duration avoid failures attached to the wire bonds ageing. The dissipated power is defined by the voltage supply level (U_{DC}) applied to the devices between emitter and collector terminals. In our tests, the voltage supply levels used are $U_{DC} = 37.5$ V and $U_{DC} = 45.0$ V corresponding to dissipated powers of 75 W and 90 W (Cf. **Fig. 3**).

Junction temperature (T_j) is estimated just after the power injection phase by the measurement of V_{CE-SAT} at a very low current injection level through the device in order to avoid self heating (Cf. **Fig. 3**). So to obtain the highest degree of accuracy, a characterization campaign has been carried out in order to determine the better calibration $T_j(V_{CE-SAT})$ by the current level. We have chosen a current level of 2 mA. This choice is conditioned both by the amplitude variation of V_{CE-SAT} for T_j between 50 and 180 °C and by the linear dependence of V_{CE-SAT} with T_j . Diodes D_1 and D_2 have been selected for their similar forward voltage drop. So, V_{CE-SAT} is estimated by simultaneous measurements of voltages V_{CE1} and V_{CE2} (Cf. **Fig. 3**). Before and during the indirect measurement of the junction temperature, transistor T_1 has to be turned on in order to impose the gate voltage of the DUT (15 V).

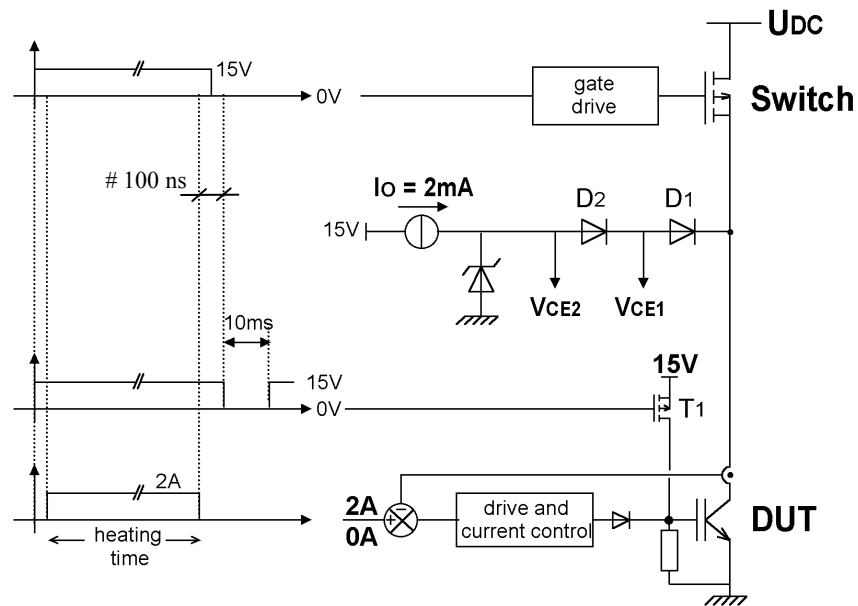


Fig. 3 : Chronogram of the power cycling test.

The plate temperature control by the Peltier modules generates a significant disturbance on the physical measures. So, an inhibition of the Peltier modules power supply is necessary and is carried out by the control program of the endurance bench. A delay time of 1 ms between the end of the power injection and the measurement acquisitions is necessary to switch-off the Peltier current (Cf. **Fig. 4**).

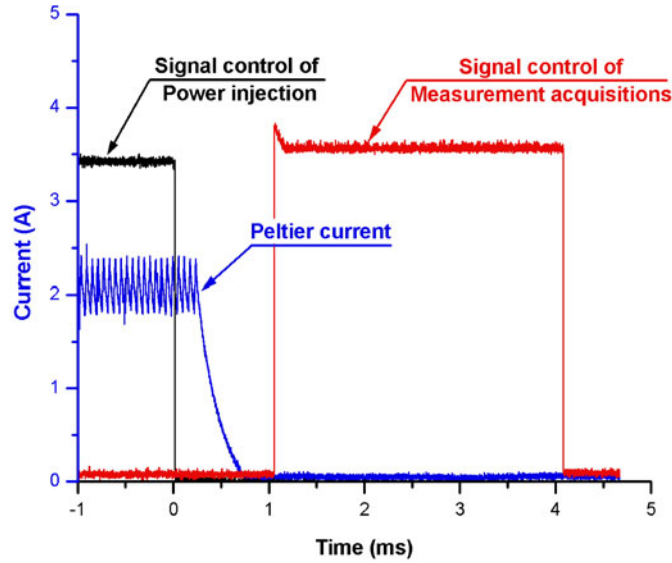


Fig. 4 : Data acquisition chronogram for the indirect temperature measurements.

In fact, the measurements don't report the device thermal state at the end of the power injection because of the 1 ms delay time. The solution is to estimate this values from measurements made after the cancellation of the current in the Peltier modules. These measurements consists of 30 successive acquisitions during 3 ms (Cf. Fig. 4). As illustration, Fig. 5 shows the decrease of the junction temperature after the 1 ms delay time during a sequence of 30 acquisitions.

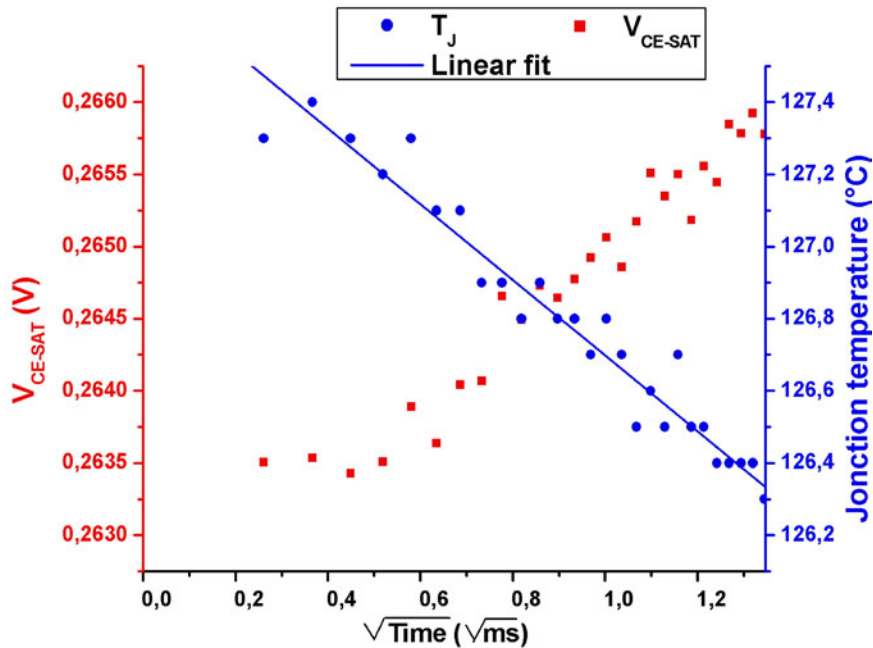


Fig. 5 : Estimation of the junction temperature to be left of the 30 measurements.

In a thermal modelling study with a constant heat flux, the temperature at a local point of the assembly decrease linearly with the square root of time [8] (Square root of time is indicated on the X-Axis on Fig. 5). Then, successive acquisitions carried out after the delay time make it possible to extrapolate the average junction temperature at the end of the power injection by linear interpolation according to the least squares method.

2. Thermal simulation of the tested devices

2.1. Model of the tested IGBT

The thermal model needs the knowledge of the various material layers dimensions and thermal properties of the module assembly. After a device was cut-off and polished, the thickness measurement is carried out by an optical microscope (Cf. **Fig. 6**). On the left of the cross section microscopy (Cf. **Fig. 6**) labels T1 to T8 are defined for each interface layer under the chip like shown in the temperature evolution graph (Cf. **Fig. 7(a)**).

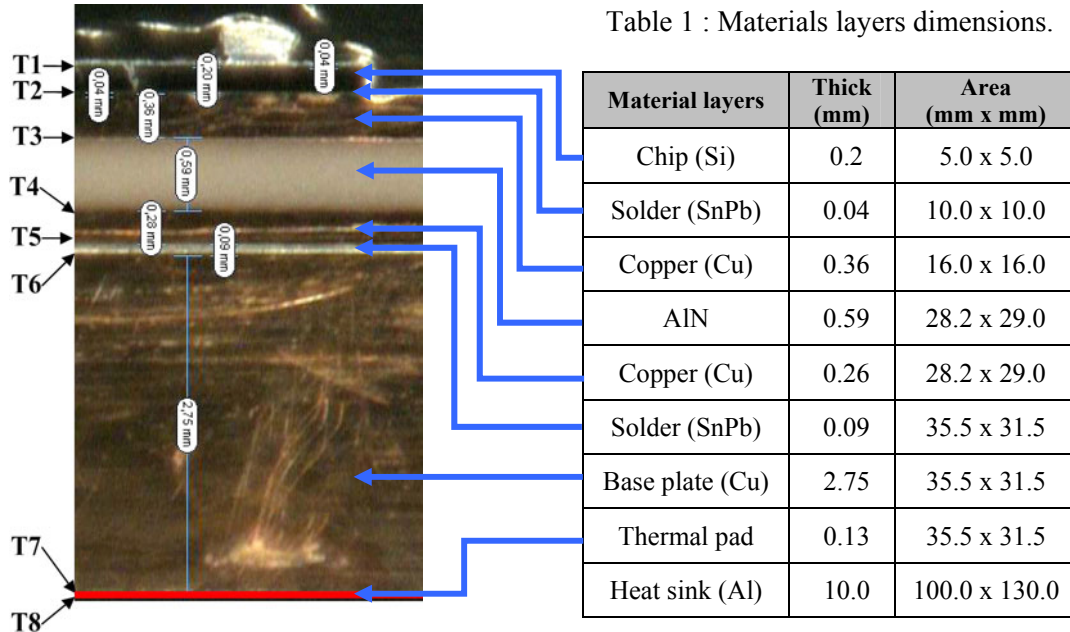


Fig. 6 : Material layers of the tested IGBT.

The purpose is to identify the thermal time-constant of the assembly in order to assess the minimal duration of power injection during accelerated cycling test. In addition, the simulation allows to estimate the temperature fields in the package, especially on the chip. Thermal simulation is carried out using a 3D simulation tool based on Finite Elements Method analysis ANSYS software [9]. The thermal properties of the IGBT material layers are presented in the table below.

Table 2 : Thermal properties of IGBT material layers.

Material	λ ($\text{W.m}^{-1}.\text{K}^{-1}$)	C_{th} ($\text{J.kg}^{-1}.\text{K}^{-1}$)	Density (kg.m^{-3})
Silicon	150	735	2330
Solder (SnPb)	50	150	8530
Copper	390	385	8960
Al_2O_3	30	795	3800
Thermal pad	1.6	-	-
Heat sink (Al)	129	920	2800

The presented results (**Fig. 7**) are obtained for a base plate temperature equal to 90 °C, an injected power of 75 W corresponding to 300 W/cm² heat flux applied on the chip active area.

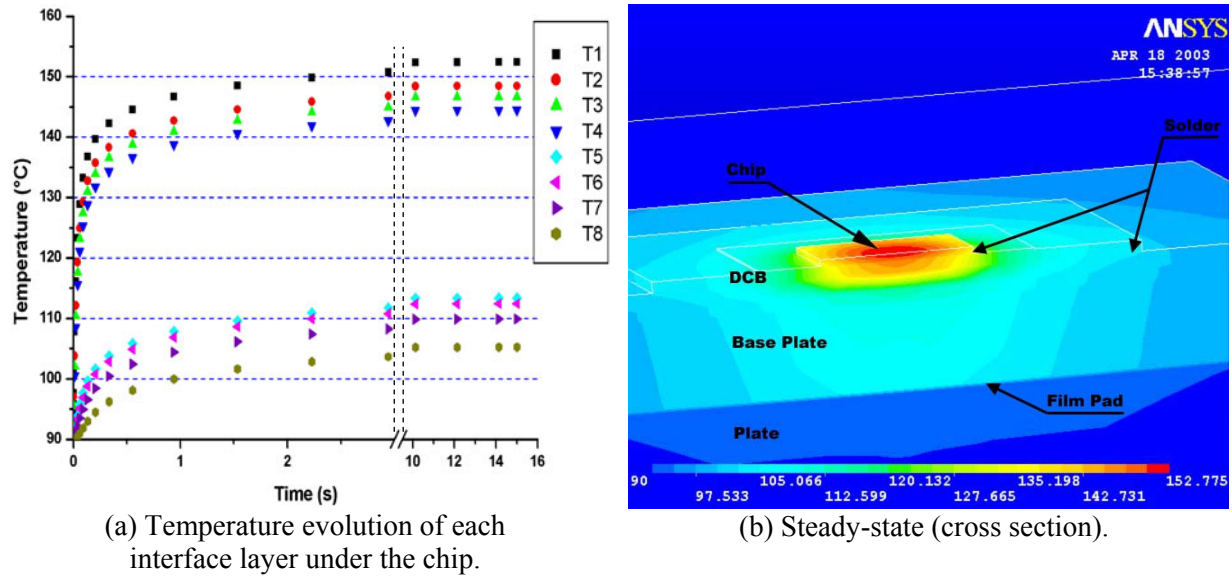


Fig. 7 : Temperature distribution in the simulated IGBT ($P = 300 \text{ W/cm}^2$ - Plate Temp. = 90°C).

It can be seen, in **Fig. 7(b)**, a low increase in temperature on the borders of the soldered joint between the base plate and the DCB. The simulation results give a value of 153 °C for the junction temperature which corresponds to the maximum value according to manufacturer datasheet. As shown in the **Fig. 7(a)**, the thermal steady-state of the system is attained in a time lower than 10 s. This duration condition is the minimal value required to get the steady-state conditions.

3. Experimental results

The first experimental results obtained after 220,000 cycles of 75 W (300 W/cm²) power injection is shown in **Fig. 8**, for a plate temperature of 90 °C and 10 s for each heating and cooling phase. The junction and plate temperatures are given in this figure as well as the junction to plate thermal resistance, during the ageing. The junction temperature estimated after each power injection cycle is close to the calculated value (Cf. **Fig. 7**).

Unfortunately, **Fig. 8** shows that there is no significant variation of the thermal resistance between the junction and the plate. It let's suppose the absence of solder delamination between the base plate and the DCB. The similitude of solder acoustic scans between the base plate and the DCB before and after the 220,000 thermal cycles applied to the IGBT shown on **Fig. 9** confirms this assumption. This result is induced by the large difference of the chip area compared to the DCB area. The low increase in temperature on the border of the solder between the ceramic layer and the base plate limits its ageing during the power cycling tests [5].

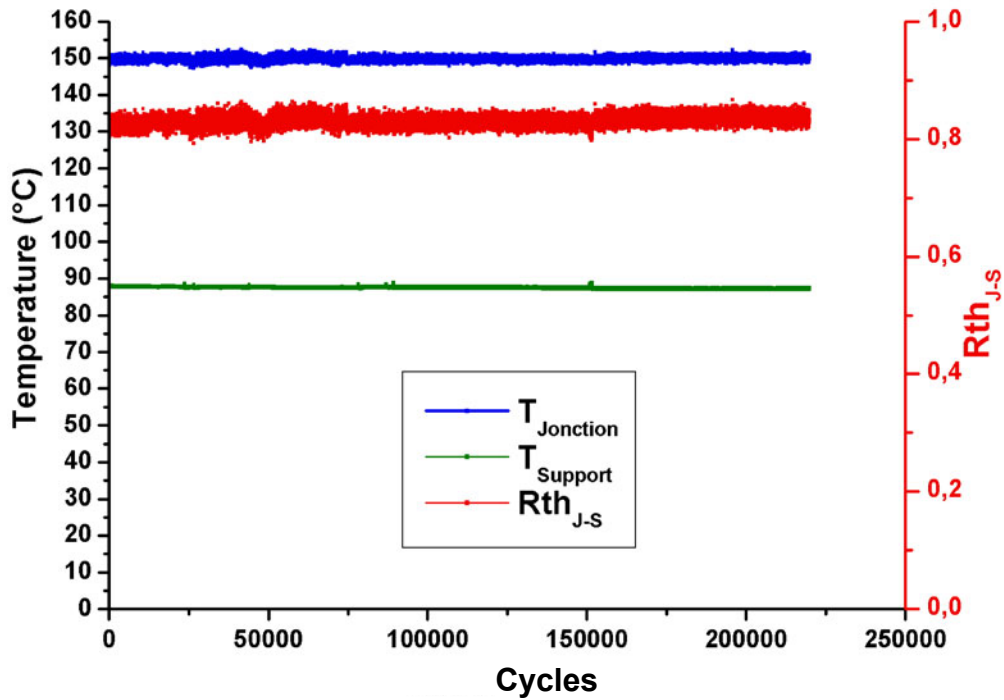


Fig. 8 : Long term power cycling results
 ($P = 75 \text{ W}$ (300 W/cm^2), Heating time = 10 s, Cooling time = 10 s, $T_{\text{Sup.}} = 90 \text{ }^\circ\text{C}$).

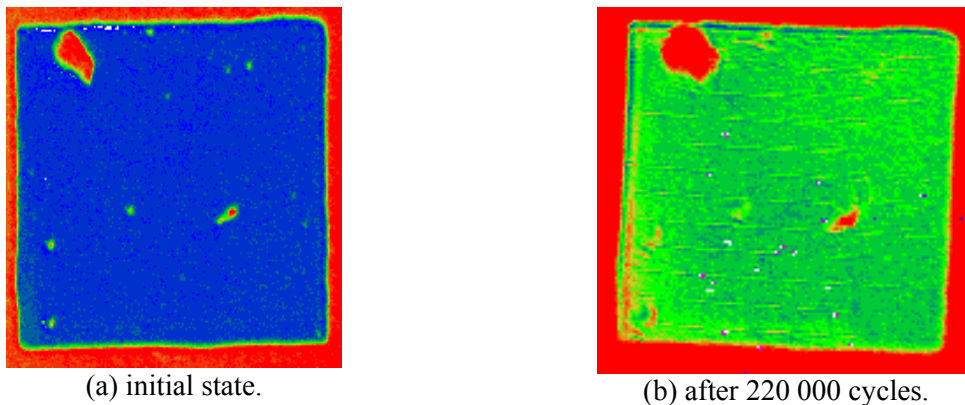


Fig. 9 : Acoustic scans of the solder layer between base plate and DCB.

Nevertheless, one observes on **Fig. 9(b)** an increase of the solder voids size, located at the edge of the DCB. But it influences very lightly the heat flux. Moreover, the flat evolution of the thermal resistance during the ageing shows that the solder area located under the chip does not seem deteriorate in spite of the $60 \text{ }^\circ\text{C}$ of temperature variation (ΔT) during power cycling.

4. Conclusion

The paper presents the first ageing results obtained on a power cycling test circuit which base plate temperature is controlled between 30 °C and 100 °C. The study is focused on the solder layers degradations. So, the power injection occurs with a low current in order to avoid failures attached to the wire bonds ageing. According to the injected power in the IGBTs the base plate temperature is controlled by Peltier modules (cooling) and heating resistors (heating) independently of the injected power loosed in the IGBTs.

The thermal resistance is the main ageing indicator in the case of solder layer degradations. Thermal resistance is estimated after each power cycle by indirect measurement of the “average” junction temperature. Unfortunately, the ceramic layer area is too large compared to the chip area of the low power IGBT used for the test of the power cycle bench. So, in these circumstances, the injected power does not allow to significantly increase the temperature on the edge of the solder layer between the ceramic and the base plate. So, there was no significant degradation of the solder layer after 220,000 power cycles in the case of a base plate temperature equal to 90 °C and an injected power flux equal to 300 W/cm². In spite of the ageing results lack, the power cycle tests have shown the good working of the power cycling test bench during several months. Moreover, this development had allowed the adjustment of the bench test control and the acquisition measurement solution to obtain a specific tool for the solder ageing test of electronic power devices.

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