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Influence of IGBT Current Rating on the Thermal Cycling Lifetime of a Power Electronic Active Rectifier in a Direct Wave Energy Converter

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***Abstract* - Direct Wave Energy Converters offer high reliability potential, which is a key factor in offshore environments, yet their electrical power produced is strongly pulsating. The thermal cycling of their power electronic switches (considered here to be Insulated Gate Bipolar Transistors, IGBT) may reduce the lifetime of the power electronic converter. This study proposes a generic design method for choosing both the IGBT current rating and the heatsink thermal resistance in order to satisfy a reliability constraint. A parametric electro-thermal model has thus been developed to determine the junction temperature time series. Moreover, a rainflow cycle counting method is introduced for the reliability analysis and lifetime prediction using two aging models, one for wire bonds, the other for the solder joint of the chip.**

***Keywords* - Ageing, Power cycling, IGBT, Design, AC machine, Wave energy.**

1. Introduction

Reliability in Wave Energy Converters (WEC) constitutes a key issue for two main reasons. First of all, maintenance operations are restricted due to few weather window opportunities in energetically attractive sites [1]. Secondly mechanical and electrical power fluctuations are strong and frequent during wave energy conversion, a phenomenon that tends to reduce the equipment lifetime; this become especially true in a Direct Wave Energy Converter (DWEC), for which wave power fluctuations lead directly to fluctuations in the electrical power produced and junction temperature within power electronics modules. According to studies [2–4], the power semiconductors and DC bus capacitors are both weak points in the converter.

A power electronic converter must offer a trade-off between cost, size, reliability and performance over the entire operating lifetime (considered to be 20 years in this case). Reliability studies on Insulated-Gate Bipolar Transistor (IGBT) converters have been conducted under other conditions with strong power fluctuations, involving namely: wind power systems [5], STATCOM [6] and railway traction [7]. In a DWEC, the speed of the electrical Power Take-Off (PTO) is canceled twice in a single wave period, hence the fluctuations are even more frequent. To the best of our knowledge, no study has yet been undertaken on converter ageing in a DWEC. In addition, most recent aging models [8] have provided statistical information and taken into account the various failure modes.

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A model is developed herein that relates the rated current with loss and thermal parameters in the case of a constant IGBT voltage rating (in this application, the DC bus voltage has been fixed). This model serves to evaluate the influence of IGBT rating over the IGBT lifetime according to this application. The goal of this paper is to optimize the rating of power electronic converters; the model derived is part of a more global modeling approach covering the entire WEC, as shown in Fig. 1.

In our case, the studied DWEC is the SEAREV [9-10], which consists of a completely enclosed floating buoy with an embedded pendular wheel. Excitation forces from the swell on the buoy generate a relative motion between the float and the wheel; this oscillating motion is then damped in order to produce energy (see Fig.1). Damping is controlled by a three-phase Permanent Magnet Synchronous Generator (PMSG) connected to a back-to-back converter. The PMSG is a surface permanent magnet low-speed high-torque machine with 124 pole pairs; its design has been optimized to minimize the per-kWh production cost [10]. The back-to-back converter is composed of: a Pulse Width Modulation (PWM) inverter connected to the PMSG, for controlling damping; a PWM-inverter connected to the grid, for regulating the DC bus voltage and supplying the grid with power; and a chopper connected to supercapacitors, for smoothing electrical power output so as to achieve better grid compliance [11].

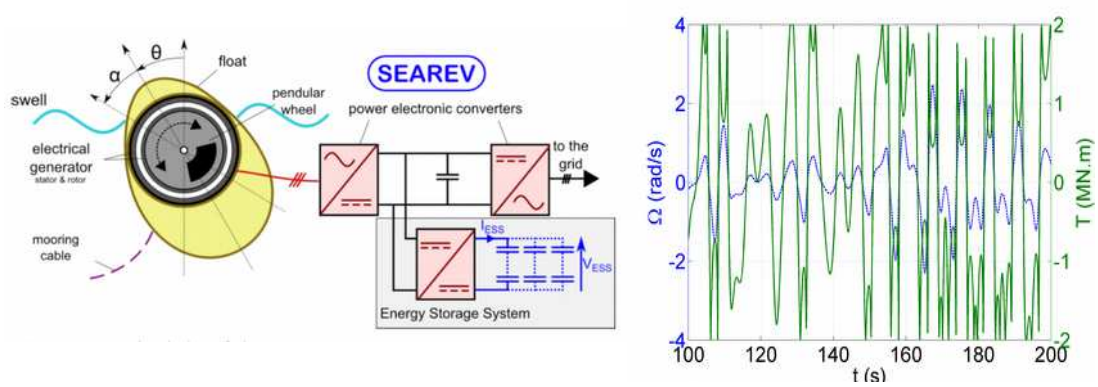


Fig. 1: Principle scheme of the SEAREV Direct Wave Energy Converter and example of Torque and Speed waveforms in the case of sea-state: H_s = 6 m; T_p = 10 s.

2. From a sea elevation profile to junction temperature waveforms

2.1. Computation of current waveforms in power electronics

A multiphysics model is used to compute current waveforms in the power electronic components from a sea elevation profile. The hydro-mechanical part of the model (developed in [9]) computes both speed and torque at the PMSG shaft based on the sea elevation profile and a damping law. The preferred damping strategy consists of applying a braking torque proportional to the rotational speed (viscous damping parameter: 4 Mnm/(rad.s^{-1})) with a power leveling (to avoid excessive power peaks in the electrical chain: P_{lev} = 1.1 MW). The electrical model (presented in [10]) yields voltages and currents in the machine based on torque-speed profiles. The current in the *q*-axis is chosen to provide the required torque (*d*-axis current exerts no influence on torque given that the generator is a non-salient machine), while current in the *d*-axis is set to minimize total power losses when taking iron and copper losses into account as well as power electronic losses. AC currents are calculated as averages over the modulation period, in order to determine the currents in each semiconductor. The computed time series last 900 s with a time step of 1 ms.

2.2. Power electronic loss computation

Conduction losses in IGBTs and freewheeling diodes are calculated by means of a piecewise linear model (with threshold voltage and dynamic resistance):

$$P_{cond\ IGBT} = \left(V_{0\,IGBT} + r_{d\,IGBT}\, I_c\right) I_c\, d_{IGBT} \quad (1)$$

$$P_{cond\ Diode} = \left(V_{0\,Diode} + r_{d\,Diode}\, I_f\right) I_f\, d_{Diode} \quad (2)$$

where $P_{cond\ IGBT}$ and $P_{cond\ Diode}$ are respectively the transistor and diode conduction losses, V_{0IGBT} and V_{0Diode} respectively the transistor and diode threshold voltages, r_{dIGBT} and r_{dDiode} respectively the transistor and diode dynamic resistances, d_{IGBT} and d_{Diode} respectively the transistor and diode duty cycles, I_c the collector current during transistor conduction and I_f the forward current during diode conduction.

Switching losses, on the other hand, are calculated from the turn-on and turn-off energy for the IGBT and from the reverse recovery energy for the diode in a reference case [12].

$$P_{sw\,IGBT}(I_c, V_{DC}) = f_d\, E_{IGBT\,ref} \left(\frac{I_c}{I_{rated}}\right)^{1,1} \left(\frac{V_{DC}}{V_{DC\,ref}}\right)^{1,35} \tag{3}$$

$$P_{sw\,Diode}(I_f, V_{DC}) = f_d\, E_{Diode\,ref} \left(\frac{I_f}{I_{rated}}\right)^{0,6} \left(\frac{V_{DC}}{V_{DC\,ref}}\right)^{0,6} \tag{4}$$

where $P_{sw\ IGBT}$ and $P_{sw\ Diode}$ are respectively the transistor and diode switching losses, f_d the PWM frequency, V_{DC} the DC bus voltage, $E_{IGBT\ ref}$ and $E_{diode\ ref}$ respectively the transistor and diode total switching energies with a current I_{rated} and DC bus voltage $V_{DC\,ref}$.

2.3. Transient thermal model

Foster's network model is used to build the junction-case thermal model (Fig. 2) [13]; this model provides a very simple form for thermal impedance and has been used in many thermal studies of semiconductors [5-6]; moreover, it depends on the rated current of IGBTs and diodes.

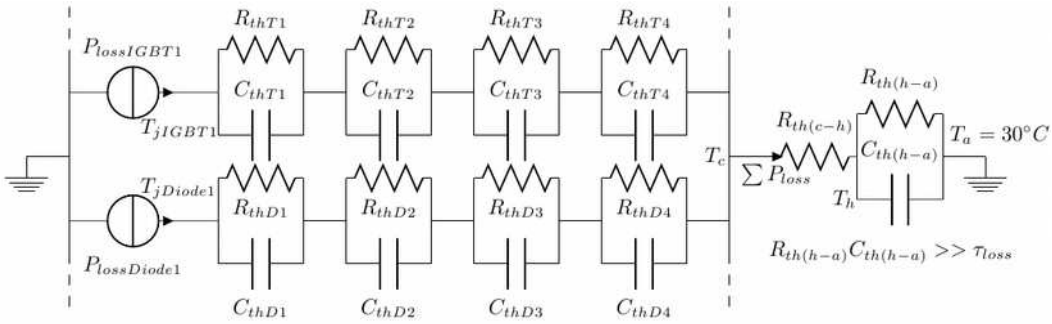


Fig. 2: Transient thermal model and hypotheses (only one of the six IGBT-diode module represented)

Thermal impulse response as a function of pulse duration can be approximated by the product of a thermal resistance $R_{th(j\text{-}c)X}$ and a normalized impedance, as follows:

$$Z_{th(j-c)IGBT}(t) = R_{th(j-c)IGBT} \sum_{i=1}^{4} r_{i\,IGBT}\left(1 - e^{-t/\tau_{i\,IGBT}}\right) \tag{5}$$

$$Z_{th(j-c)Diode}(t) = R_{th(j-c)Diode} \sum_{i=1}^{4} r_{i\,Diode}\left(1 - e^{-t/\tau_{i\,Diode}}\right) \tag{6}$$

It is reasonable to assume that the normalized impedance does not depend on the current rating, given that thermal resistances are inversely proportional to area while thermal capacitances are in fact proportional to area. The values of r_{iX} and τ_{iX} are listed in Table I.

Table I: Transient thermal model parameters

i	1	2	3	4
r_{iIGBT}	71 %	18 %	7 %	4 %
τ_{iIGBT}	200 ms	20 ms	2 ms	0.52 ms
r_{iDiode}	70 %	16 %	7 %	7 %
τ_{iDiode}	210 ms	30 ms	7 ms	1.5 ms

The six basic power modules (containing one IGBT and one diode) necessary for an inverter have been mounted onto a single heatsink using a thermal compound to improve thermal contact. It is assumed herein that this thermal interface layer has very little and, in reality negligible, thermal inertia. The thermal inertia of this heatsink is assumed to be high enough to neglect any significant variations in heatsink temperature (with the typical thermal time constant for an air-forced heatsink being around 250 s). In this initial study, we have assumed that the heatsink temperature equals a constant for a sea-state (the typical duration of a sea-state is 1 hour) and moreover only depends on the ambient temperature (30 °C) and average losses in semiconductor components: the thermal resistance heatsink-ambient equals $R_{th\ (h\text{-}a)}$ = 7 K/kW at the beginning of this study. Hereafter, the size of the heatsink, like other system components, will be considered as a design parameter.

2.4. Reference components and reference parameters

The DC bus voltage is set at 1300 V and the switching frequency at 2 kHz. The model parameters are based on an extrapolation of the characteristics of four components of the ABB HiPak 1700 V Soft-Punch-Through technology [14].

Threshold voltages, dynamic resistances and switching energies are all determined from datasheet-based interpolations for a current between 0.5 and 1.2 times the rated current (i.e. the range of formulae validity). Thermal resistance and capacitance values are also based on datasheets. In Fig. 3, the threshold voltage V_{0X}, the voltage drop across the dynamic resistances (when current equals the rating $r_{dX} I_{rated}$) and the relative switching energy of the IGBT and diode are all plotted as a function of the rated current. The points on the graph correspond to retrieved data, while the curves correspond to application of a scaling law.

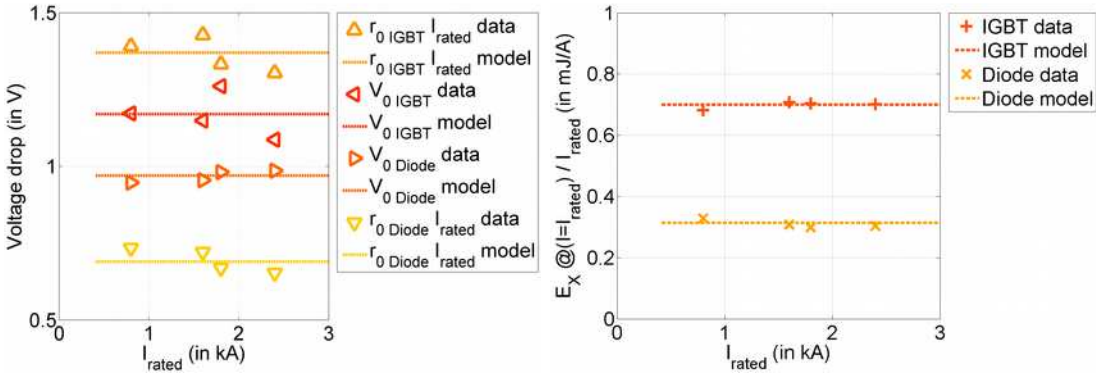


Fig. 3: Voltage drop parameters and relative switching energies vs. rated current (at the junction temperature: 125°C, DC voltage: 900 V)

These four components are produced by the parallelization of 100 A chips. The scaling laws clearly reflect this parallel connection of single chips, with a proportional relationship between chip area and current rating. The values used are summarized in Table II.

Table II: Loss and thermal model parameters as a function of current rating

X	V_{0X}	$r_{dX} I_{rated}$	$E_X(I_{rated}, 900\ V) / I_{rated}$	$R_{th(j\text{-}c)X} I_{rated}$	$R_{th(c\text{-}h)} I_{rated}$
IGBT	1.17 V	1.37 V	0.695 mJ/A	16.7 A.(K/W)	2.12 A.(K/W)
Diode	0.97 V	0.69 V	0.314 mJ/A	29.4 A.(K/W)	

2.5. Junction temperatures

In applying the electro-thermal model presented above, the junction temperature waveforms for the six IGBT and six diodes of an inverter can be computed for various wave elevation profiles, with different current ratings and different heatsink thermal resistances. These junction temperatures are then used for the lifetime prediction derived from thermal cycling models.

3. Reliability model

3.1. Thermal cycling aging models

The models presented in this paper are more comprehensive [8] compared to the conventional models used in other studies [5,6,7]. They have been built with a cyclic pattern of thermal junction temperature. This model's primary assumption is that an aging cycle with a different shape yet the same amplitude, same maximum (or minimum) temperature and same duration causes the same level of damage. Two failure modes are explored in this study:

- The first corresponds to the aging of wire bonding. $N_{10\%wb}$ is the number of cycles when the probability of wire bonding failure reaches 10 %; in this instance, it depends on the junction temperature cycle amplitude and maximum junction temperature during the cycle.
- The second mode corresponds to the aging of chip solder joints: for this mode, $N_{10\%sj}$ represents the number of cycles when the probability of chip solder joint failure reaches 10 %; it depends on the junction temperature cycle amplitude, minimum junction temperature during the cycle, and cycle duration.

The wire bonding fatigue model is a Coffin-Manson model that takes non-destructive elastic deformations into account [15]:

$$N_{10\%wb} = \begin{cases} 8.56e8\left(\Delta T_j - \Delta T_{j\,cut-off}\right)^{-2} & \text{if } \Delta T_j > \Delta T_{j\,cut-off} \\ +\infty & \text{if } \Delta T_j \leq \Delta T_{j\,cut-off} \end{cases} \quad (7)$$

$$\Delta T_{j\,cut-off} = 148 - 0{,}308\, T_{j\,max} \quad (8)$$

where ΔT_j denotes the junction temperature cycle amplitude (in Kelvin), and $T_{j\,max}$ the maximum junction temperature during the cycles (Kelvin).

The model for chip solder joint fatigue has been fitted on the basis of 92 $N_{10\%sj}$ cycle numbers given for various conditions[8] (with cycle periods between 1 second and 1 day; minimum cycle temperature between -20°C and 120°C; temperature amplitudes between 30°C and 120°C):

$$N_{10\%sj} = 3.33e141 \times t_{cycle}^{-1.93} T_{j\,min}^{-42.2} \Delta T_j^{-15.4} + 1.31e23 \times t_{cycle}^{-0.207} T_{j\,min}^{-4.52} \Delta T_j^{-3.29} \quad (9)$$

where t_{cycle} is the cycle duration in seconds, ΔT_j the junction temperature amplitude of the cycles (Kelvin), and $T_{j\,min}$ the minimum junction temperature during the cycles (Kelvin).

3.2. Rainflow cycle counting algorithm

Originally used to study mechanical fatigue, the rainflow-counting algorithm transforms time series into various cycles in order to apply cycling aging models in the case of complex loadings [16]. This algorithm has been described in detail in the relevant standard [17], and a MATLAB implementation is given in [18]; it is used herein to determine, from a junction temperature time series, the cycles and half-cycles along with their maximum junction temperature, amplitude and duration. The damage corresponding to each cycle and half-cycle can then be summed, according to Miner's rule [19]. It has been shown that the rainflow algorithm, in association with Miner's cumulative damage rule (as opposed to other counting algorithms), more closely approximates the result of a multiphysics finite element model as regards the cycling fatigue of power semiconductor devices [20].

A sea-state can be described using two parameters: the significant wave height H_s and the peak wave period T_p. The time $t_{10\%X}(H_s,T_p)$ corresponds to the time when failure probability reaches 10% for a given sea-state (H_s,T_p) and can therefore be computed for both models:

$$t_{10\%X}(H_s, T_p) = t_{simu} \sum_{i=1}^{N_{hc}} \frac{1}{2\, N_{10\%\,X\,i}} \quad (10)$$

where t_{simu} is the simulation duration (here 900 s), N_{hc} the number of equivalent half-cycles during the simulation and $N_{10\%X\,i}$ the 10 % lifetime corresponding to the i^{th} half-cycle.

In the simulation corresponding to each sea-state encountered, the weighted average of $t_{10\%X}(H_s,T_p)$ leads to the following lifetime result:

$$\frac{1}{t_{10\%X}}=\sum_{i=1}^{N_{EM}}\frac{p_i}{t_{10\%X}(H_{si},T_{si})} \tag{11}$$

where p_i is the probability of occurrence of the i^{th} sea-state, which features a significant wave height $H_{s\,i}$ and peak wave period $T_{p\,i}$. The sea-state probabilities of occurrence for this study are correlated to with Francec's Yeu Island, located 20 km off of the country's western coast, near the city of Nantes. This sea-state occurrence appears in Fig. 4, with the average power production for each state. The term by term multiplication of these two information elements yields the sea-state energy contribution.

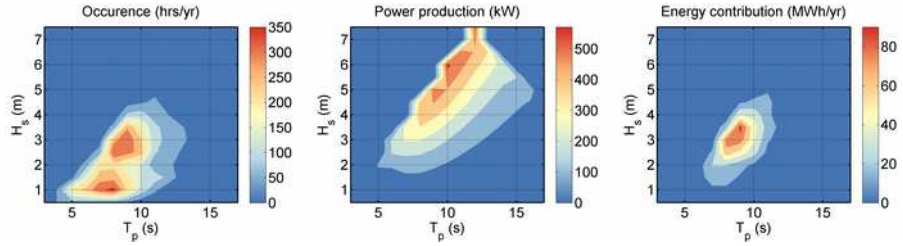


Fig. 4: Occurrence for Yeu island, SEAREV power matrix and average energy contribution for each sea-state

3.3. Failure probability distribution

The distribution of failures follows a Weibull distribution for both models, which in turn allows calculating failure probability as a function of time, i.e.:

$$F_X(t)=1-\exp\left(\ln(0.9)\left(\frac{t}{t_{10\%X}}\right)^{\beta_X}\right) \tag{12}$$

where F_X is the failure distribution function for either the wire bonding aging model (F_{bm}) or the solder joint aging model (F_{sj}). The shape parameter β_X characterizes the spread of this distribution. The greater the value of this parameter, the more heavily concentrated the time to failure around the median of the distribution. β_X equals respectively 3.6 for the wire bonding model and 6.6 for the chip solder joint model, both of which are relatively high shape parameter value.

The failure distribution for an entire module with an IGBT and diode is given by the following expression, in accordance with the combination formula:

$$F_{mod.}(t)=1-\left(1-F_{wb\,IGBT}(t)\right)\left(1-F_{sj\,IGBT}(t)\right)\left(1-F_{wb\,Diode}(t)\right)\left(1-F_{sj\,Diode}(t)\right) \tag{13}$$

We are considering here a 6-module inverter, though the failure probabilities of capacitors, the gate driver and other components have not been taken into account. If a module fails, then the whole inverter fails, just like 6 links in a chain. The formula for series systems can therefore be employed:

$$F_{Inv.}(t)=1-(1-F_{mod.}(t))^6 \tag{14}$$

where $F_{mod.}$ is the failure distribution for a single module and F_{inv} the failure distribution for the whole inverter.

4. Results

This study presents just the results for the active rectifier connected to the PMSG (Fig. 5), whose structure is also described in Fig. 5. The decision to focus on this rectifier stems from the fact that this particular converter is most adversely affected by speed and power fluctuations. An electrical storage system is used to smooth the power for better grid compliance, hence power fluctuations are reduced in the PWM inverter connected to the grid.

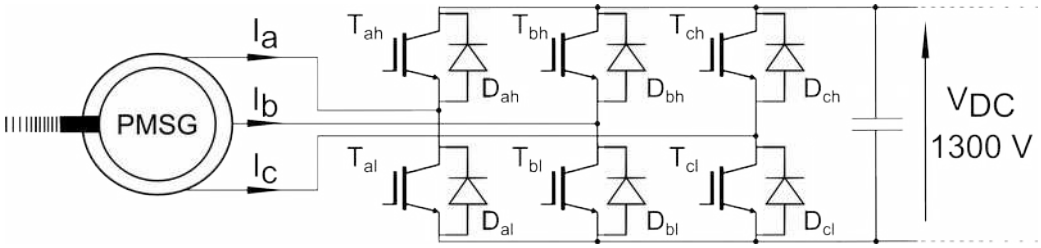


Fig. 5: Generator side power converter (PWM active rectifier)

Simplifying assumptions have been introduced, like using a Foster network thermal model and neglecting the loss dependence of temperature. As a result, the computation time with MATLAB to calculate aging for one sea-state is very low: 4.1 s (with an Intel-Xeon X5550 clocked at 2.67GHz).

4.1. Results for two different sea-states

A sea-state is described by its significant wave height H_s and peak wave period T_p; it provides important information on the power source, as wind speed for wind turbines. At the outset, 2 sea-states were used. The first, with H_s = 3 m and T_p = 9 s, is a typical state for DWEC design studies due to its high energy: it is frequent (340 hours a year) and powerful (average production: 250 kW). The second state, with H_s = 6 m and T_p = 10 s, is the more powerful (average production: 590 kW), hence in all likelihood the most critical in terms of reliability, though its occurrence remains rare (4 hours a year). The current waveform during one phase of the PMSG is shown in Fig. 6. The maximum current in this case equals 1400 A. Three time scales of fluctuations are apparent: wave groups (50-s period), waves (10-s period) corresponding to two speed cancellations, and electric pulsation (on the order of 50 ms).

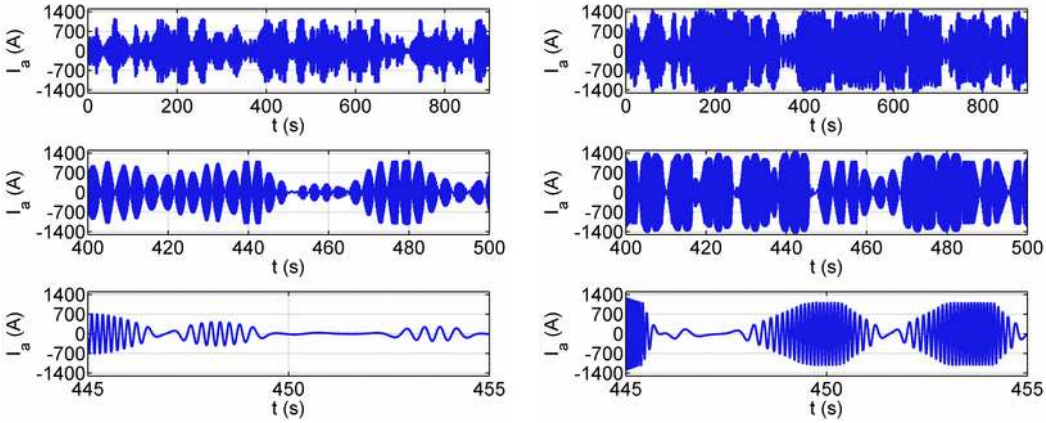


Fig. 6: Current waveforms in the first phase of the PMSG vs. time (3 time scales) in two sea-state examples: H_s = 3 m and T_p = 9 s for the left-hand figure (average production: 245 kW); and H_s = 6 m and T_p = 10 s for the right figure (average production: 590 kW)

For the first evaluation, the IGBT current rating has been set equal to the maximum current (1400 A). The heatsink thermal resistance has been chosen to reach a junction temperature of 125°C during the most powerful sea-state (i.e. $R_{th\ (h\text{-}a)}$ = 7 K/kW). The junction temperature of an IGBT and a diode vs. time is shown in Fig. 7. Since the converter is being used as an active rectifier, the diode junction temperature tends to exceed IGBT junction temperature. In an active rectifier, diodes actually conduct more often than the IGBT.

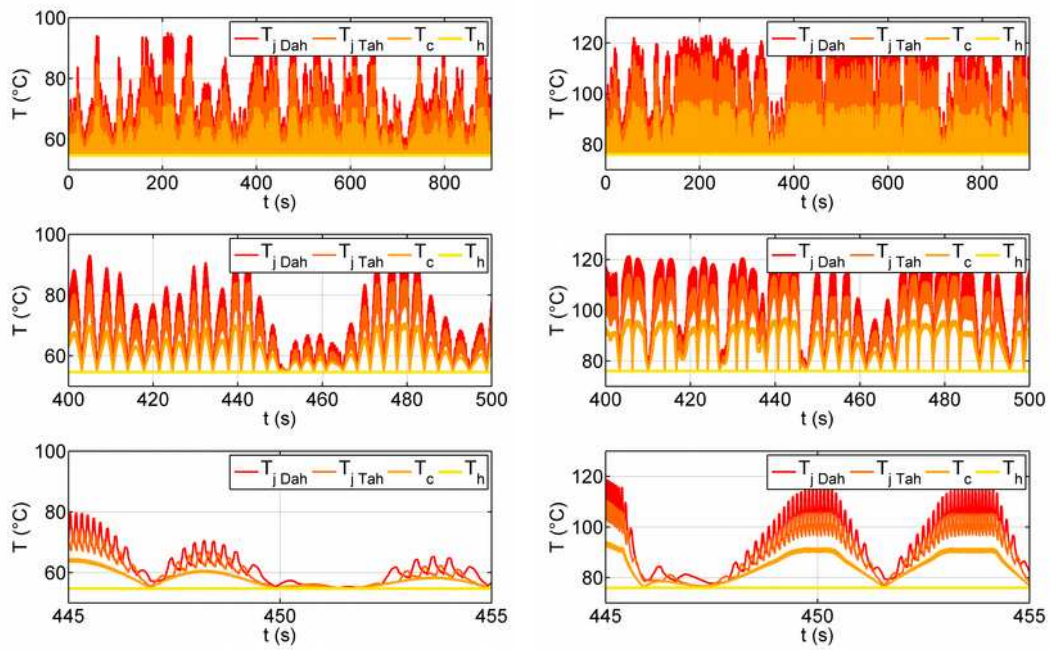


Fig. 7: Junction, case and heatsink temperature waveforms (3 time scales) for a rated current of 1400 A and heatsink thermal resistance of 7 K/kW in two sea-state examples: H_s = 3 m and T_p = 9 s for the left-hand figure (average production: 245 kW); and H_s = 6 m and T_p = 10 s for the right (average production: 590 kW)

Table III shows the lifetime prediction for two sea-state examples. The diode chip solder joint seems to be the weak link in the system. The sea-state plays an important role in semiconductor degradation, as is obvious from this table. For this reason, a sea-state distribution will be used for the remainder of this study.

Table III: Single-module lifetime prediction for two sea-state examples with a rated current of 1400 A and a heatsink temperature resistance of 7 K/kW

Sea-state	$t_{10\%\ wb\ IGBT}$ (IGBT wire bonding)	$t_{10\%\ sj\ IGBT}$ (IGBT solder joint)	$t_{10\%\ wb\ Diode}$ (Diode wire bonding)	$t_{10\%\ sj\ \mathrm{Diode}}$ (Diode solder joint)
H_s = 3 m; T_p = 9 s	∞	160 years	160 years	14 years
H_s = 6 m; T_p = 10 s	16 years	5.4 years	2.4 years	2.0 years

4.2. Results for all sea-states

106 different sea-states are introduced to model an annular sea-state distribution, from H_s = 0.5 m - T_p = 3 s up to H_s = 7.5 m - T_p = 12 s. Less than 8 minutes are needed to compute these states for the purpose of conducting a lifetime analysis for a given design. Various configurations have thus been tested to reach a 1% failure probability after 20 years of use. The heatsink thermal resistance has varied in this study from 0 to 25 K/kW, with 0 K/kW corresponds to the ideal case of an infinite heatsink. The liquid cooled heatsink typically ranges between 5 and 40 K/kW, the forced convection heatsink from 20 to 80 K/kW and the natural convection heatsink up to 200 K/kW. Semiconductor rated current varies from 1000 A to 2200 A., and the maximum current in a PMSG phase during a cycle is 1400 A.

The 20-year failure probability for the active rectifier is given in Fig. 8. The sizes of both the semiconductors and heatsink exert a tremendous impact on reliability. The initial size (I_{rated} = 1400 A ; $R_{th(h-a)}$ = 7 K/kW) displays a 5% failure probability, which for our purposes is considered too high.

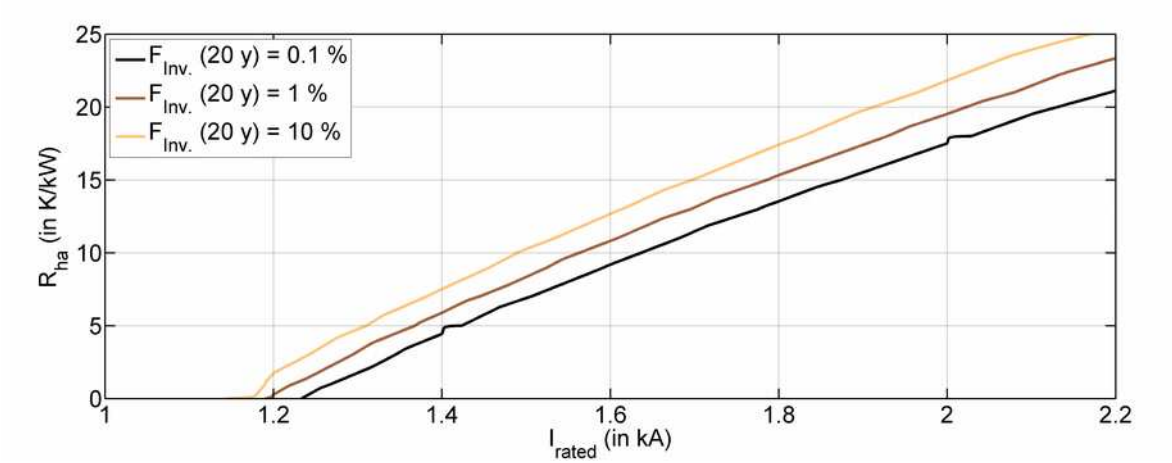


Fig. 8: Iso-failure probability at 20 years for the 6 modules in all sea-states as a function of both the heatsink thermal resistance and semiconductor current rating

Table IV lists detailed results for three points identified on the 1% failure probability curve. It has been confirmed that the diode chip solder joint has a shorter life expectancy with the full range of all possible designs.

Table IV: Single-module lifetime prediction for all sea-states with three different designs, all of which satisfy the 99% reliability constraint

Design choice	$t_{10\%\ wb\ IGBT}$	$t_{10\%\ sj\ IGBT}$	$t_{10\%\ wb\ Diode}$	$t_{10\%\ sj}$ Diode
I_{rated} = 1400 A $R_{th(h-a)}$ = 6.4 K/kW	8100 years	250 years	170 years	37 years
I_{rated} = 1600 A $R_{th(h-a)}$ = 11.3 K/kW	3400 years	240 years	160 years	38 years
I_{rated} = 1800 A $R_{th(h-a)}$ = 15.7 K/kW	1200 years	240 years	110 years	38 years

5. Conclusion

This paper has presented a methodological study on power cycling stress in an active IGBT rectifier used in a Direct Wave Energy Converter. 106 mission profiles corresponding to 106 different sea-states have been computed based on a multiphysics model; these computations have made it possible to carry out a lifetime analysis for the failure probability determination. The goal here was to set the IGBT current rating and heatsink thermal resistance in order to achieve a 99% reliability rate after 20 years for the active rectifier. The oversizing necessary for a 20-year duration is indeed significant. Results have shown the importance of such a study in the case of high-power fluctuations and high reliability requirements, which would be the typical case for Direct Wave Energy Converters.

The proposed methodology is feasible for other application with strong power fluctuations (STATCOM, photovoltaic and wind power, automotive, railway traction), other semiconductor technologies (MOSFET) or other topologies (multilevel or matrix converters). The losses and both thermal and aging models can be improved for greater precision, in particular through electro-thermal coupling.

This study is only part of the design of a complete electric conversion chain that takes the lifetime into account. In the case of DWEC, other more efficient control strategies [21] are available, though they are also more stringent in terms of power fluctuation and hence in terms of fatigue cycling in semiconductors. The influence of these control strategies for recovery modes should be considered in future research on this topic.

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7. References

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