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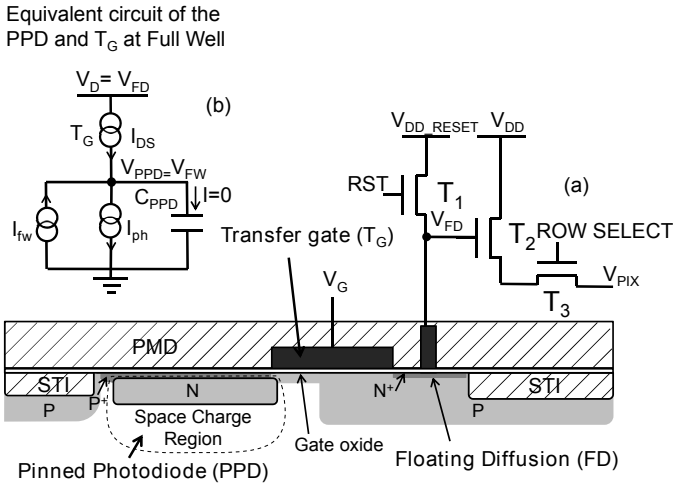

Fig. 1. (a) Cross sectional view (not to scale) of a 4T Pinned Photodiode (PPD) active pixel. (b) Equivalent circuit of the PPD and Transfer Gate (T_G) at Full Well conditions. Details on the device tested in this work: 256x256, 4.5 μm-pitch pixel array, PPD CIS 0.18 μm technology, Charge to Voltage conversion Factor (CVF)$\approx 70 \mu \mathrm{V/e^-}$.

***Abstract*—This letter presents a simple analytical model for the evaluation of the Full Well Capacity (FWC) of Pinned Photodiode CMOS Image Sensors depending on the operating conditions and on the pixel parameters. While in literature and technical documentations FWC values are generally presented as fixed values independent of the operating conditions, this work demonstrates that the PPD charge handling capability is strongly dependent on the photon flux.**

***Index Terms*—Active pixel sensors (APS), charge transfer, CMOS Image Sensors (CIS), full well capacity, pinned photodiode (PPD), pinning voltage, semiconductor device modeling.**

I. Introduction

IN Pinned Photodiodes (PPD) CMOS Image Sensors (CIS) (see Fig. 1(a) for a simplified cross-sectional view of a PPD pixel) the maximum output voltage swing can either be limited by the saturation of the readout electronics or by the PPD Full Well Capacity (FWC). The FWC is defined as the maximum amount of charge that can be stored on the photodiode capacitance. Its evaluation and the accurate identification of the limiting parameters are of primary importance for the development and the optimization of these devices. Fig. 2 shows the mean output signal ($Q_{\mathrm{out}} = V_{\mathrm{out}}/CVF$, where CVF is the Charge to Voltage Conversion Factor) as a function of the photon fluence measured at increasing integration times with a 4 transistors PPD CIS for two constant photons fluxes Φ_{ph1} and Φ_{ph2}. The sets of integration times (T_{int}) have been chosen so that the total amount of photons N_{ph} integrated at each step ($N_{\mathrm{ph}} = \Phi_{\mathrm{ph}} \times T_{\mathrm{int}}$) is the same for both curves. The figure also shows the evolution of the output signal resulting from the integration of the dark current (referred to as dark signal) at increasing integration times. Due to the extremely low dark current of the device, dark signal data have been acquired at $40°$C. The discrepancy of the saturation level with the value measured at room temperature is less than 5%. As it can be observed, the FWC strongly depends on the illumination level, with almost a factor 2 between dark and light conditions. This striking result implies that the FWC cannot be defined unless the photon flux Φ_{ph} is specified. This FWC dependence on the photon flux is very rarely taken into account, even in recent studies on the FWC in PPD CIS [1], [2]. The phenomenon has been partially addressed in [3], where the FWC dependence on Φ_{ph} is justified by means of an analytical model based on the sub-threshold current I_{DS} of the transfer transistor T_G. This model is fairly consistent with experimental data when T_G is depleted during integration, however it does not represent well the behavior of the FWC when T_G is accumulated, which is a typical operating condition used to reduce the dark current and increase the FWC in some commercial products [1], [4]. This letter presents a simple analytical model that describes the evolution of the FWC as a function of the pixel parameters, its experimental validation in the whole biasing range of T_G during integration (reffered to as V_{LOTG}) and a few illustrations of the benefit of this simple model. Starting from the previous analysis, a new method for the estimation of the pinning voltage based on the Full Well level at equilibrium is proposed. To keep the model as simple as possible, substrate effects on the transistor threshold voltage V_T and the voltage dependency of the PPD and the floating diffusion (FD) capacitances (respectively C_{PPD} and C_{FD}) have been neglected. The device tested in this work is a 256x256, 4.5 μm-pitch pixel array, manufactured in a commercial 0.18 μm PPD CIS process, with a CVF of $\approx$70 $\mu \mathrm{V/e^-}$. All measurements (unless specified) have been made at room temperature, in steady state illumination conditions and with $V_{\mathrm{LOTG}} = 0$ V.

II. Analytical Model

The condition at which no more charge can be collected by the photodiode capacitance corresponds to the point on the

The authors are with ISAE, Université de Toulouse, Toulouse, 31055, France (e-mail: alice.pelamatti@isae.fr).

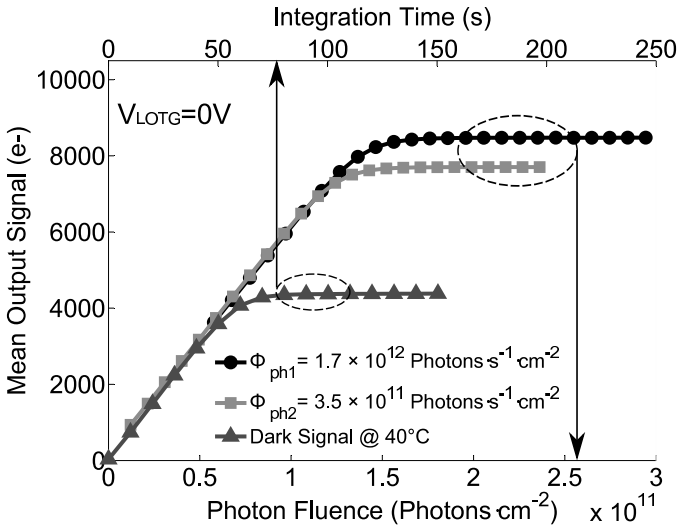

Fig. 2. Mean output signal measured for two constant photons fluxes $\Phi_{\rm ph1}$ and $\Phi_{\rm ph2}$ at increasing integration times. The figure also shows the evolution of the dark signal at $40°$C (the discrepancy of the saturation level with the value measured at room temperature is less than 5%).

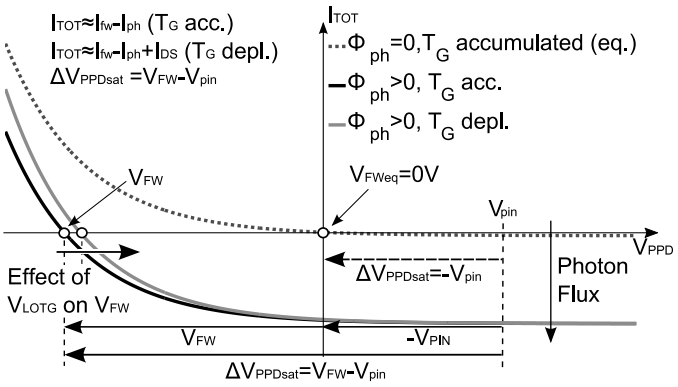

Fig. 3. Photodiode I-V characteristic (analytical model). The dotted line represents the characteristic at equilibrium (no photogeneration and no contribution of the transistor leakage current) while the solid black and grey represent the characteristic in light conditions with $\rm T_G$ respectively accumulated and depleted. The FW is reached when the total current is null, which corresponds to the open circuit condition $V_{\rm FW}$. The maximum voltage swing across the photodiode is $\Delta V_{\rm PPDsat} = V_{\rm FW} - V_{\rm pin}$. At equilibrium $V_{\rm FW} = 0V$, thus $\Delta V_{\rm PPDsat} = -V_{\rm pin}$, which means that the pinning voltage can be estimated directly from the full well level at equilibrium.

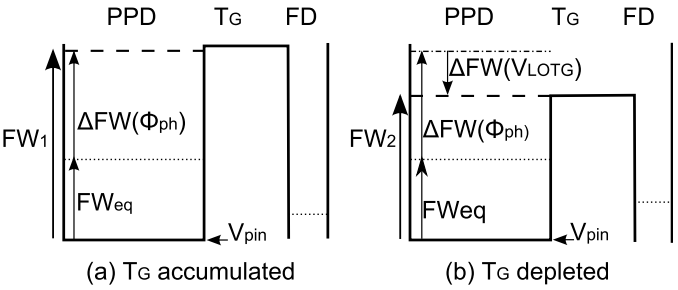

Fig. 4. Potential diagram of the PPD, $\rm T_G$ and FD structure illustrating the effect of the photon flux and $V_{\rm LOTG}$ potential on the PPD FWC for $\rm T_G$ accumulated (a) and depleted (b). $FW_{\rm eq}$ represents the Equilibrium FW level (no photo-generation and $\rm T_G$ accumulated), $\rm FW_1$ is the FW level when the sensor is illuminated (photo-generation of excess carriers) and $\rm T_G$ is accumulated, while $\rm FW_2$ is the FW level determined by the contribution of both the photo-generated excess carriers (which depends on the photon flux) and the transfer gate sub-threshold current.

diode I-V curve (Fig. 3) at which the total current is null (open circuit condition). Fig. 1(b) shows a schematic of the equivalent circuit of the PPD plus the reset transistor when the FWC condition is reached. In our model we considered three main current contributions: the photocurrent $I_{\rm ph} = \eta\Phi_{\rm ph}$ (with η an efficiency factor < 1), the sub-threshold current $I_{\rm DS}$ of $\rm T_G$, and the intrinsic forward current of the photodiode $I_{\rm fw}$. At FWC condition, it yields:

$$I'_{\rm D0} e^{\frac{V_{\rm LOTG}-V_{\rm FW}-V_T}{n v_{\rm th}}} + I_{\rm sat}\left(e^{\frac{-V_{\rm FW}}{v_{\rm th}}} - 1\right) = \eta\Phi \qquad (1)$$

where $I'_{\rm D0} = I_{\rm D0}\frac{W}{L}$, with $I_{\rm D0}$ a technological parameter and W and L respectively the width and the length of $\rm T_G$. $V_{\rm FW}$ is the PPD voltage at full well, $v_{\rm th}$ is the thermal voltage, n is the strong inversion slope factor of the transistor (which for simplicity will be considered $\rm n = 1$) and $I_{\rm sat}$ is the photodiode reverse current [5]. Generation and recombination processes within the depletion region of the PPD have been neglected. The Full Well Capacity $Q_{\rm FW}$ can be approximated as the product of $C_{\rm PPD}$ and the maximum voltage swing across the PPD $\Delta V_{\rm PPDsat}$, which, as shown in Fig. 3, can be estimated from the PPD pinning voltage $V_{\rm pin}$ [6] and the PPD saturation voltage $V_{\rm FW}$:

$$Q_{\rm FW} = -\left(V_{\rm FW} - V_{\rm pin}\right) \times C_{\rm PPD} \qquad (2)$$

where $V_{\rm FW}$ can be calculated from (1) as:

$$V_{\rm FW} = -v_{\rm th} ln\left(\frac{\eta\Phi + I_{\rm sat}}{I'_{\rm D0} e^{\frac{V_{\rm LOTG}-V_T}{v_{\rm th}}} + I_{\rm sat}}\right) \qquad (3)$$

Note that even at low photon fluxes the photodiode is in the forward region, thus $V_{\rm FW} > 0$. This implies that the maximum voltage swing across the PPD can be larger than the pinning voltage. The expression can be simplified for two biasing conditions depending on whether (a) $\rm T_G$ is accumulated ($I_{\rm DS}$ can be neglected) or (b) $\rm T_G$ is depleted (the potential barrier between the PPD and the channel of $\rm T_G$ is lowered, with consequent contribution of the sub-threshold current $I_{\rm DS}$):

$$Q^a_{\rm FW} \approx \left[V_{\rm pin} + v_{\rm th} ln\left(\frac{\eta\Phi_{\rm ph}+I_{\rm sat}}{I_{\rm sat}}\right)\right] \times C_{\rm PPD} \qquad (4)$$

$$Q^b_{\rm FW} \approx \left[V_{\rm pin} - V_{\rm LOTG} + V_T + v_{\rm th} ln\left(\frac{\eta\Phi_{\rm ph}}{I'_{\rm D0}}\right)\right] \times C_{\rm PPD} \qquad (5)$$

At the equilibrium (i.e. under no illumination and with $\rm T_G$ accumulated) the open circuit voltage $V_{\rm FW}$ is null, hence the maximum voltage swing across the photodiode directly gives an estimate of the pinning voltage. From this simple model we can easily infer the effects of the different parameters on the FWC depending on the biasing conditions of the transfer transistor. In the whole biasing range of $V_{\rm LOTG}$, $Q_{\rm FW}$ depends logarithmically on the photon flux and has a linear dependence on $V_{\rm pin}$ and $C_{\rm PPD}$. When $\rm T_G$ is depleted $V_{\rm LOTG}$ and V_T linearly affect the FWC by changing the height of the potential barrier between the photodiode and the transfer transistor channel, resulting in an electron flow from the PPD to the

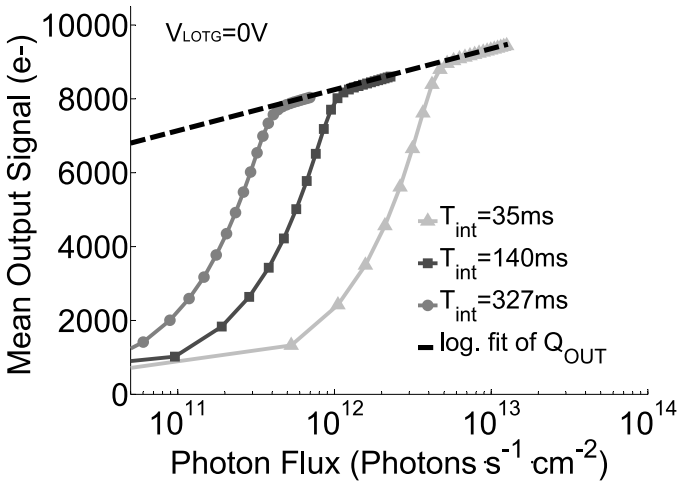

Fig. 5. Mean output signal measured for 3 constant integration times $T_{\rm int}$ at increasing photon flux. Since the FW level is increased by the increasing contribution of the photocurrent $I_{\rm ph} = \eta\Phi_{\rm ph}$, the curves never saturate. As it can be observed, the behavior of the FWC is well fitted by a logarithmic curve.

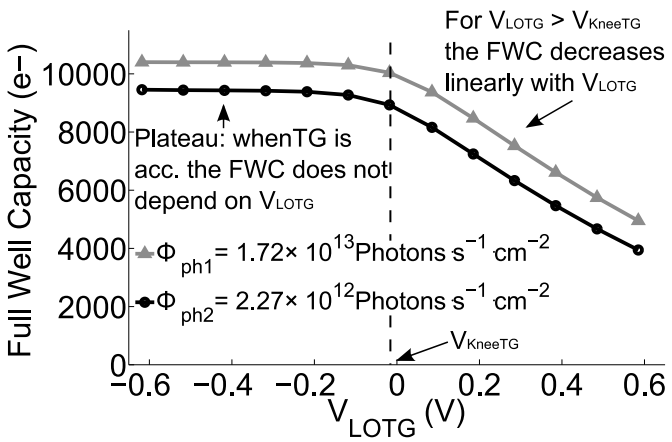

Fig. 6. FWC as a function of $V_{\rm LOTG}$ measured for two different photon fluxes. At $V_{\rm LOTG} > V_{\rm KneeTG}$ the FWC drops linearly with $V_{\rm LOTG}$, while at $V_{\rm LOTG} < V_{\rm KneeTG}$ the FW level reaches a plateau. In both biasing conditions the photon flux level adds an offset to the FWC. The FWC value presented here corresponds to the mean output signal (in e^-) $Q_{\rm out}$ determined in the saturation regime (i.e. the saturation plateau in Fig. 2).

floating diffusion [1]. The FWC dependence on the transistor parameters $I_{\rm D0}$, W and L is logarithmic. To facilitate the understanding of the model, the effect of $\Phi_{\rm ph}$ and $V_{\rm LOTG}$ on the potential distribution within the device during integration is schematized in Fig. 4.

III. Experimental Validation

Fig. 5 shows the mean output signal as a function of the photon flux measured for three different integration times. As it can be observed, the curves never truly saturate since the FW level is continuously shifted because of the increasing photocurrent contribution (due to the increasing photon flux). As predicted, the FWC is well fitted by a logarithmic function. Fig. 6 shows the FWC (corresponding to the mean output signal (in e^-) $Q_{\rm out}$ determined in the saturation regime) as a function of the biasing voltage $V_{\rm LOTG}$ for two different photon fluxes. The results are once again consistent with the model, with a plateau when T_G is accumulated and a linear drop when T_G is depleted. The crossing from one operation mode to the other is indicated as $V_{\rm KneeTG}$, which corresponds to the point at which the transistor leakage current is compensated by the diode forward current.

IV. Conclusion

A simple analytical model of the FWC of PPD CIS has been presented. This model is consistent with experimental data both under equilibrium (dark) condition, non-equilibrium (illuminated) condition and anti-blooming operating condition ($V_{\rm LOTG} > V_{\rm KneeTG}$), thus it can be very useful to identify the phenomenon limiting the FWC in a particular regime. The effect of the off-state biasing condition of the transfer transistor on the FWC has been shown and discussed. Note that the dependence on $V_{\rm LOTG}$ was also addressed in [1], [2], but no analytical model was proposed to support the experimental evidence. This letter has demonstrated that the FW level also strongly depends on the photon flux, showing that at classical illumination conditions the Full Well Capacity can be increased by a factor of 2 with respect to the value observed at equilibrium (the Equilibrium Full Well Capacity $FWC_{\rm eq}$). This result is of primary importance for the characterization and the design of PPD CIS, since if the illumination level is not provided with a FWC value, large errors can be made in the evaluation of both the FWC and the parameters determined from the FWC. The proposed approach can be used as an alternative method to the one presented in [7] to evaluate the PPD pinning voltage. The FWC has been described in steady state illumination conditions. The extension of this model to the description of the transient behavior of the FWC (such as the one reported in [2]) will be discussed in a future work.

[1] The phenomenon attributed to a feedforward mechanism in [2] is included in the proposed model through the contribution of the T_G subthreshold current.

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