



HAL
open science

Estimation and Modeling of the Full Well Capacity in Pinned Photodiode CMOS Image Sensors

Alice Pelamatti, Vincent Goiffon, Magali Estribeau, Paola Cervantes, Pierre Magnan

► **To cite this version:**

Alice Pelamatti, Vincent Goiffon, Magali Estribeau, Paola Cervantes, Pierre Magnan. Estimation and Modeling of the Full Well Capacity in Pinned Photodiode CMOS Image Sensors. IEEE Electron Device Letters, 2013, vol. 34, pp. 900-902. <10.1109/LED.2013.2260523>. <hal-00854018>

HAL Id: hal-00854018

<https://hal.science/hal-00854018v1>

Submitted on 26 Aug 2013

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization



Open Archive Toulouse Archive Ouverte (OATAO)

OATAO is an open access repository that collects the work of Toulouse researchers and makes it freely available over the web where possible.

This is an author-deposited version published in: <http://oatao.univ-toulouse.fr/>
Eprints ID: 9226

To link to this article: DOI: 10.1109/LED.2013.2260523
URL: <http://dx.doi.org/10.1109/LED.2013.2260523>

To cite this version: Pelamatti, Alice and Goiffon, Vincent and Estribeau, Magali and Cervantes, Paola and Magnan, Pierre *Estimation and Modeling of the Full Well Capacity in Pinned Photodiode CMOS Image Sensors*. (2013) IEEE Electron Device Letters, vol. 34 (n° 7). pp. 900-902. ISSN 0741-3106

Any correspondence concerning this service should be sent to the repository administrator: staff-oatao@inp-toulouse.fr

Estimation and Modeling of the Full Well Capacity in Pinned Photodiode CMOS Image Sensors

Alice Pelamatti, Vincent Goiffon, *Member, IEEE*, Magali Estribeau, *Member, IEEE*, Paola Cervantes, Pierre Magnan, *Member, IEEE*

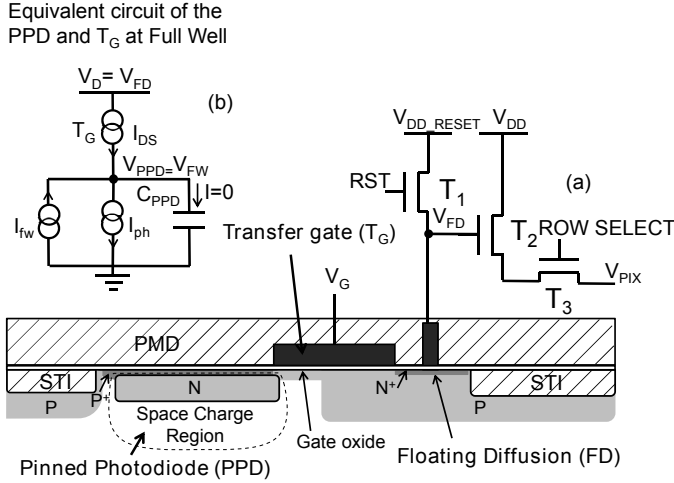


Fig. 1. (a) Cross sectional view (not to scale) of a 4T Pinned Photodiode (PPD) active pixel. (b) Equivalent circuit of the PPD and Transfer Gate (T_G) at Full Well conditions. Details on the device tested in this work: 256x256, 4.5 μm -pitch pixel array, PPD CIS 0.18 μm technology, Charge to Voltage conversion Factor (CVF) $\approx 70 \mu\text{V}/e^-$.

Abstract—This letter presents a simple analytical model for the evaluation of the Full Well Capacity (FWC) of Pinned Photodiode CMOS Image Sensors depending on the operating conditions and on the pixel parameters. While in literature and technical documentations FWC values are generally presented as fixed values independent of the operating conditions, this work demonstrates that the PPD charge handling capability is strongly dependent on the photon flux.

Index Terms—Active pixel sensors (APS), charge transfer, CMOS Image Sensors (CIS), full well capacity, pinned photodiode (PPD), pinning voltage, semiconductor device modeling.

I. INTRODUCTION

IN Pinned Photodiodes (PPD) CMOS Image Sensors (CIS) (see Fig. 1(a) for a simplified cross-sectional view of a PPD pixel) the maximum output voltage swing can either be limited by the saturation of the readout electronics or by the PPD Full Well Capacity (FWC). The FWC is defined as the maximum amount of charge that can be stored on the photodiode capacitance. Its evaluation and the accurate identification of the limiting parameters are of primary importance for the development and the optimization of these devices. Fig. 2 shows the mean output signal ($Q_{\text{out}} = V_{\text{out}}/\text{CVF}$, where

CVF is the Charge to Voltage Conversion Factor) as a function of the photon fluence measured at increasing integration times with a 4 transistors PPD CIS for two constant photons fluxes $\Phi_{\text{ph}1}$ and $\Phi_{\text{ph}2}$. The sets of integration times (T_{int}) have been chosen so that the total amount of photons N_{ph} integrated at each step ($N_{\text{ph}} = \Phi_{\text{ph}} \times T_{\text{int}}$) is the same for both curves. The figure also shows the evolution of the output signal resulting from the integration of the dark current (referred to as dark signal) at increasing integration times. Due to the extremely low dark current of the device, dark signal data have been acquired at 40°C. The discrepancy of the saturation level with the value measured at room temperature is less than 5%. As it can be observed, the FWC strongly depends on the illumination level, with almost a factor 2 between dark and light conditions. This striking result implies that the FWC cannot be defined unless the photon flux Φ_{ph} is specified. This FWC dependence on the photon flux is very rarely taken into account, even in recent studies on the FWC in PPD CIS [1], [2]. The phenomenon has been partially addressed in [3], where the FWC dependence on Φ_{ph} is justified by means of an analytical model based on the sub-threshold current I_{DS} of the transfer transistor T_G . This model is fairly consistent with experimental data when T_G is depleted during integration, however it does not represent well the behavior of the FWC when T_G is accumulated, which is a typical operating condition used to reduce the dark current and increase the FWC in some commercial products [1], [4]. This letter presents a simple analytical model that describes the evolution of the FWC as a function of the pixel parameters, its experimental validation in the whole biasing range of T_G during integration (referred to as V_{LOTG}) and a few illustrations of the benefit of this simple model. Starting from the previous analysis, a new method for the estimation of the pinning voltage based on the Full Well level at equilibrium is proposed. To keep the model as simple as possible, substrate effects on the transistor threshold voltage V_T and the voltage dependency of the PPD and the floating diffusion (FD) capacitances (respectively C_{PPD} and C_{FD}) have been neglected. The device tested in this work is a 256x256, 4.5 μm -pitch pixel array, manufactured in a commercial 0.18 μm PPD CIS process, with a CVF of $\approx 70 \mu\text{V}/e^-$. All measurements (unless specified) have been made at room temperature, in steady state illumination conditions and with $V_{\text{LOTG}} = 0 \text{ V}$.

II. ANALYTICAL MODEL

The condition at which no more charge can be collected by the photodiode capacitance corresponds to the point on the

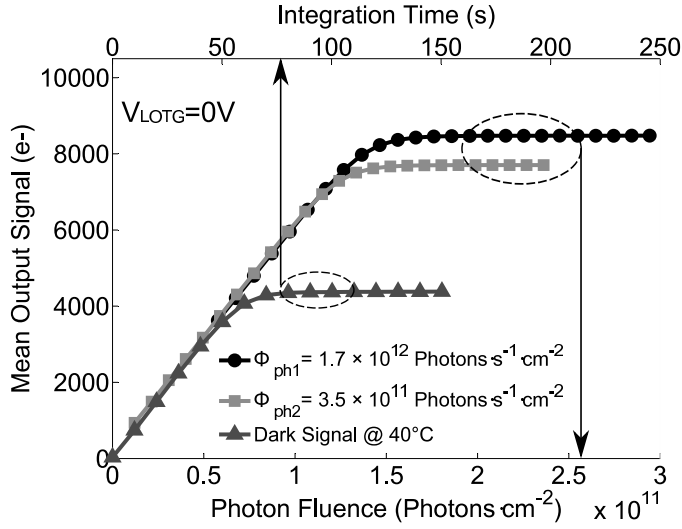


Fig. 2. Mean output signal measured for two constant photons fluxes Φ_{ph1} and Φ_{ph2} at increasing integration times. The figure also shows the evolution of the dark signal at 40°C (the discrepancy of the saturation level with the value measured at room temperature is less than 5%).

diode I-V curve (Fig. 3) at which the total current is null (open circuit condition). Fig. 1(b) shows a schematic of the equivalent circuit of the PPD plus the reset transistor when the FWC condition is reached. In our model we considered three main current contributions: the photocurrent $I_{ph} = \eta\Phi_{ph}$ (with η an efficiency factor < 1), the sub-threshold current I_{DS} of T_G , and the intrinsic forward current of the photodiode I_{fw} . At FWC condition, it yields:

$$I'_{D0} e^{\frac{V_{LOTG} - V_{FW} - V_T}{n v_{th}}} + I_{sat} \left(e^{-\frac{V_{FW}}{v_{th}}} - 1 \right) = \eta\Phi \quad (1)$$

where $I'_{D0} = I_{D0} \frac{W}{L}$, with I_{D0} a technological parameter and W and L respectively the width and the length of T_G . V_{FW} is the PPD voltage at full well, v_{th} is the thermal voltage, n is the strong inversion slope factor of the transistor (which for simplicity will be considered $n = 1$) and I_{sat} is the photodiode reverse current [5]. Generation and recombination processes within the depletion region of the PPD have been neglected. The Full Well Capacity Q_{FW} can be approximated as the product of C_{PPD} and the maximum voltage swing across the PPD ΔV_{PPDsat} , which, as shown in Fig. 3, can be estimated from the PPD pinning voltage V_{pin} [6] and the PPD saturation voltage V_{FW} :

$$Q_{FW} = -(V_{FW} - V_{pin}) \times C_{PPD} \quad (2)$$

where V_{FW} can be calculated from (1) as:

$$V_{FW} = -v_{th} \ln \left(\frac{\eta\Phi + I_{sat}}{I'_{D0} e^{\frac{V_{LOTG} - V_T}{v_{th}}} + I_{sat}} \right) \quad (3)$$

Note that even at low photon fluxes the photodiode is in the forward region, thus $V_{FW} > 0$. This implies that the maximum voltage swing across the PPD can be larger than the pinning voltage. The expression can be simplified for two biasing conditions depending on whether (a) T_G is accumulated (I_{DS}

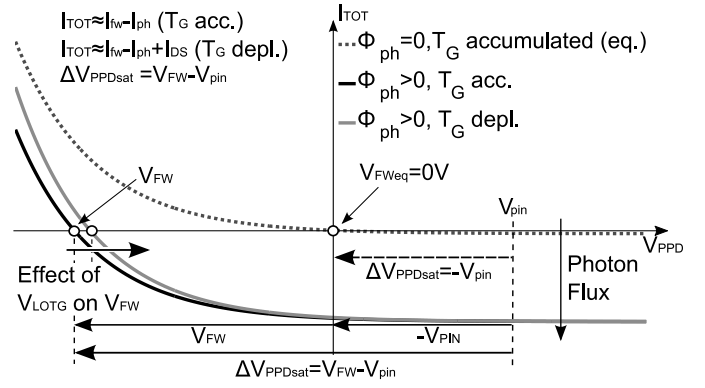


Fig. 3. Photodiode I-V characteristic (analytical model). The dotted line represents the characteristic at equilibrium (no photogeneration and no contribution of the transistor leakage current) while the solid black and grey represent the characteristic in light conditions with T_G respectively accumulated and depleted. The FW is reached when the total current is null, which corresponds to the open circuit condition V_{FW} . The maximum voltage swing across the photodiode is $\Delta V_{PPDsat} = V_{FW} - V_{pin}$. At equilibrium $V_{FW} = 0V$, thus $\Delta V_{PPDsat} = -V_{pin}$, which means that the pinning voltage can be estimated directly from the full well level at equilibrium.

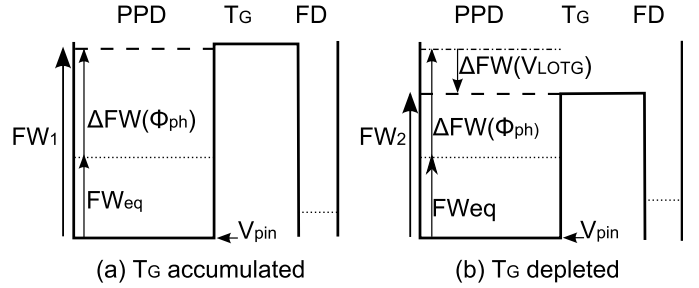


Fig. 4. Potential diagram of the PPD, T_G and FD structure illustrating the effect of the photon flux and V_{LOTG} potential on the PPD FWC for T_G accumulated (a) and depleted (b). $FWeq$ represents the Equilibrium FW level (no photo-generation and T_G accumulated), FW_1 is the FW level when the sensor is illuminated (photo-generation of excess carriers) and T_G is accumulated, while FW_2 is the FW level determined by the contribution of both the photo-generated excess carriers (which depends on the photon flux) and the transfer gate sub-threshold current.

can be neglected) or (b) T_G is depleted (the potential barrier between the PPD and the channel of T_G is lowered, with consequent contribution of the sub-threshold current I_{DS}):

$$Q_{FW}^a \approx \left[V_{pin} + v_{th} \ln \left(\frac{\eta\Phi_{ph} + I_{sat}}{I_{sat}} \right) \right] \times C_{PPD} \quad (4)$$

$$Q_{FW}^b \approx \left[V_{pin} - V_{LOTG} + V_T + v_{th} \ln \left(\frac{\eta\Phi_{ph}}{I'_{D0}} \right) \right] \times C_{PPD} \quad (5)$$

At the equilibrium (i.e. under no illumination and with T_G accumulated) the open circuit voltage V_{FW} is null, hence the maximum voltage swing across the photodiode directly gives an estimate of the pinning voltage. From this simple model we can easily infer the effects of the different parameters on the FWC depending on the biasing conditions of the transfer transistor. In the whole biasing range of V_{LOTG} , Q_{FW} depends logarithmically on the photon flux and has a linear dependence on V_{pin} and C_{PPD} . When T_G is depleted V_{LOTG} and V_T linearly affect the FWC by changing the height of the potential barrier between the photodiode and the transfer transistor channel, resulting in an electron flow from the PPD to the

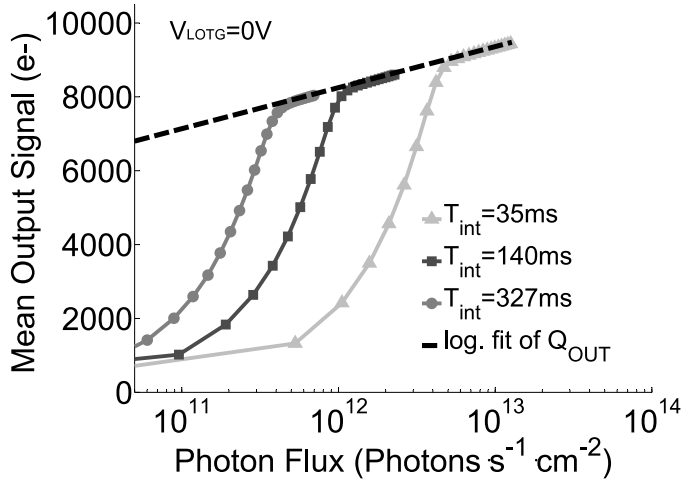


Fig. 5. Mean output signal measured for 3 constant integration times T_{int} at increasing photon flux. Since the FW level is increased by the increasing contribution of the photocurrent $I_{\text{ph}} = \eta\Phi_{\text{ph}}$, the curves never saturate. As it can be observed, the behavior of the FWC is well fitted by a logarithmic curve.

floating diffusion¹. The FWC dependence on the transistor parameters I_{D0} , W and L is logarithmic. To facilitate the understanding of the model, the effect of Φ_{ph} and V_{LOTG} on the potential distribution within the device during integration is schematized in Fig. 4.

III. EXPERIMENTAL VALIDATION

Fig. 5 shows the mean output signal as a function of the photon flux measured for three different integration times. As it can be observed, the curves never truly saturate since the FW level is continuously shifted because of the increasing photocurrent contribution (due to the increasing photon flux). As predicted, the FWC is well fitted by a logarithmic function. Fig. 6 shows the FWC (corresponding to the mean output signal (in e^-) Q_{out} determined in the saturation regime) as a function of the biasing voltage V_{LOTG} for two different photon fluxes. The results are once again consistent with the model, with a plateau when T_G is accumulated and a linear drop when T_G is depleted. The crossing from one operation mode to the other is indicated as V_{KneeTG} , which corresponds to the point at which the transistor leakage current is compensated by the diode forward current.

IV. CONCLUSION

A simple analytical model of the FWC of PPD CIS has been presented. This model is consistent with experimental data both under equilibrium (dark) condition, non-equilibrium (illuminated) condition and anti-blooming operating condition ($V_{\text{LOTG}} > V_{\text{KneeTG}}$), thus it can be very useful to identify the phenomenon limiting the FWC in a particular regime. The effect of the off-state biasing condition of the transfer transistor on the FWC has been shown and discussed. Note that the dependence on V_{LOTG} was also addressed in [1], [2], but no

¹The phenomenon attributed to a feedforward mechanism in [2] is included in the proposed model through the contribution of the T_G subthreshold current.

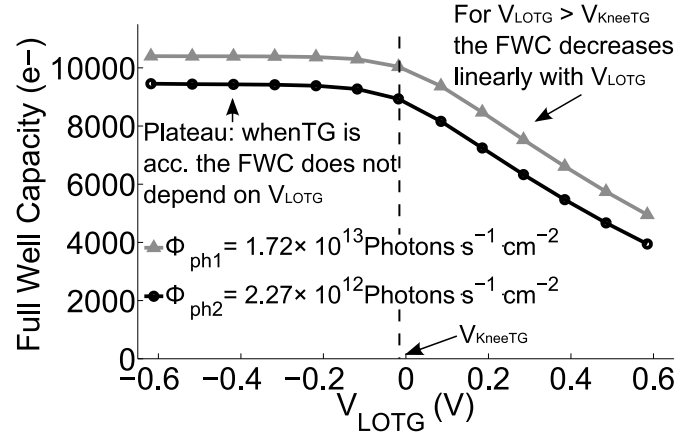


Fig. 6. FWC as a function of V_{LOTG} measured for two different photon fluxes. At $V_{\text{LOTG}} > V_{\text{KneeTG}}$ the FWC drops linearly with V_{LOTG} , while at $V_{\text{LOTG}} < V_{\text{KneeTG}}$ the FW level reaches a plateau. In both biasing conditions the photon flux level adds an offset to the FWC. The FWC value presented here corresponds to the mean output signal (in e^-) Q_{out} determined in the saturation regime (i.e. the saturation plateau in Fig. 2).

analytical model was proposed to support the experimental evidence. This letter has demonstrated that the FW level also strongly depends on the photon flux, showing that at classical illumination conditions the Full Well Capacity can be increased by a factor of 2 with respect to the value observed at equilibrium (the Equilibrium Full Well Capacity FWC_{eq}). This result is of primary importance for the characterization and the design of PPD CIS, since if the illumination level is not provided with a FWC value, large errors can be made in the evaluation of both the FWC and the parameters determined from the FWC. The proposed approach can be used as an alternative method to the one presented in [7] to evaluate the PPD pinning voltage. The FWC has been described in steady state illumination conditions. The extension of this model to the description of the transient behavior of the FWC (such as the one reported in [2]) will be discussed in a future work.

REFERENCES

- [1] B. Mheen, Y.-J. Song, and A. Theuwissen, "Negative offset operation of four-transistor CMOS image pixels for increased well capacity and suppressed dark current," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 347–349, Apr. 2008.
- [2] M. Sarkar, B. Buttgen, and A. Theuwissen, "Feedforward effect in standard CMOS pinned photodiodes," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1154–1161, Mar. 2013.
- [3] J. Bogaerts, G. Meynants, K. Van Wichelen, and E. Gillisjans, "Recent radiation testing on 180 nm and 110 nm CMOS image sensor processes," presented at *CNES Workshop on Radiation Effects on Optoelectronic Detectors*, Toulouse, Nov. 2012.
- [4] T. Watanabe, J.-H. Park, S. Aoyama, K. Isobe, and S. Kawahito, "Effects of negative-bias operation and optical stress on dark current in CMOS image sensors," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1512–1518, Jul. 2010.
- [5] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, 2nd ed. Cambridge University Press, Aug. 2009.
- [6] A. Krymski and K. Feklistov, "Estimates for scaling of pinned photodiodes," in *Proc. IEEE Workshop On CCD and Advanced Image Sensors*, Jun. 2005, pp. 60–63.
- [7] J. Tan, B. Buttgen, and A. Theuwissen, "Analyzing the radiation degradation of 4-transistor deep submicron technology CMOS image sensors," *IEEE Sensors J.*, vol. 12, no. 6, pp. 2278–2286, Jun. 2012.