



HAL
open science

Effectiveness of wafer level test for electromigration wear out reporting in advanced CMOS interconnects reliability assessment

Franck Lionel Bana, Emmanuel Petitprez, David Ney, Lucile Arnaud, Yves Wouters

► To cite this version:

Franck Lionel Bana, Emmanuel Petitprez, David Ney, Lucile Arnaud, Yves Wouters. Effectiveness of wafer level test for electromigration wear out reporting in advanced CMOS interconnects reliability assessment. *Microelectronic Engineering*, 2013, 106, pp.195-199. 10.1016/j.mee.2013.01.022 . hal-00850229

HAL Id: hal-00850229

<https://hal.science/hal-00850229>

Submitted on 13 May 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution - NonCommercial 4.0 International License

Effectiveness of wafer level test for electromigration wear out reporting in advanced CMOS interconnects reliability assessment

F. Bana^{a,b,*}, E. Petitprez^a, D. Ney^a, L. Arnaud^c, Y. Wouters^b

^aSTMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France

^bSIMaP UMR5266 CNRS/UJF/Grenoble-INP, 1130 rue de la piscine, BP 75, 38402 St-Martin-d'Hères Cedex, France

^cCEA-Leti Minatec, 17 rue des martyrs, 38054 Grenoble Cedex 09, France

Electromigration (EM) copper lines reliability is assessed through standard wafer level (WL) and PL (PL) test in the present work. Since these tests are highly accelerated, one of the main questions as in all reliability studies is the effectiveness of reporting failure phenomena as they occur under use conditions. WL is known to have been intensively used for fast EM process monitoring on high volumes with elevated stress conditions. On the other hand, the PL test having less aggressive stress conditions is used in a process qualification scheme. We use the later in this study as a reference to evaluate WL test results through various processes. Thus, the present paper deals with the ability of WL in comparison to PL to effectively report reliability performances variations for different Cu lines process modifications. Results from WL reliability and PL reliability are compared in terms of lifetime variations and standard deviation evolution. Only limited correlation is found, suggesting that the failure mechanisms acting for both methods are not the same. Moreover, the results of this study highlight the need of defining new reliable EM testing structures and methods compatible with high volumes monitoring.

1. Introduction

EM refers to matter displacement driven by an electrical current in metal lines. Electrons from an applied electric field transfer their momentum to metallic atoms whose movement creates voids in the line and even complete line openings [1]. EM is an increasing reliability concern in the microelectronic industry, exacerbated by continuous down scaling of on-chip interconnects which drive more and more currents. Interconnects resistance against EM phenomenon is assessed by performing accelerated aging tests on simple configurations structures (in comparison with more complex architectures encountered in real operating circuits). Accelerating factors are temperature T and current density j , according to the empirical Black's equation [2]:

$$MTF = Aj^{-n} \exp(E_a/kT)$$

where MTF is the median time to failure, n and E_a the current density exponent and the activation energy respectively, k the Boltzmann's constant and A is a geometric factor.

Two accelerated aging tests are commonly used to characterize electromigration. PL test is used during process qualification to predict interconnects lifetime at use conditions. Extrapolation to using conditions is performed using experimental data and Black's equation based models. For this test, moderated conditions are used and the tests may last up to some weeks. These long test times are a drawback from a manufacturing point of view, since fast feedback is needed to pick up eventual process drifts. Moreover, there is a time over cost due to dice packaging in assembly lines. At the other side, in a production line context, WL is used to track process drifts which can occur. Test conditions of WL are highly accelerated. Few seconds to hours are sufficient to complete the test. The advantage here is the ability to quickly test high wafer volumes. Nevertheless, the fundamental point rising when using WL is whether the failure mechanisms acting here are the same as at operating conditions. Considering PL as the reference test (whose conditions are closer to operating ones), the question boils down to find a correlation between WL and PL test. Some interesting results have been mentioned about correlation between these two testing methods. However the reported results are sometimes opposed and recommendations in using WL must be considered [3–5].

Correlation of EM performances between the two testing methods is therefore a critical point that directly impacts EM reliability strategy in industry. Such a correlation would lead to a more robust EM investigation technique dealing indifferently with process

* Corresponding author at: STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France.

E-mail address: franck-lionel.bana@st.com (F. Bana).

qualification and line control. In this paper, we propose an experimental study to evaluate in which extent WL strategy could be used to respond to this requirement. Dual damascene Cu lines with different processes are evaluated through both methods. WL results are compared to PL ones in terms of lifetime and standard deviation variations.

2. Experimental

Electromigration test structures used in this study are dual damascene Cu via/lines embedded in a low- k ($k = 2.5$) dielectric. The lines are $225 \mu\text{m}$ long and 63 nm wide. They are surrounded (bottom and sidewalls) by a thin TaN/Ta diffusion barrier and capped with a SiCN based dielectric. Each line extremity is ended by one via. Upstream and downstream electron flow configurations are investigated (see Fig. 1).

The test structures are repeated twice per die and located close to each other to avoid intra-die dimensional fluctuations on each sampling population. EM test is first conducted at WL on one of the twin structures; the second one is then ceramic packaged for PL test. The sampling for each test is at least 50 dice. Tests conditions are summarized in Table 1. One can notice that for PL test, temperature is controlled by an oven while for WL test, Joule heating controls the line temperature by applying a constant current which depends on the line's temperature coefficient of resistance.

The EM performances are evaluated by studying the resistance evolution of a stressed line. While for PL the resistance trace is characterized by a step and then a gradual increase, WL shows an abrupt resistance step increase to the infinite, characteristic of a dramatic line opening [6]. The failure criteria we considered in our study are the time of the abrupt resistance increase in the case of WL test and a 10% initial resistance increase in the case of PL test. We note that the 10% criterion in the PL samples is within the resistance step increase so that the failure time is recorded when the created void reaches the bottom line trench.

Specific steps of the back-end fabrication process were deliberately modified to induce EM performance variations. The process modifications are either geometrical or concern the line chemistry.

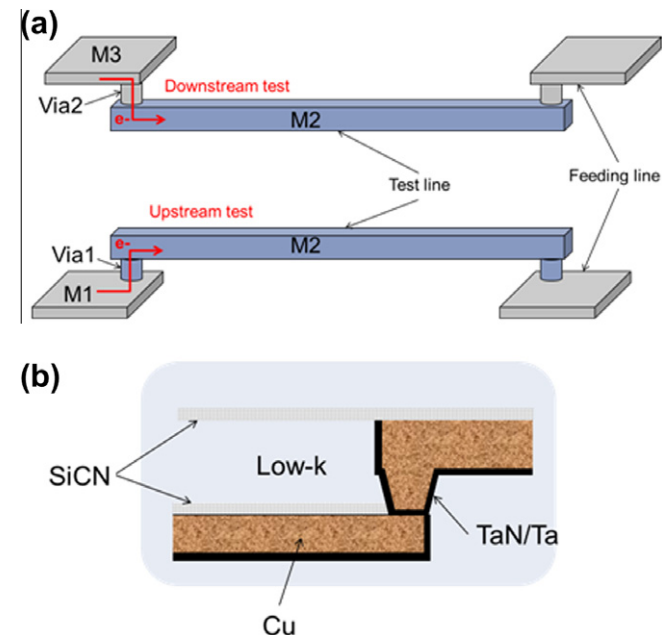


Fig. 1. Schematic of the test structure (a) electron flow configurations; and (b) copper and capping layers (cross section).

Table 1

Test conditions for PL and WL electromigration tests.

	j (MA/cm ²)	T (°C)	Failure criterion (time at)
PL	2	300	10% initial resistance increase
WL	~ 70	200–250	Electrical open circuit

The correlation between the two testing methods was studied using these samples which characteristics are detailed in Table 2.

2.1. Experimental data

2.1.1. Reproducibility of the process

A preliminary investigation is to check the reproducibility of measurements for the processes studied in this work. For that purpose, we compared for each technique two wafers of the same lot and process. The purpose is to determine if any wafer to wafer variation maybe present at either PL or WL. If yes, do these variations may be attributable to the testing method or to a “natural” wafer to wafer variation. Fig. 2 shows the results of this preliminary verification conducted at both PL and WL for process sample B.

There is no evidence of a particular mismatch between two wafers of same lot and process for both PL and WL. In each case, we obtain failure times distributions which are almost merged. The same results are obtained for the other processes studied (not shown here). This first result overcomes questioning about fluctuations on measurements of electromigration performances for different wafers of the same process for the coming tests.

2.1.2. Lifetime variations

In a second step, we study how each test method behaves in presence of lifetime variations. We thus investigate samples A1, A2, B and C with downstream electron flow configuration. This is done by comparing the log-normal failure times' distributions of couple of samples (A1, B) and (A2, C) at both PL and WL.

In a first step, sample B is compared to reference sample A1. At PL, an increase of factor 3 is observed between the improved barrier sample B and the reference process sample A1 (Fig. 3a). On the other hand, the same samples compared at WL (Fig. 3b) do not exhibit any change in lifetime. Since the two distributions are merged, we infer that WL is unable to faithfully reproduced lifetime improvements of sample B. Considering this fact inversely, it is likely that any process drift leading to degraded EM performances (at least down to one third of the lifetime target) may not be detectable with WL test.

Next on Fig. 4, the process used for sample C shows an even more pronounced lifetime improvement with respect to reference process. At PL, the MTF is 6 times higher for sample C than for sam-

Table 2

Sample description (the colors link the samples which are compared one to the other).

Sample	Metal level (electron flow)	Metal level of the feeding line	Description
A1	M2 (downstream)	M3	Reference process
A2	M1 (downstream)	M2	
B	M2 (downstream)	M3	Improved barrier
C	M1 (downstream)	M2	Improved etching
D	M2 (upstream)	M1	Reference process with large via misalignment
E	M2 (upstream)	M1	Reference process with small via misalignment

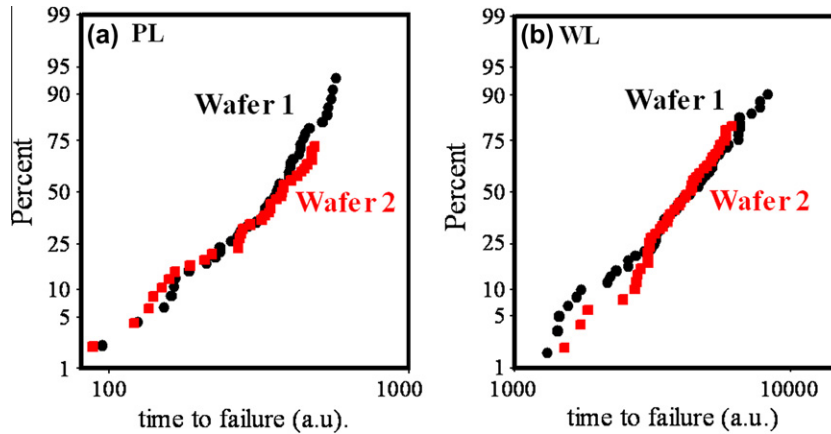


Fig. 2. Time to failure distributions (TTF) at PL (a) and WL (b) for sample B: process reproducibility verification.

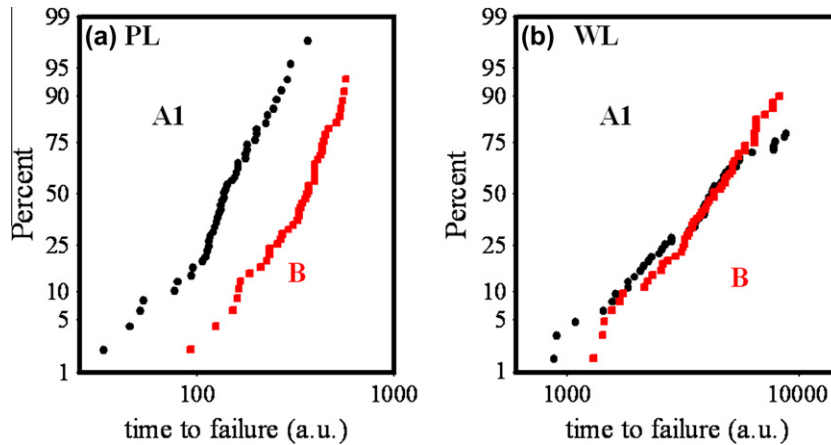


Fig. 3. TTF distributions of samples A1 vs. B for PL (a) and WL (b); EM improved performances are not visible for the WL test.

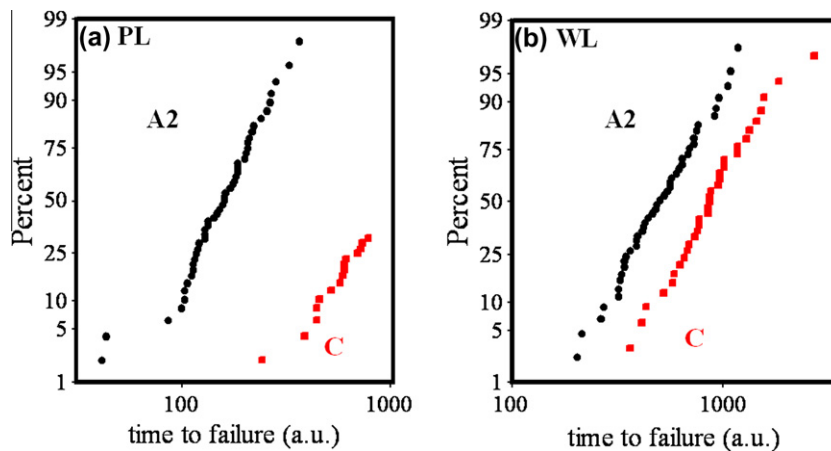


Fig. 4. TTF distributions of samples A2 vs. C for PL (a) and WL (b).

ple A2. Unlike previously, a lifetime increase is now also seen at WL although the MTF ratio between samples C and A2 is much lower at WL than at PL.

These results (Figs. 3 and 4) lead to two major findings. First, they point out the difficulty to assign any quantification to WL data. This, in turn, prevents from setting efficient specification lim-

its for process reliability monitoring. Secondly, they show that WL is unable to detect all EM performances variations. The latter is confirmed by results obtained with samples B and C. The improved barrier stoichiometry in sample B obviously enhances Cu wettability which thereafter allows a more robust Cu microstructure profile against electromigration. For sample C, we played with the line's

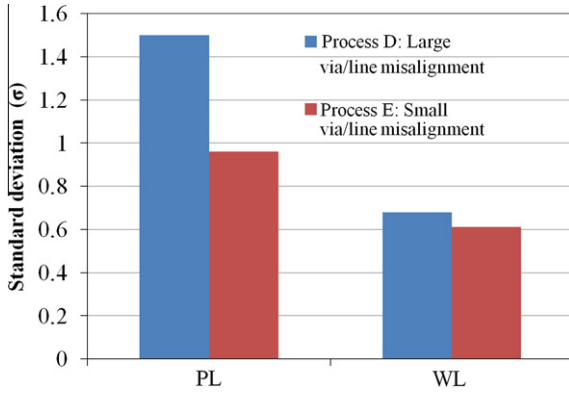


Fig. 5. Comparison of σ for samples D and E for PL and WL.

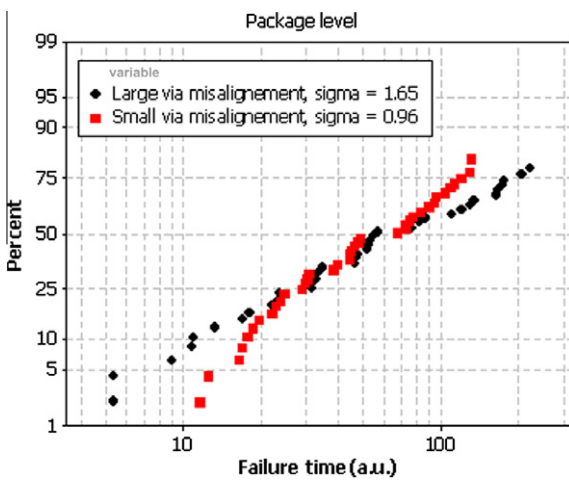


Fig. 6. The high sigma values in the PL test are not due to bimodality of TTF distributions.

geometry. The sensitivity of the WL is therefore process dependent. Considering all possible process modifications which can be encountered in dual-damascene fabrication, this selective sensitivity appears as a serious drawback for an effective electromigration evaluation method.

2.1.3. Standard deviation evolution

Our third comparison item for a correlation between WL and PL is the standard deviation (σ) of failure time's distributions. Similar

σ is expected in both tests if same failure mechanisms are assumed to occur. We have chosen not optimized processes to evaluate this last point. This is done on upstream structures of samples D and E. For these samples, there is a misalignment between via 2 and the feeding line located at M1 level. This particular configuration has been obtained using a trench first hard mask (TiN) process.

It is first interesting to note that via misalignment reduction between sample D and E is clearly seen on the σ values for PL test (Fig. 5). The greater is via to line misalignment, the larger the standard deviation of failure time's distribution will be. Meanwhile, with WL any significant difference between the two processes is seen. This indicates that the failure mechanisms occurring at WL are not sensitive to via weakness whereas the electromigration degradation is located at the cathode via vicinity [7]. The results also raise an uncertainty on the ability of WL test to detect manufacturing process issues that broaden the lifetime distribution, such as the occurrence of extrinsic failures.

An analysis of samples D and E TTF distributions show there is no reason to consider bimodality (Fig. 6). If present, the possible early and late modes are so that the bimodality is not detected. We have analyzed the same structure in the downstream configuration and for both PL and WL; we obtain similar values of standard deviation around 0.6 in the case of large and small via/line misalignments respectively.

2.1.4. Process maturity evolution

Going further into the analysis, we followed EM performance on three lots of different maturities and processing date. The results are presented in Fig. 5 where the oldest lot is X and the latest one is Z. Each lot is characterized by a set of process variations which are modified to improve EM performances along the time. An evidence of no matching between PL and WL electromigration data is demonstrated again here in Fig. 7. After showing the selective sensitivity of, we point here the inability of WL to follow a set of process modifications that improve interconnects reliability along the time.

3. Discussion

The results collected in this study indicate almost no correlation between PL and WL in the range of our experimental conditions. WL appeared to be selectively sensitive to process variations; the only visible impact being that of geometrical modifications of the tested line. In order to understand the reasons of these differences, we localized voids corresponding to electromigration failure of each of the testing techniques. Post-mortem failure analyses are shown on Fig. 8. The voids are spotted by their distance D from

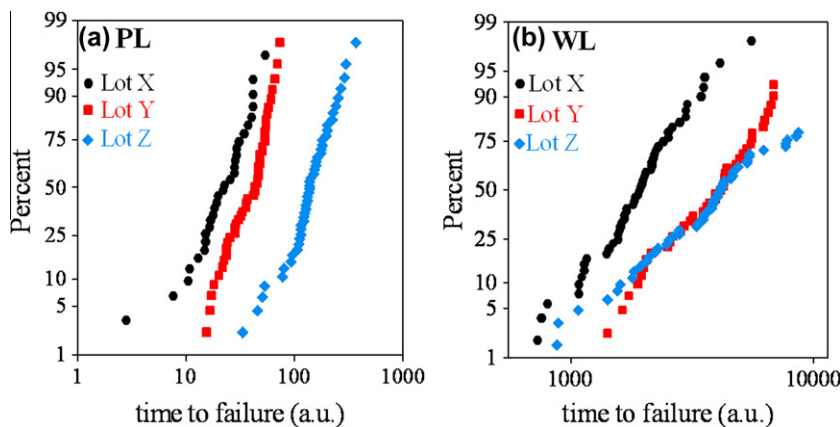


Fig. 7. Comparison of EM performances on three lots at different steps of process maturity.

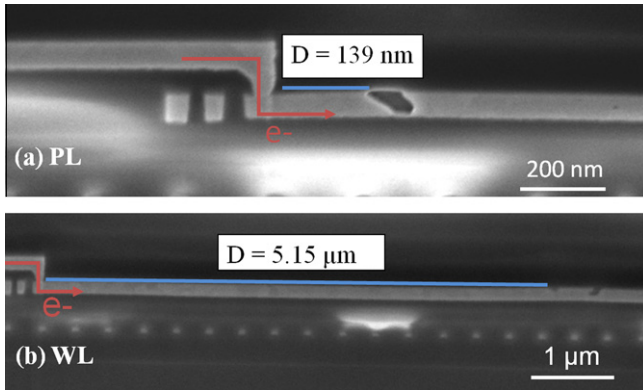


Fig. 8. EM void location after downstream (a) PL and (b) WL tests.

the cathode via. We observe for PL test that the EM void is located close to the cathode via while in the WL case, (where we stopped the test right before complete line opening); the void is much more distant from the cathode via. This observation confirms previous assumptions on void positions for both methods [8] and moreover, supports the assumption of different failure mechanisms for the two testing methods.

Given the accelerated test conditions and the width of current leads, a strong temperature gradient is present along the line during a WL test. In this case, the line extremities are colder than the line middle. Wider current leads facilitating heat evacuation from the line extremities. This temperature configuration may then explain the void location far from the cathode via in the case of WL. It may also explain the lack of sensitivity of WL test for different via/line misalignments (see Fig. 5). However, it hardly accounts for the other process modifications (see Fig. 3). Based on all these results, we strongly believe there is a potential risk of using WL EM test for manufacturing process reliability monitoring. We suggest that new test structures should be developed to respond to fast feedback requirement, while keeping relevant failure mechanisms. In this context multi-link [9] and self-heating structures [10] for example seem to be good candidates and should be thoroughly investigated. They could allow reducing the testing current used now in monitoring while keeping the same feedback in time and meeting the

same failure mechanisms as at use conditions. Another important point to mention is the possibility to address lower stress temperatures with a reasonable test time [11]. Moreover, multi-link structures present the advantage of providing more data points which is a critical aspect for early failures investigations because of addressing low failure rates in TTF distributions.

4. Conclusion

We have presented a comparison between WL and PL electromigration tests on Cu dual damascene lines. The objective of the study being the evaluation WL electromigration effectiveness for manufacturing process drifts tracking. Almost no correlation was found in the range of experimental conditions used, this preventing any quantification of from WL. We also demonstrated that WL test sensitivity does not allow following all process-related performance variations that have being applied. Finally, we observed that the failure mechanisms occurring during a WL test are far different than those acting at operating conditions. We therefore conclude that the use of WL test for manufacturing reliability control present a potential risk since it may not reflect the real interconnect electromigration performances and would not address weakness of via or extrinsic failures linked to via robustness. It would be necessary to develop new EM test structures able to follow process modifications and answering to fast feedback requirements. Particular attention must be paid on multilink and self-heating structures which can meet these challenges.

References

- [1] C.-K. Hu, *Microelectron. Reliab.* 46 (2-4) (2006) 213-231.
- [2] J.R. Black, *Proc. IEEE* 57 (9) (1969) 1587-1594.
- [3] M. Lepper, R. Bauer, A.E. Zitzelsberger, *IEEE Int. Reliab. Workshop, Final Report*, 2000 pp. 70-73.
- [4] C. Ryu et al., *IEEE Int. Reliab. Phys. Symp. Proc.* (2001) 189-193.
- [5] O. Aubel et al., *IEEE Trans. Device Mater. Reliab.* 7 (2) (2007) 270-277.
- [6] L. Doyen et al., *J. App. Phys.* 104 (12) (2008).
- [7] R.G. Filippi, P.C. Wang, A. Brendler, J.R. Lloyd, *App. Phys. Lett.* 95 7 (2009).
- [8] D. Tibel, T.D. Sullivan, *IEEE Int. Reliab. Phys. Symp. Proc.* (2001) 194-199.
- [9] M. Hauschildt, M. Gall, R. Hernandez, *J. Appl. Phys.* 108 1 (2010) 013523-013523-10.
- [10] C. Chappaz, P. Nakkala, *IEEE Int. Reliab. Phys. Symp. Proc.* (2010) 887-889.
- [11] S.C. Lee, A. Oates, *IEEE Int. Reliab. Phys. Symp. Proc.* (2010) 107-114.