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► **To cite this version:**

Xavier Fonteneau, Florent Morel, Cyril Buttay, Hervé Morel, Philippe Lahaye. Predicting Static Losses in an Inverter-Leg built with SiC Normally-Off JFETs and SiC diodes. APEC, Mar 2013, Long Beach, CA, United States. pp.2636-2642, 10.1109/APEC.2013.6520668 . hal-00829353

**HAL Id: hal-00829353**

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Submitted on 3 Jun 2013

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# Predicting Static Losses in an Inverter-Leg built with SiC Normally-Off JFETs and SiC diodes

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**Abstract**—Predicting static losses in switches is an essential step to design a converter. This document details the methodology of a method to calculate static losses in an inverter leg built with SiC Normally-Off JFETs and diodes. Different parameters such as the temperature, the load current and the modulation ratio... are taken into account. As the JFETs can be used in reverse conduction, two strategies (using or not this capability) are described and compared. The devices are characterized and modelled, then analytical calculations are used to compute the static losses in each component. As the behaviour of the components depends on the temperature, an iterative program is used to determine the steady-state temperature of the junctions and the static losses. A good agreement is demonstrated between measurements and the proposed model with a constant current. The proposed method is applied to a three phase inverter to evaluate the benefit of using SiC devices instead of a Si power module.

## I. INTRODUCTION

Nowadays, the use of wide band-gap materials such as silicon carbide is subject of intense research in power electronics. Indeed, their characteristics allow operation at higher temperatures, higher voltages or with reduced switching times [1]. These studies have led to market SiC diodes at the beginning of the 21st century. Recently, SiC controlled switches have been released, mainly as "Normally-On" Junction Field Effect Transistors (JFETs). This "Normally-On" characteristic, which means that the device conducts current when no bias voltage is applied on the gate, is a main difference with the switches classically used in power electronics. As a result, "Normally-On" devices are not completely accepted in the industry.

Since 2009, Semisouth's Laboratory has been producing SiC JFETs whose particularity is to be "Normally-Off", which means they do not conduct in the absence of gate bias voltage. However, contrary to the "Normally-On" JFETs from Infineon, these components do not have any body diodes [2]. To develop an inverter leg, external SiC diodes should be added in parallel of the JFETs (Fig. 1).

The channel of a JFET can conduct both positive and negative drain currents [3]–[6]. Therefore, compared to Si IGBTs different strategies (using or not reverse conduction) can be used to control an inverter leg. These strategies influence the static losses, so the classic methods used to

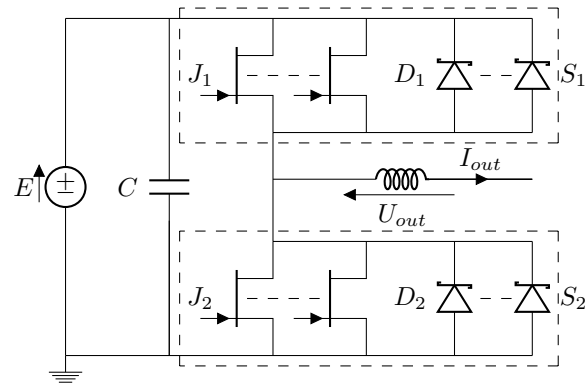


Fig. 1. Schematic of one inverter leg with several dies in parallel

predict the losses for converters built with IGBTs [7]–[9] can not always be used with SiC JFETs. Yet, this calculation is essential to determine if several dies should be used in parallel to meet the power specifications of the converter. Indeed, for many applications, the rated current of the dies (JFETs and diodes) is not large enough.

The goal of this study is to evaluate the advantages and drawbacks of using SiC JFETs in converters operated at room temperature. Expected advantages are reduced losses and increased switching frequency. As we are not considering here operation over an extended temperature range, the JFETs and the diode are not tested at more than than 150°C. This makes it possible to use standard (plastic) packaging. The considered SiC devices are Schottky diodes SDP30S120 [10] and JFETs SJEP120R063 [11] manufactured by Semisouth Laboratories.

In section II, we present the characterization and the modelling (according to the temperature) of the SiC components in order to calculate their static losses in a converter. Section III details the possible strategies and the resulting calculations of static losses. Then an iterative method to calculate both the static losses and the junction temperatures of JFETs and diodes is detailed in section IV. To validate the model of the SiC devices, a SiC switch built with four JFETs and a diode is tested in direct and reverse conduction with a DC current

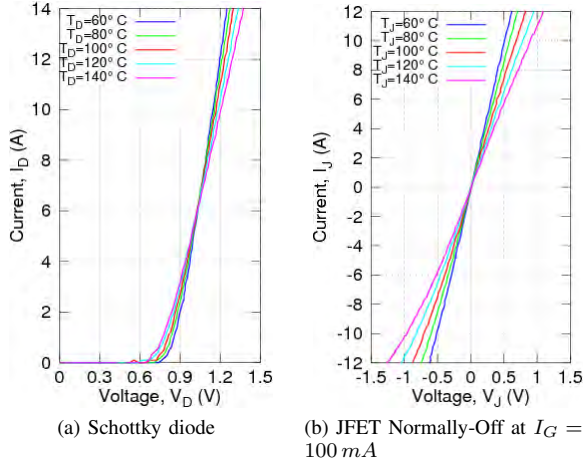


Fig. 2. Static characterization of one sample of each considered device

in section V. In section VI, the proposed method is used on an existing three phase inverter to estimate the advantages and drawbacks of using SiC devices instead of Si power module. Finally, conclusion and perspectives are given in section VII.

## II. CHARACTERIZATION AND MODELLING OF SiC COMPONENTS

According to the datasheets of the diode and the JFETs, the temperature influences their static losses. However, the data provided by Semisouth are not detailed enough to define accurate models. Therefore, we had to experimentally record the static characteristic of several samples of diodes and JFETs for different temperatures.

A TEK 371A curve tracer from Tektronix is used to measure the static characteristic of the devices. Their temperature is controlled by a thermal conditioner (Thermonics T-2500E).

Although, the Drain-to-Source resistance of the JFETs decreases with increases gate-to-source bias voltage. It has been proved that an excessive gate-to-source voltage generates extra static gate losses without reducing the on-state resistance of the JFET [12]. This remark is especially true when reverse conduction is used [13]. For this reason, the JFETs are controlled with a gate current regulated to  $I_G = 100 \text{ mA}$ . This limits  $V_{GS}$  to a sensible value. Fig. 2 shows the static behaviour of one sample of each SiC component.

For each sample and temperature, an optimization script is used to minimize the error between measurements and simple models. The optimization parameters are  $V_0$  (diode threshold voltage),  $R_D$  (diode series resistance) and  $R_J$  (drain to source JFET equivalent resistance).

- For the diodes, if  $V_D \geq V_0$ 
  - then  $I_D = \frac{V_D - V_0}{R_D}$
  - else  $I_D = 0$ .
- For JFETs  $I_J = \frac{V_J}{R_J}$ .

As this optimisation is performed for each temperature, it is possible to plot the evolution of each electrical parameter

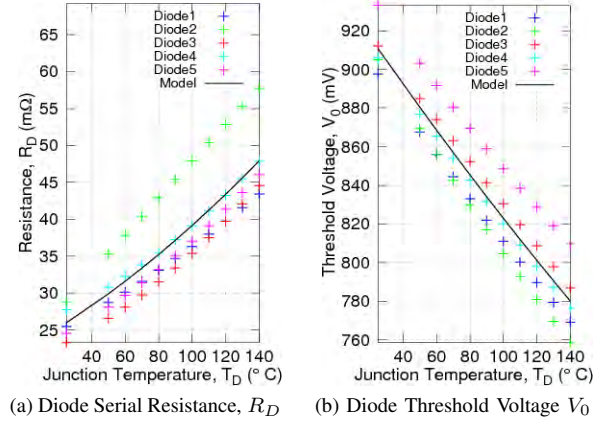


Fig. 3. Impact of the temperature on the parameters of the SiC diode Schottky electrical model

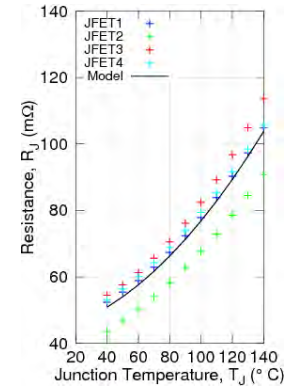


Fig. 4. Impact of the temperature on the parameters of the SiC JFET electrical model

of the model ( $V_0$  and  $R_D$  for diodes,  $R_J$  for JFETs) as a function of the junction temperature ( $T_D, T_J$ ). For each tested component, a model is established by using a second order polynomial function of the temperature. The final model parameters are calculated by averaging each coefficient issued from the sample set. Fig. 3 & Fig. 4 show the impact of the junction temperature on the calculated parameters for each sample and the obtained model.

For two JFETs with different characteristics ( $R_J(T_J)$ ) in parallel, the losses and the junction temperatures of each devices are different. However, the positive temperature coefficient of the characteristic of the JFETs tends to balance the resistances. It can be supposed that the accuracy of the model increases when several JFETs are used in parallel.

## III. STATIC LOSSES IN A SiC INVERTER LEG

In this section, the operation of an inverter leg is explained in order to establish a model of static losses. The model takes into account the number of dies in parallel, their junction temperatures (like in [14], [15]), the modulation index, the output current amplitude and the power factor of the load.

The considered hypotheses are as follows:

- The output current is sinusoidal:  $I_{out} = I \cdot \sqrt{2} \cdot \sin \theta$ .
- Each switch is composed by  $N_j$  JFETs in parallel and  $N_d$  anti-parallel diodes. For the sake of clarity, only one JFET and diode will be considered in the theoretical development below.
- The duration when the JFET  $J_1$  conducts, divided by the switching period, is  $\frac{1}{2}(1 + M \sin(\theta - \varphi))$  where  $M$  is the modulation ratio and  $\varphi$  is the angle between the current  $I_{out}$  and the fundamental frequency of the voltage  $U_{out}$ .

The study is done for a positive output current  $I_{out} > 0$  i.e.  $\theta \in [0; \pi]$ . When  $I_{out}$  is negative, results are simply obtained by swapping  $J_1$  and  $J_2$  and diode  $D_2$ .

#### A. $S_1$ is ON

When  $J_1$  is ON and the load current is positive,  $I_{out}$  flows through the JFETs referred as  $J_1$  (Fig. 5a).

The mean power during a period of the current is given by eq. 1.

$$P_{S_1} = \frac{N_j}{2\pi} \int_0^\pi \frac{(1 + M \sin(\theta - \varphi))}{2} \cdot R_J(T_J) \cdot \left( \frac{I_{out}(\theta)}{N_j} \right)^2 \cdot d\theta \quad (1)$$

#### B. $J_1$ is OFF

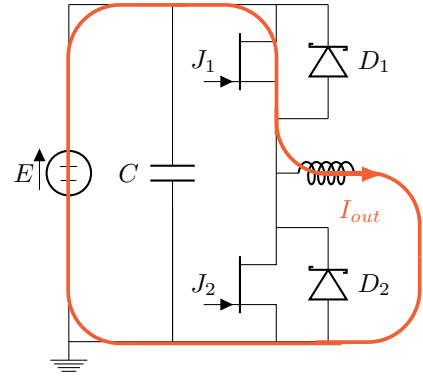
When  $J_1$  is OFF and the load current is positive,  $I_{out}$  flows through  $S_2$ . Two strategies are possible.

1)  $J_2$  is OFF (Fig. 5b): The current flows through the diodes  $D_2$  [16]. The static losses during a period of the current are given by eq. 2.

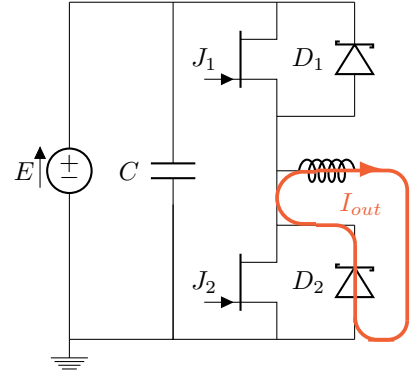
$$P_{S_2} = \frac{N_d}{2\pi} \int_0^\pi \frac{(1 - M \sin(\theta - \varphi))}{2} \cdot V_0(T_d) \cdot \left( \frac{I_{out}(\theta)}{N_d} \right) \cdot d\theta + \frac{N_d}{2\pi} \int_0^\pi \frac{(1 - M \sin(\theta - \varphi))}{2} \cdot R_d(T_d) \cdot \left( \frac{I_{out}(\theta)}{N_d} \right)^2 \cdot d\theta \quad (2)$$

2)  $J_2$  is ON (Fig. 5c): For a low load current level, it can be supposed that the current flows through the JFETs  $J_2$  only. If the current is large, the voltage across the switch  $S_2$  exceed the threshold voltage of the diodes and the load current is divided between the JFETs and the diodes. The calculation of the static loss is therefore more complex (eq. 3 with  $\theta_1$  equal to  $\frac{R_J(T_J)}{N_j} \cdot I \cdot \sqrt{2} \cdot \sin(\theta_1) = V_0(T_D)$ ).

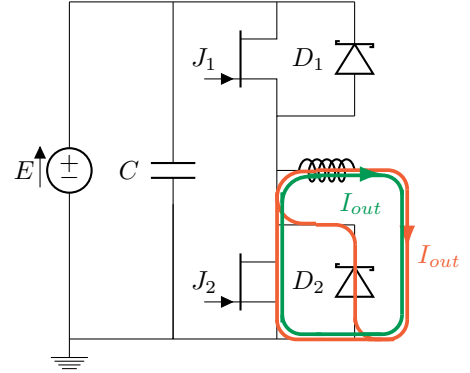
$$P_{S_2} = \frac{N_j}{\pi} \int_0^{\theta_1} \frac{(1 - M \sin(\theta - \varphi))}{2} \cdot R_j(T_j) \cdot \left( \frac{I_{out}(\theta)}{N_j} \right)^2 \cdot d\theta + \frac{N_j}{2\pi} \int_{\theta_1}^{\pi - \theta_1} \frac{(1 - M \sin(\theta - \varphi))}{2} \cdot R_j(T_j) \cdot I_j(\theta)^2 \cdot d\theta + \frac{N_d}{2\pi} \int_{\theta_1}^{\pi - \theta_1} \frac{(1 - M \sin(\theta - \varphi))}{2} \cdot R_d(T_d) \cdot I_d(\theta)^2 \cdot d\theta + \frac{N_d}{2\pi} \int_{\theta_1}^{\pi - \theta_1} \frac{(1 - M \sin(\theta - \varphi))}{2} \cdot V_0(T_d) \cdot I_d(\theta) \cdot d\theta \quad (3)$$



(a)  $J_1$  ON &  $J_2$  OFF



(b)  $J_1$  OFF &  $J_2$  OFF



(c)  $J_1$  OFF &  $J_2$  ON

Fig. 5. Current path inside the inverter leg for different control strategy and a positive  $I_{out}$

With:

$$I_J(\theta) = -\frac{N_d \cdot V_0(T_d) + R_D(T_d) \cdot I_{OUT}(\theta)}{N_d \cdot R_J(T_j) + N_j \cdot R_D(T_d)}$$

$$I_D(\theta) = \frac{-N_j \cdot V_0(T_d) + R_J(T_j) \cdot I_{OUT}(\theta)}{N_d \cdot R_J(T_j) + N_j \cdot R_D(T_d)}$$

#### IV. ITERATIVE COMPUTATION OF STATIC LOSSES AND TEMPERATURE OF JUNCTIONS

For a given load current, the static losses evolve with the junction temperature and the junction temperature evolves with losses (and with the room temperature, the thermal resistance...). Therefore, static losses and junction temperatures

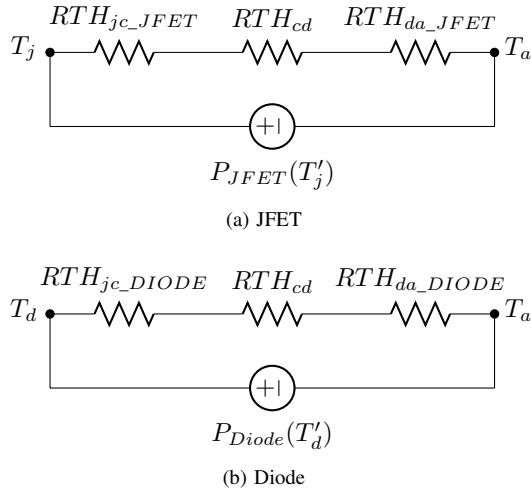


Fig. 6. Thermal circuit of SiC devices

must be calculated simultaneously [14]. Fig. 6 shows the thermal equivalent circuit for each device with:

$RTH_{jc\_JFET}$ : Thermal resistance between the junction and the case of a JFET [ $^{\circ}C/W$ ].

$RTH_{jc\_DIODE}$ : Thermal resistance between the junction and the case of a diode [ $^{\circ}C/W$ ].

$RTH_{da\_JFET}$ : Thermal resistance of the heat sink for a JFET [ $^{\circ}C/W$ ].

$RTH_{da\_DIODE}$ : Thermal resistance of the heat sink for a diode [ $^{\circ}C/W$ ].

$RTH_{cd}$ : Thermal resistance of a Sil Pad [ $^{\circ}C/W$ ].

$P_{JFET}(T_j)$ : Total losses inside a JFET for a complete period of the output current  $I_{out}$  [W].

$P_{DIODE}(T_d)$ : Total losses inside a diode for a complete period of the output current  $I_{out}$  [W].

$T_a$ : Maximal ambient temperature [ $^{\circ}C$ ].

$T_j$ : Junction temperature of a JFET [ $^{\circ}C$ ].

$T_d$ : Junction temperature of a diode [ $^{\circ}C$ ].

In this paper an iterative method is proposed (Fig. 7).

- 0) The junction temperature of the dies is considered to be equal to the room temperature.
- 1) The electrical parameters of diodes ( $R_D$ ,  $V_0$ ) and JFETs ( $R_J$ ) are calculated for the current junction temperature (see model Fig. 3 and Fig. 4).
- 2) The losses are calculated for each component (the static losses: eq. 1 and eq. 2 or 3 and the switching losses<sup>1</sup>).
- 3) With the thermal resistance between junction and the surrounding air, the junction temperatures ( $T_{J_f}$ ,  $T_{D_f}$ ) of JFETs and diodes are calculated.
- 4) If the difference between final and initial temperatures

<sup>1</sup>As a simple evaluation by using the datasheet provided by Semisouth, the total energy losses ( $E_{TS}$ ) during one switching period are extrapolated by a polynomial function depending on the value of the switched current for the JFETs and the blocking voltage for the diode. At the end, an estimation of the switching losses is possible for a fixed switching frequency.

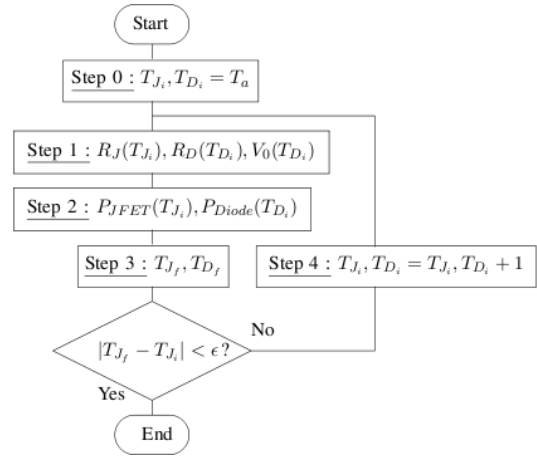


Fig. 7. Schematic of the program to determine the losses and the junction temperature of each SiC devices

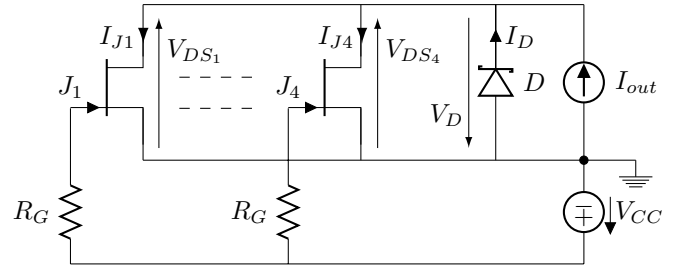


Fig. 8. SiC switch built with four JFETs and a single Schottky diode tested in forward and reverse conduction with  $R_G = 270 \Omega$  and  $V_{CC} = 30 V$ .

is lower than a given threshold ( $\epsilon$ ), it can be considered that the operating point is reached, else a new iteration is performed (step 1). Other tests are performed to ensure that the algorithm converges.

## V. SiC SWITCH TESTED WITH A DC LOAD CURRENT

To validate the model of the losses developed in section III, a SiC switch built with four JFETs in parallel and one diode is tested for a constant current  $I_{out}$  ranging from -55 A to 50 A. Fig. 8 shows the electrical circuit used to test the SiC switch. To reduce thermal coupling, each device was mounted on an individual heatsink ( $RTH_{ca} = 5.9^{\circ}C/W$ ). Then, thermal paste (Thermal Interface) is used to improve the contact between components and heatsinks ( $RTH_{TIM} = 0.1^{\circ}C/W$ ). The temperature ( $T_{JFET1-4}$ ,  $T_{DIODE}$ ) of the case and the voltage ( $V_{DS1-4}$ ,  $V_{DIODE}$ ) across each component are monitored by a precision multimeter from Keithley (2700 Data Acquisition System). K thermocouples are used and located between the heatsink and the back side of components. A current Probe (TCP0030) and an oscilloscope (DPO7104) from Tektronix are used to record the current inside the JFETs and the diode. The "measured losses" are calculated by multiplying the values of the current  $I_J$  and the voltage  $V_{DS}$

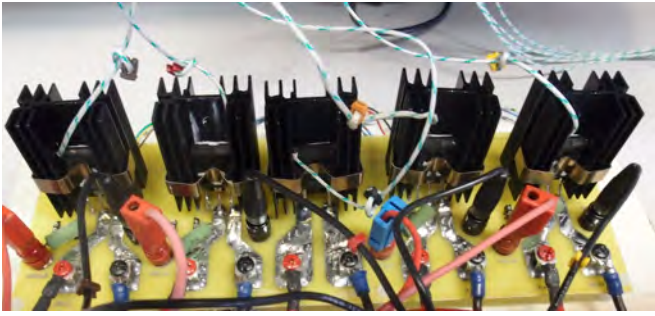


Fig. 9. View of the test set up

for the JFET and  $I_D$  and  $V_D$  for the diode. Each JFET is controlled with a gate current  $I_{G_{1-4}} = \frac{30-2.6}{270} \approx 100 \text{ mA}$ .

#### A. Current inside the JFETs and the diode

Fig. 10 shows the distribution of the current  $I_{out}$  inside the JFETs and the diode.

In a direct conduction of the SiC switch, the current flows through the JFETs only. The current inside each JFET is well distributed, indeed, the maximal current scattering is roughly 1 A at  $I_{out} = 50 \text{ A}$ . The measured temperature of the JFETs is close to  $120^\circ\text{C}$ . However, the calculated junction temperature is higher than the maximal operating temperature advised by the manufacturer ( $T_{limit} = 150^\circ\text{C}$ ) and the model considers that the device is outside of its safe operations area. This result is due to the misjudgment of the thermal resistance  $R_{TH_{jc}}$ ,  $R_{TH_{TIM}}$  and  $R_{TH_{ca}}$ .

In a reverse conduction and for a low level of the load current, the current flows entirely through the JFETs. When the voltage across the switch is large enough, the Schottky diode begins to conduct. The current is then distributed between the JFETs and the diode. The results shows that when the diode conducts, the current inside the JFETs seems to be stable at  $-10 \text{ A}$ . According to the measure, the model of the SiC switch fits well the measurements. However, the model of the diode doesn't match. Indeed, the diode begins to conduct for a load current roughly 4 A lower than expected. It can be supposed that the heat sink of the diode absorbs a part of the heat emit by the JFET (thermal convection and/or thermal radiance). This heat transfert is linked to the distance between the components and to the difference of the temperature of their heat sink. So, the diode temperature is higher than the calculated temperature, this error leads to a lower threshold voltage than expected and an anticipated conduction of the diode. We can consider that the thermal transfer do not influence the JFETs because their case temperature are approximately the same ( $\Delta T_{JFET_{1-4}} \approx 0$ ). For a load current of  $-50 \text{ A}$ , the temperature of the JFETs and diode dissipators are  $110^\circ\text{C}$  and  $90^\circ\text{C}$  respectively. Due to the conduction of the diode, the case temperatures of JFETs are lower in reverse than in direct conduction. When the current  $I_{out}$  decreases to  $-55 \text{ A}$ , the temperatures of JFETs are still below to the maximal operating temperature advised by the manufacturer.

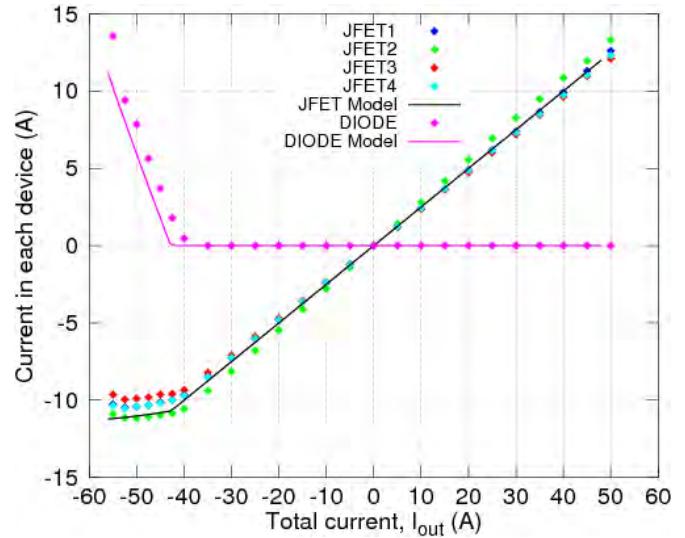


Fig. 10. Current distribution inside each components of the SiC Switch

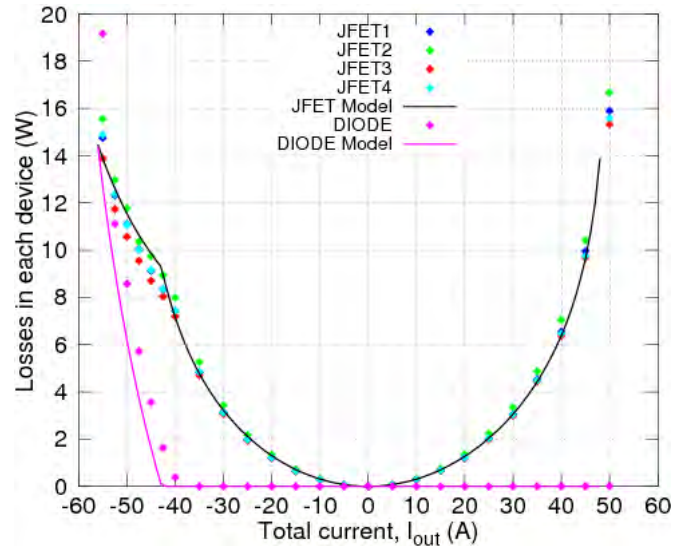


Fig. 11. Impact of the load current on the losses inside each components of the SiC Switch

#### B. Losses inside the JFETs and the diode

Fig. 11 presents the losses inside each component versus the value of the current  $I_{out}$ . In a direct conduction, it can be considered that the calculated losses fit the measured losses well. Indeed, a maximal scattering of  $0.5 \text{ W}$  is observed for a load current between 0 to 45 A. The maximal losses is roughly  $17 \text{ W}$  (JFET2) at  $I = 50 \text{ A}$ .

## VI. EXAMPLE OF USE OF THE PROPOSED METHOD

The proposed method has been tested on a three-phase inverter to evaluate the benefits of using SiC JFETs and Schottky diodes instead of Si-IGBTs. The reduction of the baseplate between a power module and discrete components



Electrical parameters	Value
E	450 VDC
$I_{MAX}$	$40\sqrt{2} A$
$U_{OUT}$	180 VRMS
f	12 kHz
$N_j$	4
$N_d$	1
$\cos \varphi$	0.85
$RTH_{cd}$	$0.3^\circ C/W$
$RTH_{jc\_JFET}$	$0.6^\circ C/W$
$RTH_{jc\_DIODE}$	$0.5^\circ C/W$
$RTH_{da}$	$0.05^\circ C/W$
$T_a$	$55^\circ C$
$S_{DIODE} = S_{JFET}$	$15 * 21mm^2$
$S_{module}$	$137 * 162mm^2$

Table I. Electrical characteristic used to compute the losses model.

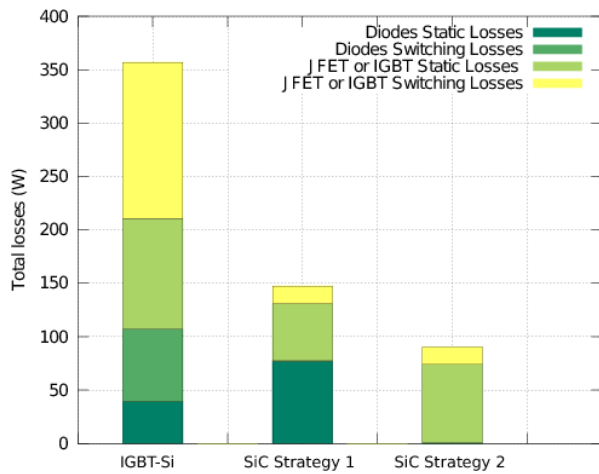


Fig. 12. Distribution of the calculated losses inside a Three Phase Inverter  $40 A_{RMS}$ .

increase the value of the thermal resistance to ambient, this one can be supposed inversely proportional to the ratio of the surface. Table I shows the electrical characteristics used as an input to compute the losses. For the IGBT power module, the data corresponds to a three-phase inverter from the range product Alectis market by ECA-EN. Figure 12 shows the losses inside a three-phase inverter with an output current of  $40 A_{RMS}$  with an IGBT power module and discrete SiC components for the two control strategies. The results show that using four JFETs and one schottky diode for each switch leads to a massive reduction in losses compared to a power module using Si IGBT and diodes.

Furthermore, the strategy described in section III-B2 leads to a slight increase of power losses in the JFETs balanced by a dramatic reduction for the diode as compared to the strategy in section III-B1. Overall, the total losses are reduced. Moreover, the junction temperatures of JFETs are

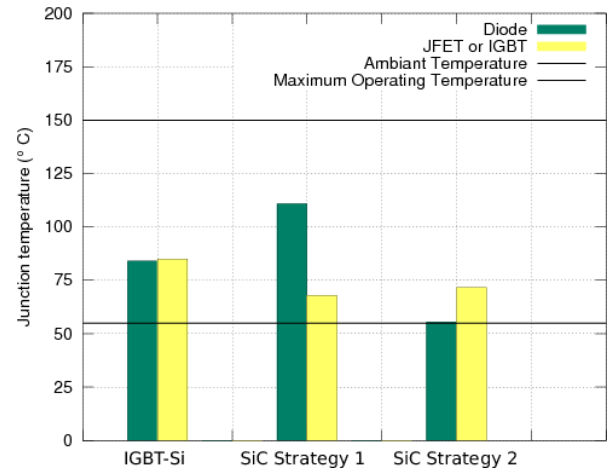


Fig. 13. Distribution of the calculated temperatures inside a Three Phase Inverter  $40 A_{RMS}$ .

a little higher for the strategy III-B1 than the strategy III-B2.

For the SiC devices, static losses represents the main part of the total losses, approximately 90% for the first strategy and 80% for the second strategy.

Figure 14 shows the impact of the switching frequency on the total losses for the different technologies and the two strategies for a  $40 A_{RMS}$  load current.

For a switching frequency equal to 50 kHz, the losses inside a SiC converter are lower than a Si converter at 12 kHz. A reduction from 38% to 58% is expected for both strategies presented in sections III-B1 & III-B2 compared with the initial losses in a Si converter despite the increase in the switching frequency. Moreover, the junction temperature reached by the diode with the first strategy is high ( $T_D \approx 120^\circ C$ ). Then, it is suitable to use the reverse conduction of the JFETs to decrease the thermal stress on the diode.

## VII. CONCLUSION

A novel method to predict power losses in a SiC leg inverter has been developed. It allows to predict power losses and junction temperatures in a switch composed by  $N_j$  JFETs and  $N_d$  diodes in parallel. Results show that a huge reduction of power losses is possible when SiC is used instead of Si in an inverter. This opens new perspectives in power electronics such as a reduction of heating or an increase in switching frequency... Moreover, it was shown that using JFETs in reverse conduction in parallel with diodes leads to a significant reduction in static losses while the increase in junction temperature is low.

Further studies will be dedicated to better modelling of the switching losses and the thermal coupling.

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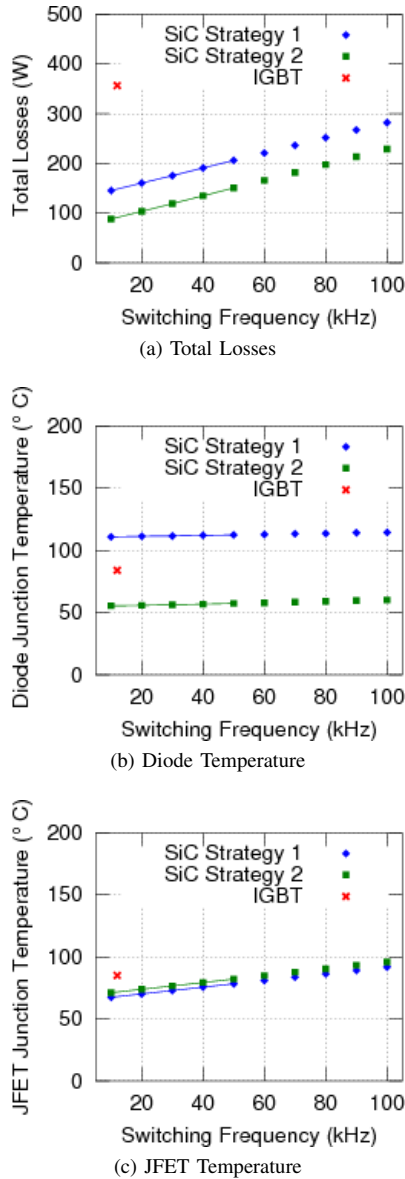


Fig. 14. Impact of the switching frequency on the total losses and the junction temperatures in a three phase inverter with a load current of  $40 A_{RMS}$

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