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## A converging route towards very high frequency, mechanically flexible, and performance stable integrated electronics

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The ability to realize flexible circuits integrating sensing, signal processing, and communicating capabilities is of central importance for the development of numerous nomadic applications requiring foldable, stretchable, and large area electronics. A key challenge is, however, to combine high electrical performance (i.e., millimeter wave, low noise electronics) with mechanical flexibility required for chip form adaptivity in addition to highly stable electrical performance upon deformation. Here, we describe a solution based on ultimate thinning and transfer onto a plastic foil of high frequency CMOS devices initially processed on conventional silicon-on-insulator wafers. We demonstrate a methodology relying on neutral plane engineering to provide high performance stability upon bending, by locating the active layer, i.e., the transistor channel, at the neutral fiber of the flexible system. Following this strategy, record frequency performance of flexible n-MOSFETs, featuring  $f_T/f_{MAX}$  of 120/145 GHz, is reported with relative variations limited to less than 5% even under aggressive bending on cylinders with curvature radii down to 12.5 mm. © 2013 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4801803>]

### I. INTRODUCTION

Mechanically flexible electronics is particularly well suited to the development of nomadic and space-weight-and-power (SWAP) constrained applications featuring ubiquitous intelligence and high frequency (HF) communication capabilities.<sup>1–4</sup> Over the last decade, the so-called field of macroelectronics<sup>5</sup> has led to numerous demonstrations involving thin, lightweight, and flexible devices. Nevertheless, one has to recognize that flexible electronics is today quasi-exclusively synonymous with organic<sup>6</sup> and high-throughput printing techniques,<sup>4</sup> whose major deficiencies lie in extremely poor carriers' mobility,<sup>6–8</sup> i.e.,  $\sim 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and coarse patterning resolution, i.e.,  $\sim 10 \mu\text{m}$  at best.<sup>9,10</sup> Low cost and large surface are, therefore, no advantage for certain application classes for which increased complexity and millimeter wave (mmW) performance are necessary.<sup>11,12</sup> To cope with the mobility roadblock associated to organic electronics, the transfer-bonding of thin layers of less disordered materials onto plastic substrates has been widely reported in the literature.<sup>13–20</sup> However, many technological realizations are based on a process sequence that involves the transfer of a bare active film onto a flexible plastic handler.<sup>14,15,21</sup> According to this approach, transistors must be subsequently structured using sufficiently gentle process steps and thermal budgets compatible with the flexible substrate.<sup>18</sup> This strategy is, therefore, not capable to offer deeply scaled transistors in the decanometer range with minimal parasitic resistance and capacitance. As a consequence, frequency performance is limited well below 10 GHz.<sup>15,22</sup>

Dissociating the fabrication of transistors and circuits from the transfer-bonding step onto a plastic foil introduces considerable flexibility without suffering from the above-mentioned limitations. Starting from standard CMOS technologies, methods based on extreme thinning of the initial substrate and subsequent bonding of circuit dies on plastic films have resulted in mechanically flexible transistors reaching the 100 GHz frequency range.<sup>23–25</sup> This strategy hereafter referred to as ultimate thinning and transfer bonding of CMOS technology (UTTBM-CMOS) presents the distinctive advantage to benefit from most advanced technological generations without having to overcome inextricable process and material compatibility problems introduced by a plastic handler. Following this line, the highest unity-current-gain cutoff ( $f_T$ ) and maximum oscillation frequencies ( $f_{MAX}$ ) have been reported at 150/160 GHz for n-MOSFETs and 100/130 GHz for p-MOSFETs, respectively.<sup>25</sup> Additional measurements have also revealed that noise performance is preserved when passing from the initial rigid and thick silicon handler to a plastic substrate after thinning, resulting in 0.57 dB of minimal noise figure at 10 GHz with 17.8 dB of associated gain.<sup>26</sup> Beyond unrivaled performance over alternative methods, it is finally worth noting that the UTTBM-CMOS inherently embeds back-end of the line interconnect layers that give access to functional complexity.

In the aforementioned quoted publications,<sup>25,26</sup> it was demonstrated that the UTTBM scheme did not degrade transistors' properties in terms of high frequency and low noise operation in straight flat configuration. But apart from performance conservation, a question legitimately arises: how mechanical deformation can affect operation of complex

flexible electronic systems? In the perspective of synthesizing reliable functions with invariant characteristics, electrical properties independent of the strain type, direction, and intensity are, therefore, highly desirable. It is well known that the application of strain to a semiconductor breaks its symmetry leading to band splitting and warping.<sup>27–31</sup> As a result, carriers' transport properties can be significantly modulated depending on the strain direction and symmetry, in other words, as a function of the strain tensor structure. Over the last decade, this physical property has been widely used to enhance carriers mobility through uniaxial process-induced stress in the 90 nm CMOS technology node and beyond.<sup>32–34</sup> However, the situation considerably differs when flexible electronics is considered because one of its fundamental characteristics is that strain resulting from bending of UTTB chips is by essence random.

Here, we report on the fabrication and characterization of flexible UTTB-CMOS MOSFETs thinned down to 5.7  $\mu\text{m}$  and transferred onto a plastic foil. Using neutral plane engineering, we show that it is possible to accommodate aggressive bending configurations while maintaining a minimal strain level in the active channel of transistors. The thickness of the plastic substrate is selected to reduce the strain level developed in the silicon active layer under bending condition. This is performed by positioning the multilayer neutral plane close to the active layer. We unveil that MOSFETs DC and RF performance variations are lower than 5%, even for a curvature radius as small as 12.5 mm, as predicted by mechanical simulations.

## II. RESULTS

### A. UTTB-CMOS fabrication

The basic steps of the UTTB-CMOS processing scheme are presented in Figure 1(a) (see Appendix for details). The

methodology is similar to the one reported in previous work.<sup>25,26,35</sup> The process sequence starts from an industrially mature 65 nm partially depleted silicon-on-insulator (SOI) CMOS technology featuring back-end-of-line (BEOL) layers with six copper levels and one aluminum-cap.<sup>36</sup> The final multilayer system constituted of a thin flexible plastic handler, an adhesive layer, and the topmost part of the initial CMOS wafer comprising the buried oxide (BOX) up to the top metal layer of the interconnection BEOL stack, as shown by scanning electron microscopy (SEM) in Figure 1(b). It is worth noting that after bonding the temporary carrier, the entire process is conducted at low temperature ( $<50^\circ\text{C}$ ), ensuring compatibility with the maximum thermal budget acceptable by most commonly used plastic films. Low temperature processing also avoids the generation of thermal mismatch stress due to the difference in coefficients of thermal expansion between the inorganic (thinned CMOS wafer) and organic (plastic handler) layers. No degradation can be seen after thinning and transfer on plastic, using optical microscopy, SEM imaging of a cross-section, Figure 1(b), or TEM, Figure 1(c).

### B. Electrical properties' sensitivity to strain

In the following developments, the focus is put on the sensitivity of static and high frequency properties of flexible transistors under the application of external mechanical strain. As required from a system application perspective, the accent is placed on how to limit variations of electrical properties even in the case of aggressive bending. To this end, mechanical strain was applied to UTTB-CMOS dies by conforming them on cylinders of various radii, Figure 1(d), while static and high frequency characteristics were measured, as shown in Figure 1(e). To get a better insight into the

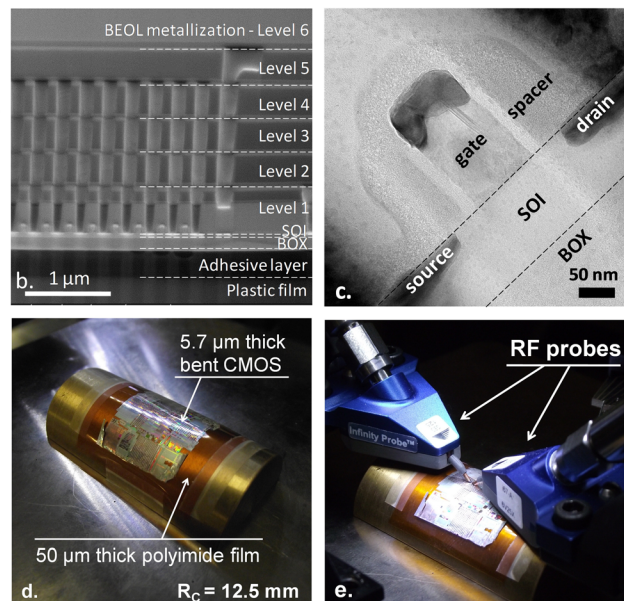
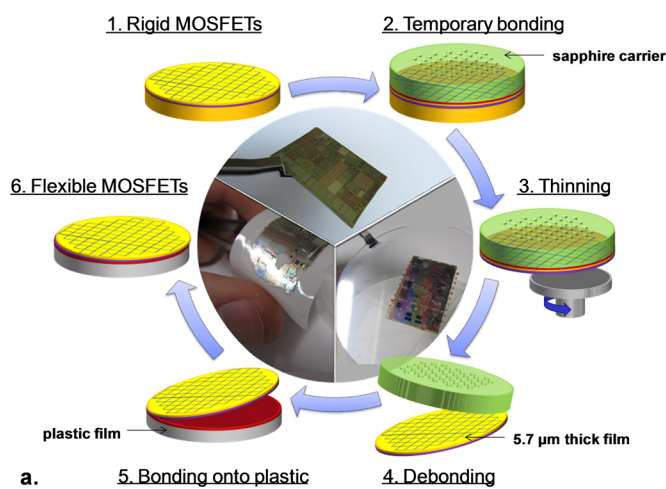


FIG. 1. UTTB-CMOS MOSFETs fabrication. (a) Schematic of MOSFETs thinning and transfer procedure onto an organic film (see Appendix for details). (b) SEM cross-section of a flexible UTTB-HF-MOSFET highlighting several gate fingers and the levels of interconnection. (c) TEM image of a single gate finger after transfer on plastic showing that no physical degradation of the transistor channel is observed. (d) 5.7  $\mu\text{m}$  thick UTTB-CMOS chip transferred onto a 50  $\mu\text{m}$  thick polyimide handler and under flexure on semi-cylinders with a 12.5 mm curvature radius. (e) Flexible UTTB-CMOS chip under HF probing in bent configuration.

measured variations of electrical performance, strain calculations were coupled to the silicon piezoresistivity tensor to evaluate the theoretical change in mobility. In this analysis, the position of the neutral plane, defined as the surface perpendicular to the cross-sectional plane where there is neither compression nor elongation, is a parameter of utmost importance, which determines strain distribution over the thickness of the multilayer stack. Following a simplified one-dimensional approach, its position from the bottom of the stack, referred to as  $\delta$  in Figure 2(b), can be formulated as a function of the thickness,  $t_i$ , Young's modulus,  $E_i$ , and centroidal axis position,  $z_i$ , of each layer<sup>21,29,37</sup> according to the following equation:

$$\delta = \frac{\sum_i z_i E_i t_i}{\sum_i E_i t_i} \quad (1)$$

This relation clearly indicates that the addition of a thin rigid inorganic film (here, the topmost layers of CMOS dies) on top of a thicker flexible—i.e., featuring a low Young's modulus—organic handler tends to move the neutral plane towards the interface, or even in the inorganic film. The principle is, therefore, to associate a thick soft material to an ultra-

thin stiff overlayer to locate the neutral plane close to their joining interface. Although UTTB-CMOS is a very complex system owing to the heterogeneity of the BEOL interconnection network, the aforementioned principle can be well illustrated and the related mechanics well captured by adopting a simple bilayer system. Figure 2(a) quantifies the position  $d$  of the neutral plane with respect to the interface normalized by the total thickness  $t_{TOT}$  (see the inset in Figure 2(b)) as a function of the thickness ratio  $t_{film}/t_{handler}$ . This functional dependence of  $d/t_{TOT}$  versus  $t_{film}/t_{handler}$  is parametrized by the Young's moduli ratio  $E_{film}/E_{handler}$  of both materials. This graph emphasizes the fact that the neutral plane of the multilayer can be positioned at, or close to the interface ( $d=0$ ), or at any position that may be relevant<sup>38–40</sup> by a proper selection of materials' stiffness and thickness. From this analysis, it naturally ensues that the neutral plane of the UTTB-CMOS system must be adjusted as close as possible to the active layer where electron transport takes place to minimize the impact of bending on transistors' performance.

For the 65 nm SOI-CMOS technology considered in this work, the active layer is the 60 nm thick SOI film. It is only separated from the plastic handler by the BOX layer (145 nm) and the adhesive layer (~500 nm). In a more realistic

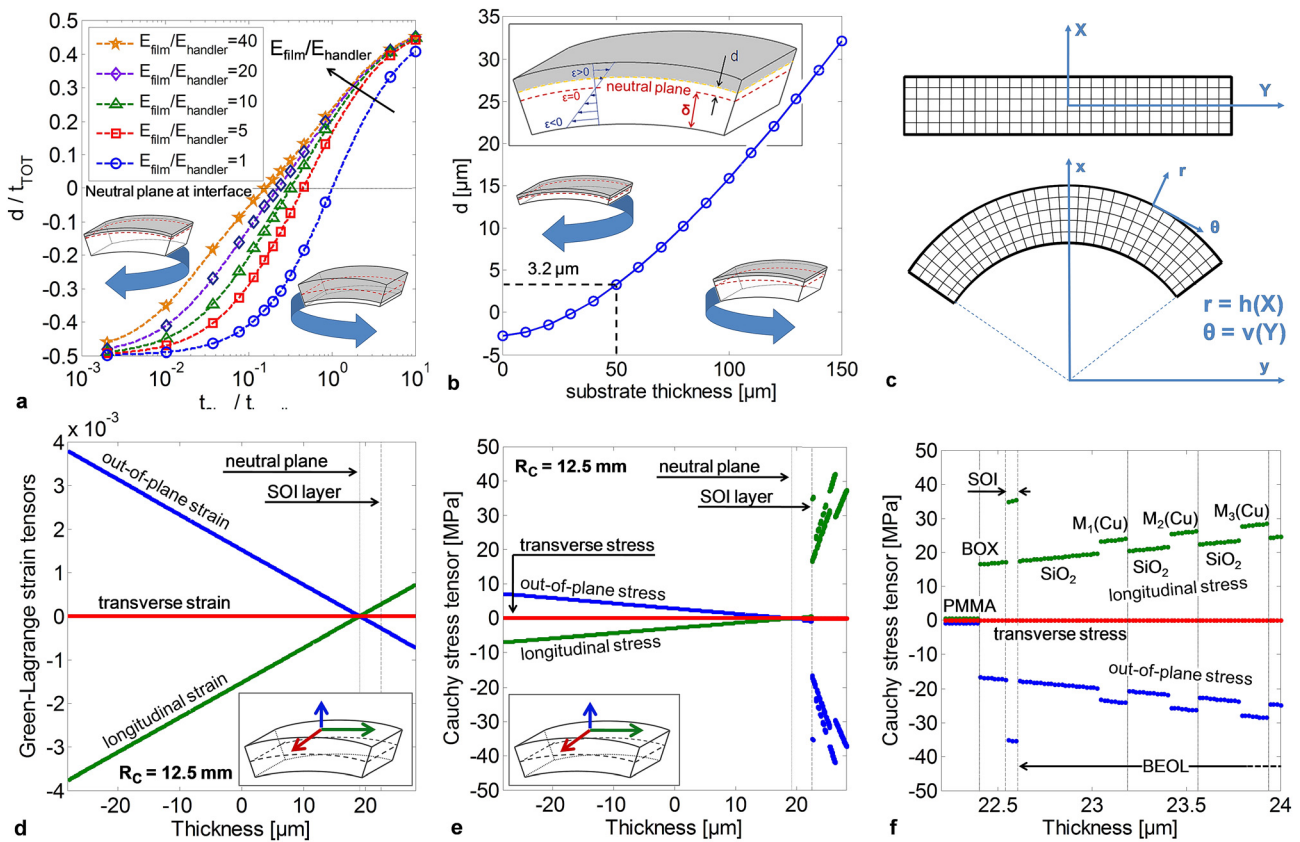


FIG. 2. Mechanical considerations. (a) Neutral plane location dependence on thickness and Young's modulus of a bilayer represented by plotting the interface to neutral plane distance  $d$  over total thickness  $t_{TOT}$  versus the thicknesses ratio  $t_{film}/t_{handler}$  for various Young's moduli ratios  $E_{film}/E_{handler}$ . (b) Dependence of the neutral plane to active layer distance  $d$  on the plastic handler thickness when considering the UTTB-CMOS stack. Inset: Schematic of the sample under flexure where the UTTB-CMOS multilayer is represented in grey (the neutral plane is defined in red dashed line and longitudinal strain is represented by blue arrows). (c) Initial (top) and deformed (bottom) mesh of the modeled UTTB-CMOS sample on its plastic handler highlighting the correspondence between initial and deformed coordinates. (d) Green-Lagrange strain tensor components. (e) Cauchy stress tensor components simulated at various positions along the thickness of the multilayer stack for a UTTB-CMOS sample bent over a cylinder with a 12.5 mm curvature radius. In the latter two graphs, the neutral plane and active SOI layer are highlighted in dotted and dashed lines, respectively. (f) Zoom-in of Figure 2(e) in the front end and first layers of BEOL of the bent UTTB-CMOS stack.

description of the UTTB-CMOS stack, 17 uniform layers of various thicknesses and Young's moduli have been taken into account for an accurate treatment of the mechanical problem. Using a  $50\ \mu\text{m}$  thick polyimide handler in the UTTB-CMOS process, Figure 2(b) shows that the distance between the neutral plane and the SOI layer is reduced to approximately  $3\ \mu\text{m}$ . After the determination of the neutral plane position, strain and stress distributions across the UTTB-CMOS multilayer stack can be calculated according to continuum mechanics considerations. The cylindrical bending of a thin plate transforms horizontal material planes into concentric tubes, i.e.,  $r = h(X)$ , and vertical planes into radial ones, i.e.,  $\theta = v(Y)$ , as reported in Figure 2(c). Figures 2(d)–2(f) show the three diagonal components of the Green-Lagrange strain and Cauchy stress tensors (see Appendix for details) across the thickness of the multilayer stack after bending over a cylinder featuring a  $12.5\ \text{mm}$  curvature radius. On these graphs, the positions of the neutral plane and active SOI layer are highlighted with black dotted and dashed lines, respectively. For electrical considerations, the strain and stress developed in the SOI active layer have to be taken into account. It can be observed in Figure 2(d) that the longitudinal (defined as the direction parallel to the electronic transport) component of strain in the electrically active SOI layer is  $0.03\%$ . For the same curvature radius of  $12.5\ \text{mm}$ , the associated longitudinal stress component amounts to  $36\ \text{MPa}$ , Figure 2(e). A more accurate insight is provided by Figure 2(f) that provides a zoom of the three components of stress in the front end and first layers of BEOL under bending. From the determination of the stress distribution in the SOI layer, the variation of electron mobility can be thoroughly calculated using the piezoresistance coefficients of crystalline silicon.<sup>27,28</sup> This leads to a modest longitudinal electron mobility increase of  $+1.2\%$ , and  $+2.4\%$  for cylinders with a  $25\ \text{mm}$  and  $12.5\ \text{mm}$  curvature radius, respectively. Assuming that the drain current  $I_{\text{DS}}$  is

proportional to the electron mobility both in low and high field regimes,<sup>31</sup> it is expected that the DC transconductance  $g_{\text{m}}$ , the unity gain cut-off frequency  $f_{\text{T}}$ , and the maximum oscillation frequency  $f_{\text{MAX}}$  will follow the same variation trend.

### C. DC characterization of strained UTTB n-MOSFETs

DC and HF measurements have been performed on a minimum set of four transistors to obtain statistically representative results. Electrical characteristics presented in this letter focus on  $60\ \text{nm}$  and  $65\ \text{nm}$  gate long n-MOSFETs featuring a total gate width development of  $64\ \mu\text{m}$  coming from the parallel association of  $0.5$ ,  $1$ , or  $2\ \mu\text{m}$  wide unitary gates. Static characteristics presented in Figs. 3(a) and 3(b) show  $I_{\text{DS}}-V_{\text{DS}}$ ,  $I_{\text{DS}}-V_{\text{GS}}$  current-voltage, and static transconductance  $g_{\text{mDC}}$  characteristics measured on a UTTB transistor (featuring a gate length of  $65\ \text{nm}$ , a unitary gate finger width of  $2\ \mu\text{m}$ , and a total width of  $64\ \mu\text{m}$ ) both on flat and bent configurations. Very little discrepancy between DC characteristics measured in flat and bent configurations can be noticed from these two graphics, where measurements performed in flat configuration are represented by solid blue lines, whereas characteristics of bent MOSFETs on cylinders with a  $25\ \text{mm}$  and  $12.5\ \text{mm}$  curvature radius are drawn in green dashed and red dotted lines, respectively. The relative variations of  $I_{\text{DS}}-V_{\text{DS}}$  characteristics between the bent and flat configurations are quantified in Figure 3(c). Variations after bending the UTTB transistor on a cylinder with a  $25\ \text{mm}$  (resp.  $12.5\ \text{mm}$ ) curvature radius are plotted in green dashed lines (resp. red dotted lines). Note that the special bias condition corresponding to  $V_{\text{DS}} = 1.2\ \text{V}$  and  $V_{\text{GS}} = 0.8\ \text{V}$  is highlighted in Figure 3(c) as it corresponds to the maximum of static transconductance where HF figure-of-merits, namely the unity current gain  $f_{\text{T}}$  and Mason's gain cut-off frequencies  $f_{\text{MAX}}$ , are measured.

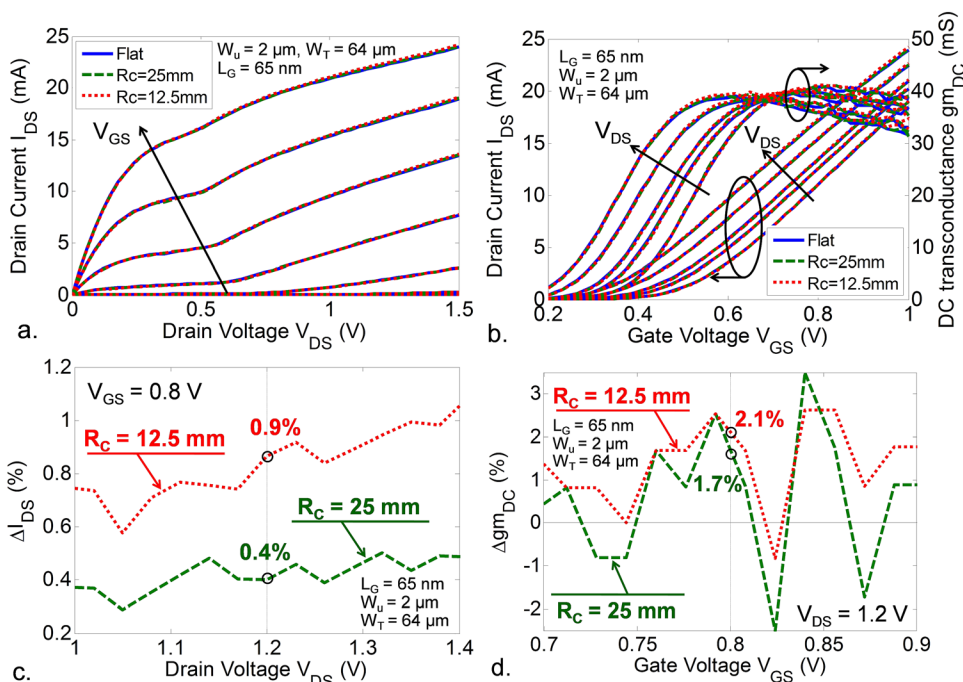


FIG. 3. DC characteristics of UTTB n-MOSFETs under flexure. (a) Current-voltage  $I_{\text{DS}}-V_{\text{DS}}$  characteristics, (b) current-voltage  $I_{\text{DS}}-V_{\text{GS}}$  and static transconductance  $g_{\text{mDC}}$ , measured flatwise (blue lines), under flexure on semi-cylinders with a  $25\ \text{mm}$  curvature radius (green dashed lines) and a  $12.5\ \text{mm}$  curvature radius (red dotted lines). (c) Relative variations of drain current  $I_{\text{DS}}$  versus  $V_{\text{DS}}$  and (d) relative variations of DC transconductance  $g_{\text{mDC}}$  versus  $V_{\text{GS}}$  after transistor bending on  $12.5$  and  $25\ \text{mm}$  radius cylinder. In the latter two graphs,  $V_{\text{DS}} = 1.2\ \text{V}$  and  $V_{\text{GS}} = 0.8\ \text{V}$  correspond to static bias conditions used to perform and extract HF figures-of-merit. The considered n-MOSFET transistor features 32 parallel gate fingers of length  $L_{\text{G}} = 65\ \text{nm}$  and unitary gate width  $W_{\text{u}} = 2\ \mu\text{m}$  leading to a total gate width development  $W_{\text{T}} = 64\ \mu\text{m}$ .

### D. HF characterization of strained UTTB n-MOSFETs

In order to extract the intrinsic HF properties of measured devices, an “OPEN” deembedding procedure has classically been applied to eliminate contributions of transistor accesses. This methodology is based on the S parameters’ (or admittance parameters Y) measurement of both the active transistor  $Y_{TOT}$  (including contact accesses, Figure 4(a)) and a passive open structure  $Y_{OPEN}$  featuring similar accesses that the HF

transistor. The “OPEN” structure can be characterized by the two open capacitances  $C_{OPEN,1}$  and  $C_{OPEN,2}$  presented in Figure 4(b) (see Appendix for details). The equivalent circuit of the HF transistor including contact accesses is drawn in the inset in Figure 4(b). The intrinsic transistor S parameters, Figure 4(c), are subsequently obtained by subtracting  $Y_{OPEN}$  to  $Y_{TOT}$ . Measured S parameters of UTTB HF transistors whose DC characteristics were discussed previously are shown in Figure 4(a) before deembedding, and in Figure 4(c)

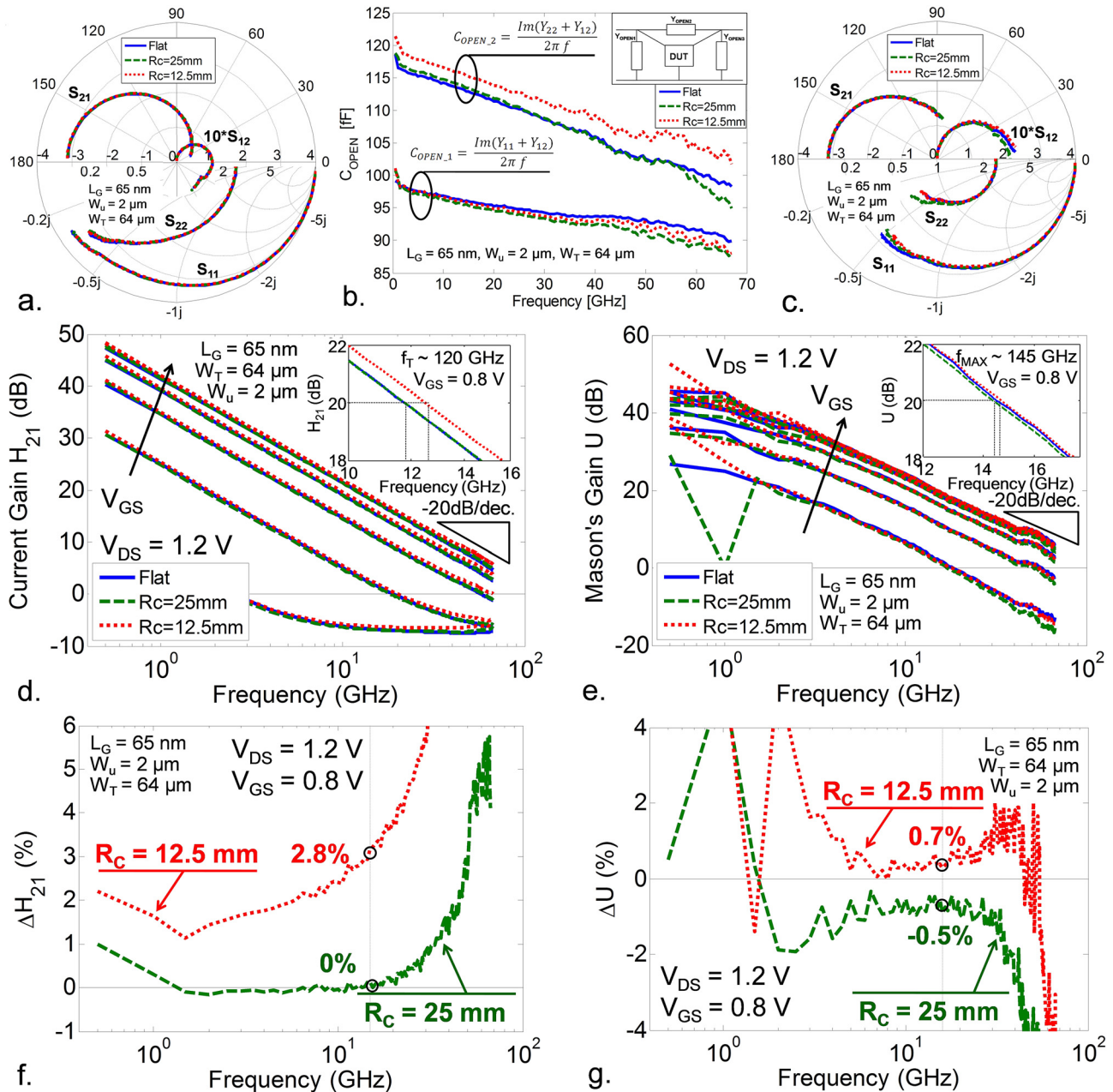


FIG. 4. HF characteristics of UTTB n-MOSFETs under flexure. (a) S parameters including extrinsic accesses measured on a HF transistor featuring 32 parallel gate fingers of length  $L_G = 65$  nm and unitary width  $W_u = 2$   $\mu$ m leading to a total gate development  $W_T = 64$   $\mu$ m, (b) open capacitances  $C_{OPEN,1}$  and  $C_{OPEN,2}$  characterizing extrinsic contributions using the “OPEN” methodology, measured flatwise, and under flexure, (c) deembedded S parameters measured on the same HF transistor, (d) unity gain  $H_{21}$ , and (e) Mason’s gain  $U$ , measured flatwise, and under flexure (same line colors as previously); both figures demonstrate good agreement between measurements and the theoretical  $-20$  dB/dec slope. (f) Relative variations of unity gain  $H_{21}$  and (g) Mason’s gain  $U$  versus frequency after transistor bending on 25 and 12.5 mm radius curvature. In the latter two graphs,  $V_{DS} = 1.2$  V and  $V_{GS} = 0.8$  V correspond to static bias conditions used to perform and extract HF figures-of-merit. Characteristic frequencies highlighted by a vertical dashed line in graphs 4(f) and 4(g) correspond to one tenth of the HF figure-of-merit (respectively unitary gain cutoff frequency  $f_T$  and maximum oscillation frequency  $f_{MAX}$ ). Around these characteristic frequencies, measured gains strictly follow the theoretical  $-20$  dB/dec slope. It ensues that relative variations of the  $H_{21}$  and  $U$  gains at these characteristic frequencies directly translate into variations of  $f_T$  and  $f_{MAX}$ , respectively.

after correction. Blue solid lines correspond to measurements performed on flat, green dashed and red dotted lines to measurements under flexure on a cylinder with 25 mm and 12.5 mm curvature radii, respectively. As in the case of DC measurements, both extrinsic and corrected S parameters exhibit only very slight variations regardless of measurement conditions, i.e., on flat or under flexure.

It is worth noting that the current gain  $H_{21}$ , Figure 4(d), and the Mason’s gain  $U$ , Figure 4(e), both closely follow the theoretical  $-20$  dB/dec slope from which  $f_T$  and  $f_{MAX}$  can be extracted by extrapolation from a high gain and low frequency region of the characteristics. The extraction of the maximum oscillation frequency  $f_{MAX}$  has also been performed from the maximum transducer gain, leading to similar values.<sup>41</sup> To summarize the results, Figures 4(d) and 4(e) show identical unity current gain  $H_{21}$  and Mason’s gain  $U$  on flat and bent configurations. Slight variations can be noticed in the insets of Figures 4(d) and 4(e) showing a zoom around 20 dB of gain, at frequencies ten times lower than  $f_T$  and  $f_{MAX}$ . Because the theoretical slope of  $-20$  dB/dec is well respected, the same  $f_T \sim 120$  GHz and  $f_{MAX} \sim 145$  GHz can be extracted on flat condition, and after bending on cylinders with a 25 mm and a 12.5 mm curvature radii. The relative variations of  $H_{21}$  under bending with respect to the flat state are given in Figure 4(f) at  $V_{DS} = 1.2$  V and  $V_{GS} = 0.8$  V, which correspond to the maximum of transconductance where best frequency performance is expected. Two

important points deserve a special attention from the analysis of Figure 4(f). First, to ensure that relative variations are meaningful and effectively induced by mechanical bending rather than introduced by the deembedding procedure, we have deliberately chosen two reference frequencies at  $f_T/10-12$  GHz and  $f_{MAX}/10-14.5$  GHz that are outlined by vertical dashed lines in Figs. 4(f) and 4(g). Second, relative variations of  $H_{21}$  and  $U$  remain below 2.8%, which is very close to the theoretical estimate previously calculated. These two reference frequencies are used in the following discussion that concentrates on a detailed analysis of the strain effect in neutral plane engineered UTTB CMOS transistors.

### III. DISCUSSION

Figure 5 gives an extended view of relative variations of static ( $\Delta I_{DS}$  and  $\Delta gm_{DC}$ ) and high frequency ( $\Delta f_T$  and  $\Delta f_{MAX}$ ) figures-of-merit. It globally demonstrates that electrical performance measured in bent configurations achieves good agreement with theoretical predictions calculated herebefore (Figure 2). Figures 5(a)–5(d) show relative variations with strain of one particular figure-of-merit for four similar transistors with geometries that only slightly differ by their gate length, 60 or 65 nm, and by their unitary gate width, 0.5, 1, or 2  $\mu$ m. In these four figures, individual measured data are represented by open symbols, average over

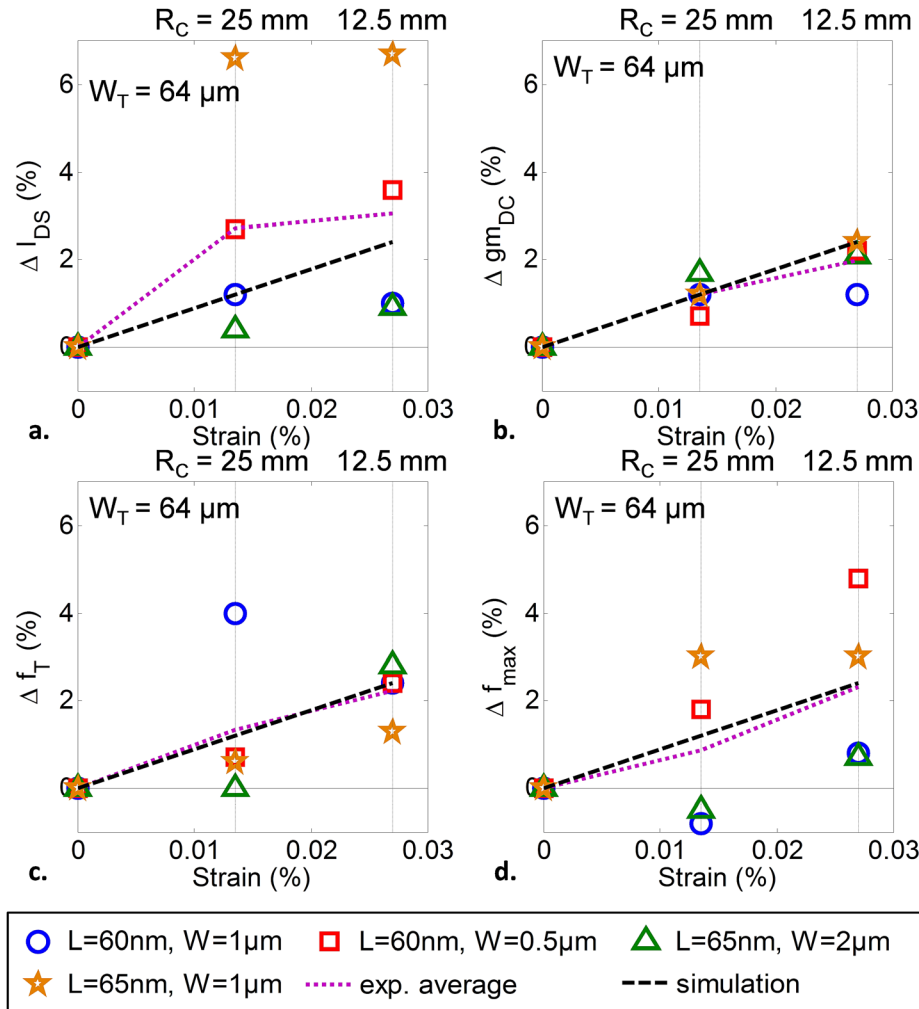


FIG. 5. Comparison of measured and simulated variations of selected electrical parameters. Relative variations of (a) drain current  $I_{DS}$ , (b) DC transconductance  $gm_{DC}$ , (c) unity gain cutoff frequency  $f_T$ , and (d) maximum oscillation frequency  $f_{MAX}$  versus strain generated in the active SOI layer of four different transistors (symbols) under flexure on 25 and 12.5 mm radius cylinders, in addition to average of experimental data points (magenta dotted lines) and theoretical predictions (black dashed lines). The four n-MOSFETs feature a total gate width development of 64  $\mu$ m. A good agreement is demonstrated between experimental variations of selected electrical parameters and their simulated counterpart after bending UTTB-CMOS transistors on cylinders with a curvature radius of 25 and 12.5 mm.



four transistors is drawn in magenta dotted line and theoretical predictions are plotted in black dashed lines. It can be observed that averaged measured variations for each figure-of-merit agree remarkably well with theoretical predictions. It can, therefore, be concluded that variations of electrical figures are limited to less than 5% as expected from the strategy of neutral plane engineering.

#### IV. CONCLUSION

Results presented in this paper demonstrate that industrial 65 nm partially depleted SOI MOSFETs thinned to micrometer-scale and transferred onto a plastic foil enable the fabrication of high performance devices with high bending stability. Slight variations of electrical properties (<5%) even after bending flexible CMOS dies on a cylinder with a curvature radius in the centimeter range pave the way to promising applications for foldable HF systems taking advantage of new form factors for heterogeneous integration. We finally comment that this work may lead to the development of foldable devices and circuits on plastic films operating in the 100 GHz frequency range for nomadic and SWAP constrained applications. Future investigations will bear on the characterization of HF circuits and communicating systems under flexure.

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#### APPENDIX: METHODOLOGIES

##### A. UTTB-CMOS fabrication

The starting material for the UTTB-CMOS fabrication is a conventional SOI wafer that features a bottom 780  $\mu\text{m}$  thick silicon handler, a 145 nm thick BOX layer, and a 60 nm thick active SOI film. After processing partially depleted SOI CMOS multi-finger gate 65 nm HF-MOSFETs, the wafer stack is completed with BEOL interconnect layers comprising six metal levels (copper) and one aluminium-cap. Details on similar thinning and transfer on plastic handler processes are described elsewhere.<sup>25,26,35</sup>

The first step of the transfer process onto a flexible organic film is the bonding of a temporary perforated sapphire carrier on top of the circuit chips in order to maintain rigidity during the thinning steps. The 780  $\mu\text{m}$  thick silicon handler is then removed by successively etching silicon by chemical mechanical lapping (using first 15  $\mu\text{m}$  then 3  $\mu\text{m}$  diameter alumina abrasive powder diluted in deionized water) and polishing, followed by a wet etching step in a mixture of nitric and hydrofluoric acids (9:1). A highly Si/SiO<sub>2</sub> selective dry etch by xenon difluoride (10 s pulsed etch steps) was used to remove the remaining silicon layer from the back side of the CMOS chip without

etching the BOX. After this step, the complete removal of the initial wafer handler has been achieved, resulting in an ultra-thin CMOS film of  $\sim 5.7 \mu\text{m}$  bonded on the temporary carrier wafer.

Unlike the previously published work,<sup>25,26,35</sup> the bonding of this thin film onto the flexible organic handler is not done by thermo-compression before the removal of the protecting sapphire carrier. In contrast, the temporary adhesive layer is first dissolved in acetone and the thin film is subsequently bonded at room temperature onto a flexible organic film. This method has been preferred because the thermo-compression step generates stress due to thermal mismatch between the inorganic film and the organic substrate. Bonding at room temperature results in a more reliable bonding and no buckling in the thin plastic film is observed.

The final multilayer system is, therefore, constituted of a thin flexible plastic handler, an adhesive layer, and the top-most part of the initial CMOS wafer comprising the BOX up to the top metal layer of the interconnection BEOL stack, as shown in Figs. 1(b) and 1(c).

##### B. Strain modeling and impact on electrical properties

The calculation of the deformed shape is performed assuming that planes orthogonal to the original reference surface remain flat and orthogonal to the deformed reference surface.<sup>21</sup> For symmetry reasons, strain and stress fields only depend on the position along the thickness axis of the sample. Bending a thin plate over a cylinder, whose radius is in the centimeter range results in infinitesimal strains but large rotation angles that invalidate the assumptions inherent to infinitesimal strain theory.<sup>42,43</sup> To overcome this limitation, strain and stress distributions in the plate cross-section have been calculated using the finite strain theory. This leads to an estimation of the strain and stress distributions in the UTTB-CMOS stack.

The material deformation gradient tensor  $\mathbf{F}$  associated to the cylindrical bending of a thin plate can be calculated using Eq. (A1), where  $r = h(X)$  describes the fact that horizontal material planes are transformed into concentric tubes and vertical planes into radial planes:  $\theta = v(Y)$ .<sup>42</sup> According to the polar decomposition theorem,<sup>42,43</sup> Eq. (A2)—stating that “any particle deformation can be expressed as a pure deformation followed by a rotation or by a rotation followed by a pure deformation”—the deformation gradient tensor can be expressed as a function of the right and left stretch tensors  $\mathbf{U}$  and  $\mathbf{V}$ , and the orthogonal rotation tensor  $\mathbf{R}$ . The right and left Cauchy-Green stretch tensors  $\mathbf{C}$  and  $\mathbf{B}$  can be calculated using Eqs. (A3a) and (A3b). A convenient and widely used finite strain metrics is the Green-Lagrange strain tensor  $\mathbf{E}$  described in Eq. (A4), where  $\mathbf{I}$  is the identity matrix, used to subtract rigid motion.

$$\mathbf{F} = \begin{bmatrix} h' & 0 & 0 \\ 0 & hv' & 0 \\ 0 & 0 & 1 \end{bmatrix}, \quad (\text{A1})$$

$$\mathbf{F} = \mathbf{R} \cdot \mathbf{U} = \mathbf{V} \cdot \mathbf{R}, \quad (\text{A2})$$

$$\mathbf{U}^2 = \mathbf{C} = \mathbf{F}^T \cdot \mathbf{F}, \quad (\text{A3a})$$

$$\mathbf{V}^2 = \mathbf{B} = \mathbf{F} \cdot \mathbf{F}^T, \quad (\text{A3b})$$

$$\mathbf{E} = \frac{1}{2}(\mathbf{C} - \mathbf{I}) = \frac{1}{2}(\mathbf{F}^T \cdot \mathbf{F} - \mathbf{I}). \quad (\text{A4})$$

The second Piola-Kirchhoff stress tensor  $\mathbf{S}$ —stress measure associated to the Green-Lagrange strain tensor  $\mathbf{E}$ —is a function of the Lamé coefficients  $\lambda$  and  $\mu$ , which are described in Eqs. (A5) and (A6), respectively, and the strain tensor  $\mathbf{E}$ , as written in Eq. (A7). The Cauchy strain tensor  $\boldsymbol{\sigma}$  can then be computed using Eq. (A8b).

$$\lambda = \frac{\nu E}{(1 + \nu)(1 - 2\nu)}, \quad (\text{A5})$$

$$\mu = \frac{E}{2(1 + \nu)}, \quad (\text{A6})$$

$$\mathbf{S} = \lambda \text{tr}(\mathbf{E}) \mathbf{I} + 2\mu \mathbf{E}, \quad (\text{A7})$$

$$\mathbf{S} = \det(\mathbf{F}) \mathbf{F}^{-1} \cdot \boldsymbol{\sigma} \cdot \mathbf{F}^{-T}, \quad (\text{A8a})$$

$$\boldsymbol{\sigma} = [\det(\mathbf{F})]^{-1} \mathbf{F} \cdot \mathbf{S} \cdot \mathbf{F}^T. \quad (\text{A8b})$$

The modeled stack contains 17 layers: from the plastic handler to the interconnection multilayer of the CMOS devices. After computing the level of stress in the SOI layer, the impact of strain on electrical properties is then evaluated using the piezoresistive tensor of monocrystalline silicon. The strain-dependent electron mobility  $\mu$  is calculated using the following piezoresistivity coefficients associated to an electron inversion layer:<sup>44</sup>

$$\pi_{11} = -84.0 \times 10^{-11} \text{Pa}^{-1}, \quad (\text{A9a})$$

$$\pi_{12} = 34.0 \times 10^{-11} \text{Pa}^{-1}, \quad (\text{A9b})$$

$$\pi_{44} = -17.0 \times 10^{-11} \text{Pa}^{-1}. \quad (\text{A9c})$$

Furthermore, transistors presented in this work feature a channel directed along the  $\langle 110 \rangle$  crystal orientation. As a result, the piezoresistivity coefficients referred to as longitudinal  $\pi_L$ , transverse  $\pi_T$ , and out-of-plane  $\pi_{\perp}$  are expressed in this coordinate system in Eqs. (A10a–A10c).

$$\pi_L = \frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44}), \quad (\text{A10a})$$

$$\pi_T = \frac{1}{2}(\pi_{11} + \pi_{12} - \pi_{44}), \quad (\text{A10b})$$

$$\pi_{\perp} = \pi_{12}. \quad (\text{A10c})$$

The piezoresistivity theory finally enables the calculation of the variation of carrier mobility  $\delta\mu$  using the relevant component of the stress tensor  $\boldsymbol{\sigma}$ , as presented in Eq. (A11).

$$\frac{\delta\mu_i}{\mu_0} = \sum_j -\pi_{ij} \sigma_j. \quad (\text{A11})$$

### C. Strain application and characterization

External mechanical strain is applied to the UTTB-CMOS transistors by bending on a semi-cylinder of known radius. The DC and HF characterization of flexible

n-MOSFETs is successively performed flatwise and under flexure using various semi-cylinders (from the larger to the smaller one). Characterization has been performed using Cascade Microtech RF Infinity Probes.

The OPEN deembedding methodology can be described by Eqs. (A12) to (A15). The admittance parameters of the “OPEN” structure are expressed as presented in Eq. (A12). The intrinsic transistor S parameters, Figure 4(c), are subsequently obtained by subtracting  $Y_{\text{OPEN}}$  to  $Y_{\text{TOT}}$ , as given by Eq. (A13). The “OPEN” structure can be characterized by the two open capacitances  $C_{\text{OPEN}_1}$  and  $C_{\text{OPEN}_2}$  calculated from Eqs. (A14) and (A15).

$$Y_{\text{OPEN}} = \begin{pmatrix} Y_{\text{OPEN}_1} + Y_{\text{OPEN}_2} & -Y_{\text{OPEN}_2} \\ -Y_{\text{OPEN}_2} & Y_{\text{OPEN}_2} + Y_{\text{OPEN}_3} \end{pmatrix}, \quad (\text{A12})$$

$$Y_{\text{DUT}} = Y_{\text{TOT}} - Y_{\text{OPEN}}, \quad (\text{A13})$$

$$C_{\text{OPEN}_1} = \frac{\text{Im}(Y_{\text{OPEN}}(1, 1) + Y_{\text{OPEN}}(1, 2))}{2\pi f}, \quad (\text{A14})$$

$$C_{\text{OPEN}_2} = \frac{\text{Im}(Y_{\text{OPEN}}(2, 2) + Y_{\text{OPEN}}(1, 2))}{2\pi f}. \quad (\text{A15})$$

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