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A Gate Level Methodology for Efficient Statistical Leakage Estimation in Complex 32nm Circuits

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***Abstract*- A fast and accurate statistical method that estimates at gate level the leakage power consumption of CMOS digital circuits is demonstrated. Means, variances and correlations of logic gate leakages are extracted at library characterization step, and used for subsequent circuit statistical computation. In this paper, the methodology is applied to an eleven thousand cells ST test IP. The circuit leakage analysis computation time is 400 times faster than a single fast-Spice corner analysis, while providing coherent results.**

***Index Terms*- Static Power, 32nm, leakage variability, correlation coefficients, covariance method, statistical leakage estimation**

I. Introduction

Leakage power increases with scaling. In addition, in nanometer technologies the variations have a large effect on leakage power [1]. Thus, accurate leakage power estimation is a key requirement in IC design.

Using MonteCarlo (MC) simulations, it is possible to obtain a relatively accurate estimation of the leakage distribution; however this is computationally expensive and not applicable on large circuits. Statistical leakage estimation which analytically estimates the leakage-current distribution of a circuit is a new and promising technique for leakage estimation (e.g. [2], [3]). There have been previous researches for estimating total leakage currents at both gate and circuit level. In [4] is presented, leakage estimation at gate level considering the effects of input vectors. But they did not consider the effect of local and global variation along with the effect of correlation between the variations on the total leakage, which is important to model. They compute the total leakage of a block using a probabilistic approach; however, they do not estimate the standard deviation of block.

In this work, the fully generic demonstrated methodology can easily predict the statistical parameters (median value and standard deviation) and the shape of the leakage probability distribution as a function of process parameters. Leakage mean and variance of individual cells, which are combined to find the total estimated leakage current, are characterized first. For an accurate analysis, correlations between cells and input state dependency are also considered.

The proposed statistical leakage estimation methodology has been applied to a complex block of eleven thousand gates (APIP), in 32nm ST Microelectronics technology.

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II. Statistical Library Cells Characterization

A. Characterization flow

The proposed approach involves a first step of characterization of leakage power mean (μ) and variance (σ^2) of each individual cell and for every input state possibility. For any cell/inputs-state combination, this is achieved using a MonteCarlo DC leakage electrical simulation, followed by simple mathematical calculations to extract the mean and variance. For the flip-flops, internal master and slave states are also considered in the combinations. At this stage, it is also necessary to build the correlation matrix between all the cell/inputs-state combinations (e.g. Table 1). To do this, we used a MC simulation embedding all cells/input states combinations without any cross-interconnections. Indeed, in 32nm high-k metal gate technology, the gate leakage is negligible, thus cells can be considered as high impedance input devices, and their interconnections have a negligible impact. Again, simple mathematical calculations are used to get the correlation factors from the simulations.

TABLE I. Example of Correlation Matrix

	INV_0	***INV_1***	***AND_00***	**…**	***NAND_111***
INV_0	1	0.6	0.7	0.62	0.5
INV_1	0.6	1	0.5	0.7	0.6
AND_00	0.7	0.5	1	0.58	0.72
…	0.62	0.7	0.58	1	0.64
NAND_111	0.5	0.6	0.72	0.64	1

B. APIP cells characterization results

In this work, we have limited the library characterization to the cells used in the APIP block. Eighty three cells/input combinations were involved. To build each cell table (leakage mean and variance for each input state), as well as the full correlation table, we performed simulations with 1000 MC runs (T=125C). The cells mean and variance complete characterization took 5 hours on a single computer, while the correlations simulation took thirty five minutes. In addition, the maximum relative error achieved in the correlation matrix is 0.4% with respect to the correlations obtained by Monte Carlo simulations. Those results demonstrate that this approach can be extended to a full library characterization, while keeping a reasonable computing time. For a large number of cells, it may be relevant to split the correlation

simulation into several smaller ones to optimize the accuracy and the computing time.

II. Gate Level Statistical Leakage Estimation

A. Circuit Leakage Estimation flow

The proposed methodology is based on the approximation that the sum of lognormal distributions is approximately lognormal [5]. Figure 1 display how the parameters of approximated lognormal distribution can be deduced from the parameter of the lognormal distributions fitted to each individual cell [6]. The algorithm for estimating the probability distribution function is as following: (1) the calculation of the total mean (M_{tot}) of the final lognormal distribution *LN(s)*; (2) the calculation of the total variance (V_{tot}) of *LN(s)*; (3) the calculation of $mu_{norm}(s)$ and $var_{norm}(s)$ (mean and variance of a normal distribution), using M_{tot} and V_{tot}; (4) the estimation of the final lognormal distribution *LN(s)* using $mu_{norm}(s)$ and $var_{norm}(s)$.

$$M_{tot} = \sum_{i=1}^{n} M_i \quad (1)$$

$$V_{tot} = \Sigma cov(X_i, X_j) = \Sigma \sqrt{var(X_i)var(X_j)}\rho(X_i, X_j) \quad (2)$$

$$mu_{norm}(s) = \ln(M_{tot}) - \frac{1}{2}\ln\left(1 + \frac{V_{tot}}{M_{tot}^2}\right) \quad (3)$$

$$var_{norm}(s) = \ln\left(1 + \frac{V_{tot}}{M_{tot}^2}\right) \quad (4)$$

$$LN(s) = f(\, mu_{norm}(s),\ var_{norm}(s)) \quad (5)$$

Fig. 1. Lognormal distribution estimation (M_i represents mean of a cell , X_i and X_j represents any pair of cell/input state leakage values, $\rho(X_i,X_j)$ the correlation between X_i and X_j, $cov(X_i,X_j)$ the covariance and $var(X_i)$ the variance)

In practical, the calculation of V_{tot} and M_{tot}, takes into account the number of instances of each cell/input-state combination to weight the library cell statistical values. The complete flow for statistical leakage analysis and estimation is illustrated in fig. 2. It is simple, fast and can be easily merged with existing CAD design flow.

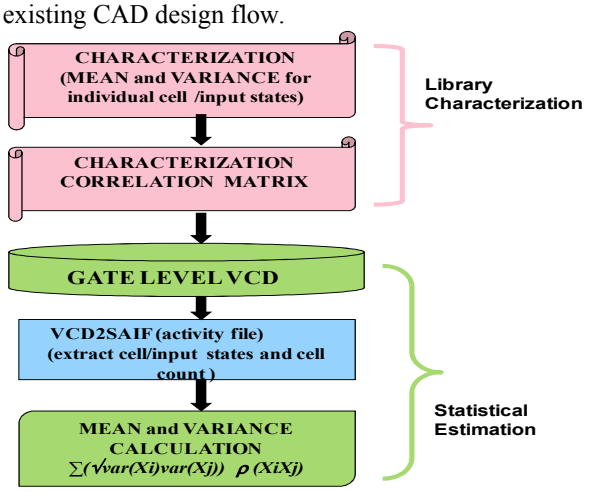

Fig. 2. Complete flow for statistical leakage analysis and estimation methodology

B. APIP statistical leakage results

The accuracy and computation efficiency of the statistical leakage analysis proposed in this paper were evaluated using as reference a fast Spice simulator, XA. Results are presented fig. 3. The probability distribution shown Fig. 3 covers all the corners estimated by XA tool. The computational time taken by the proposed methodology is nearly 400 times faster than any XA corner simulation on the same computer. To compare with MC approach on a Spice simulator, it took nearly 54hrs on ten computers in parallel, to simulate 2000 gates leakage with 1000 runs. Therefore, to get statistical leakage estimation for eleven thousand gates using MC is not feasible in terms of computation time. Our proposed approach overcomes this problem, while providing accurate results.

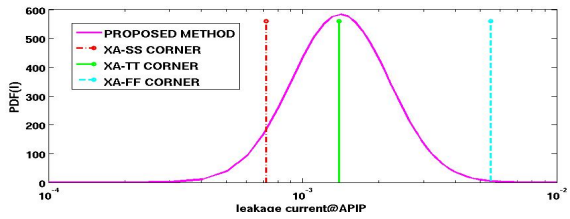

Fig. 3. APIP PDF distribution for leakage and XA corner simulations (x axis : log scale , y axis : PDF(I))

III. Conclusion

In this paper, a novel methodology to statistically estimate the distribution of the leakage current of complex circuit has been presented. It takes into account cells leakage correlations, as well as cells input state. Computation time of cells statistical leakage library characterization is compatible with existing flows. Circuit leakage estimation is very fast with a good accuracy. This method will be further extended to support spatial variations. The only required modifications are, at the characterization step, the extension of the correlation matrix adding a distance parameter, and, at the circuit estimation step, a link with the cells backend placement to determine the inter-cells distances and select the appropriate values in the correlation matrix for further calculations.

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