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Statistical Leakage Estimation in 32nm CMOS Considering Cells Correlations

Smriti Joshi [1]*, Anne Lombardot [1]
[1] STMicroelectronics
F-38926, Crolles, France,
{smriti.joshi,anne.lombardot }@st.com

Marc Belleville [2],Edith Beigne [2]
[2] CEA, LETI, MINATEC Campus
38054, Grenoble, France
{marc.belleville,edith.beigne}@cea.fr

Stéphane Girard [3]
[3] INRIA, Montbonnot,
38334, Saint-Ismier Cedex, France
{stephane.girard}@inrialpes.fr

Abstract-**In this paper a method to estimate the leakage power consumption of CMOS digital circuits taking into account input states and process variations is proposed. The statistical leakage estimation is based on a pre characterization of library cells considering correlations (ρ) between cells leakages. A method to create cells leakage correlation matrix is introduced. The maximum relative error achieved in the correlation matrix is 0.4% with respect to the correlations obtained by Monte Carlo simulations. Next the total circuit leakage is calculated from this matrix and cells leakage means and variances. The accuracy and efficiency of the approach is demonstrated on a C3540 (8 bit ALU) ISCAS85 Benchmark circuit.**

I. INTRODUCTION

As silicon industry is moving towards smaller and smaller critical dimensions, controlling device parameters during fabrication is becoming a great challenge. The variations in channel length, width, oxide thickness and channel doping profiles result in a large variation of the threshold voltage. As the leakage components in a device depend on the transistor geometry and threshold voltage, statistical variation of those parameters leads to a significant spread of the total leakage. This increased variability in advanced CMOS technologies is playing an increased role in determining the total leakage of a chip. This has accentuated the need to statistically account for leakage variations during the design cycle [1]. Designing for worst case leakage may cause excessive guard-banding, resulting in lower performances. Moreover, underestimating leakage variations can reduce the yield, as dies, violating the product leakage requirements, should be discarded.

In the past years, several works have focused on the problem of accurate prediction of leakage in digital circuits in the presence of variations. The previously proposed statistical leakage analyses approaches can be classified in three main groups. The first set of techniques approximate the transistor leakage currents with empirical equations (whose parameter are found by curve-fitting) or use Taylor expansion series to approximate the logarithmic expression of the leakage current [2-5]. The main drawback of this first group of statistical techniques is that their reliability with respect to manufacturing strongly depends on the correctness of the empiric relations used for the leakage current. The second set of methodologies proposes transistor models (developed simplifying the PSP/BSIM models, or elaborating manufacturing data) aware of process variations [6]. About this second group of methodologies, the major disadvantage is that the set of proposed equations needs new coefficients that have to be pre-determined (by fitting SPICE simulations or device extraction data for each library's cell). However, in [7] a novel methodology is proposed to estimate distributions of the leakage current of CMOS circuits in presence of process statistical variations integrated with standard BSIM4 and PSP transistor model. The third group consists of statistical leakage estimation based on Look Up Table (LUT) approaches [8-11]. LUT approach can be further subcategorized in two groups: a first category working at transistor level and second one working at cell level. In [10] is presented a statistical leakage estimation based on LUT of 23 stacks models of P-NMOS transistors in presence of PVT (process voltage temperature) variations combined with Neural Networks.

In this work we propose a solution to estimate the leakage current of larger circuit by modeling each gate for every input vector. This work is based on pre-characterizing library cells, and storing data like leakage mean, variance and correlations in tables. This is done for every input vector of each cell 10].

The rest of the paper is organized as follows. In Section II we describe briefly the motivation for using a Correlation Model. At this stage, we propose an approach to get cells leakage correlations. Section III describes a look up table approach for statistical leakage estimation. Then, in Section IV, we present the results obtained with this approach on the ISCAS 85 benchmark, 8-bit ALU,C3540 circuit, with a complete comparative analysis of our Look Up Table approach with a Monte Carlo approach. Conclusions are presented in Section V.

II. CORRELATION MODEL

A. Need of Correlation Models

To estimate accurately the full-chip leakage we must take into account the process variability and the inputs state, and the correlations between the different leakages have to be considered and modeled. In general, process variations can be classified into the following categories: inter-die variations are the variations from die to die, while intra-die variations correspond to the variability within a single chip. Inter-die variations affect all the devices on a same chip in the same way, while the intra-die variations may affect devices differently on the same chip. In addition, intra-die variations exhibit spatial correlation, i.e., devices located close to each other are more likely to have similar characteristics than those placed far away. Mathematically, inter-die variations can be regarded as a special case of intra-die variations with a correlation value of one. Under only inter-die variations, as the leakages of all gates or devices are sensitive to the process parameters in similar ways, the circuit performance can be analyzed at multiple process comers using deterministic analysis methods. With intra-die variations, statistical methods must be used to correctly predict the leakage [12].

In literature, to take into account the correlations, [12], [13] have taken into consideration both the effects of gate topologies and within-die spatial correlation. In [13] spatial correlations are modeled using a quad-tree die partitioning method. In [14], a grid model is used and the leakage is determined within a grid by summing a set of correlated lognormal distributions; then the full-chip leakage distribution is found by summing the leakage distributions of each grid. In [6] the correlation model is found by fitting the cell's leakage into a functional form to get three fitting parameters (a, b, c). Using these parameters, the leakage mean and standard deviation are analytically obtained. The fitted parameters also allow determining the leakage correlation between any pair of gates, given the channel length correlation .All these proposed methods, based on correlation models are complex for large circuits. In this paper, we propose a simpler approach to take into account the correlations, considering the inter and intra die variations.

B. Correlation matrix

The correlation is the degree to which two or more quantities are linearly associated. Given any pair of components, Xi and Xj, we denote their correlation as either cor(Xi,Xj) or ρ i,j. This Correlation is defined as

$$\rho_{i,j} = cov(Xi,Xj) / (\sigma_i \, \sigma_j) \qquad (1)$$

where σ i and σ j are the standard deviations of Xi and Xj.

As with covariance, we can summarize all the correlations of a random vector X with a symmetric correlation matrix, which gives the correlation coefficients between any pair of components:

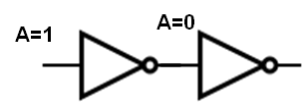
$$\boldsymbol{\rho} = \begin{pmatrix} \rho_{1,1} & \rho_{1,2} & \rho_{1,3} & \cdots & \rho_{1,n} \\ \rho_{2,1} & \rho_{2,2} & \rho_{2,3} & & \vdots \\ \rho_{3,1} & \rho_{3,2} & \rho_{3,3} & & \\ \vdots & & & \ddots & \\ \rho_{n,1} & & \cdots & & \rho_{n,n} \end{pmatrix}$$

Figure1. Correlation Matrix

To build this correlation matrix for a digital circuit we successively find out the correlation between the leakages of all standard library cells present in the circuit under study. .We can use the following approaches

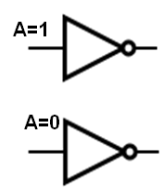
The simpler approach is to simulate the circuit and extract the leakage of each cell using Monte Carlo (MC) electrical simulations, and import the data from Monte Carlo to get the correlation matrix. This approach is not feasible for a big circuit, but will be used as a reference in this work. As an example, we used a small circuit made up of two inverters connected in series, we performed MC simulation on this circuit, extracted the leakage of each inverter and then calculated the correlation matrix shown in fig. 2.

In this work, we propose to use MC on single independent cells, including all input states combinations. We illustrate this approach with the two inverters as shown in fig. 3. We performed MC simulation on these two inverters (no connection between inverters), extracted the leakage of each inverter and then calculated the correlation matrix shown in fig. 3. If we compare the correlation matrix obtained from first and second approach we see that second approach gives 0.28% relative error with respect to correlation obtained from first approach i.e. Monte Carlo.



1	0.4635
0.4635	1

Figure 2. Schematic for First Approach and correlation matrix using MC



1	0.4622
0.4622	1

Figure 3. Schematic for Second Approach and correlation matrix using MC on single independent cells

We get similar correlation factors for Fig. 2 and Fig. 3 because gate leakage is negligible in 32nm high k metal technology, compared to other sources like sub threshold leakage, GIDL, DIBL. Thus cells can be considered as high impedance input devices, and their interconnections have a negligible impact.

We verified this approach on another schematic which consists of 10 cells (fig. 4a). We performed a 10,000 runs Monte Carlo simulation on the split schematic (fig. 4b) and we found similar results of approximately 0.4% of relative error

with respect to full-circuit Monte Carlo simulation extracted correlation coefficients.

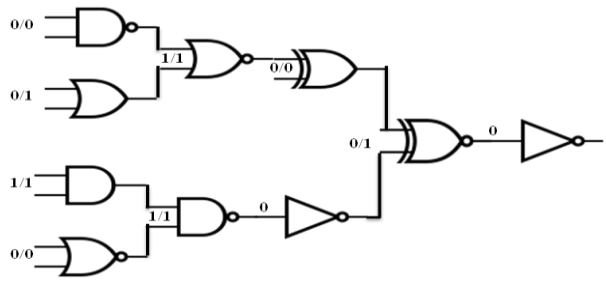


Figure 4a. Schematic A: Circuit with 10 gates

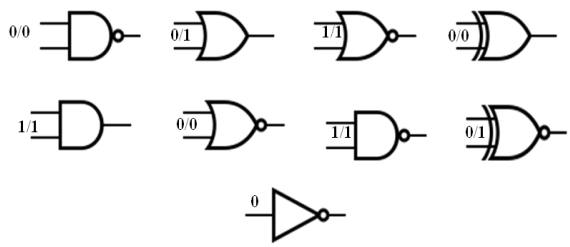


Figure 4b. Schematic for Second Approach for correlation matrix for Schematic A: Circuit with 10 gates

One major advantage of this approach is to limit the size of the simulations, as two identical cells will be replaced by a single instance. Therefore, it is compatible with a full standard cell library pre-characterization.

III. Leakage Estimation Methodology

Again, Monte Carlo will be used as a reference for this work. In this study leakage estimation is performed on technology mapped ISCAS circuits, which consist of fixed sets of cells. In order to enable a fast and efficient estimation, some information is pre computed for each cell of the library and stored in look-up tables. We also used the correlation matrix created for our leakage estimations.

A. Look Up Table Method at Cell Level

Look Up table approach involves the characterization of the mean (μ), variance (σ^2), and correlation (ρ) of leakage of each cell for each input state. To build each cell table (leakage mean and variance for each input state), we performed 10,000 simulations of Monte-Carlo Process Variations (MC-PV) at temperature (T=125C). In the MC-PV all process parameters are considered independents of each other and the variations are considered Gaussian with a deviation of $\pm 3\sigma$ around of their nominal value. In addition, the correlation matrix is built as previously described.

Table1 summarizes the content of the cells LUT.

Table 1. Content of Look Up table for Pre Characterized Cell

	A		B	…..	Z
Cell Name	INV	INV	AND	…..	NAND
Input state	0	1	00	…..	1111
Mean				……	
Variance				……	

The mean (μ) of the entire circuit is calculated as the sum of all mean's of all independent cells for a specific input state.

The variance (σ^2) of the entire circuit is calculated by taking the sum of all variance of each pre-characterized cell. For e.g. if there are two cells X and Y then the variance will be

$$\sigma^2 (I_{Leak}) = \sigma^2_X + \sigma^2_Y + 2\rho_{XY}\,\sigma_X\sigma_Y \qquad (2)$$

We explored this approach for the C3540 ISCAS 85 benchmark circuit.

IV. Leakage Estimation of a Simple Circuit and the ISCAS C3540 Circuit

In this section we present the results of the leakage estimation for the schematic A shown in figure 4 and for ISCAS 85 C3540 circuit, with a detailed comparison between Monte Carlo and the LUT approach.

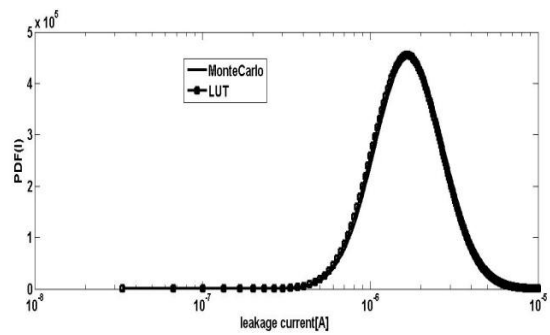


Figure5. Comparison of MC and LUT approach for Circuit with 10 gates i.e. Schematic A, PDF normalized by area, X axis (log scale): leakage current [A], Y axis: PDF(I)

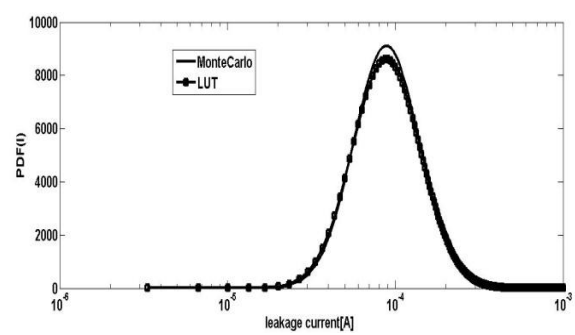


Figure6. Comparison of MC and LUT approach for C3540 ISCAS 85 circuit PDF normalized by area, X axis (log scale): leakage current [A], Y axis: PDF(I)

Variance calculated from LUT approach gives accurate results as we are considering the input state of each cell. We show the comparison of MC and LUT in fig. 5 and in fig. 6 for Schematic A and ISCAS C3540 circuit respectively. Detailed comparison for C3540 is shown in fig. 7, Q-Q plot, which compares Monte Carlo quantiles on horizontal axis with LUT quantiles on the vertical axis for ISCAS C3540 circuit. The linearity of the points shows that LUT fits the MC well. From Q-Q plot we can see that blue points are aligned with red points. From fig. 7, we computed that 99.9% of data are accurately mapped (blue line superimposed over red line in Q-Q plot) only 0.1% of data is overestimated by LUT approach, using the cell correlation coefficients.

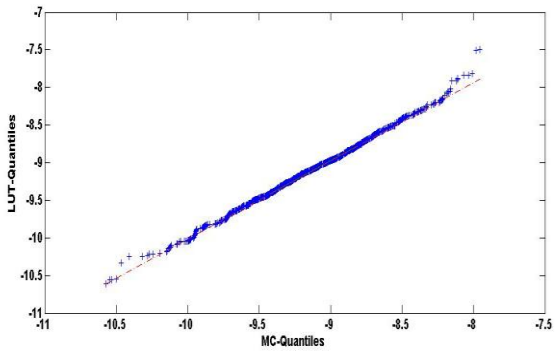


Figure7. Normalized Q-Q plot for MC and LUT approach for ISCAS C3540 circuit

As already mentioned one of the major advantage of this approach is to limit the size of the simulations, so by this methodology computational time will be reduced. For ISCAS C3540, Monte Carlo Simulation time was approximately one hr and leakage computation time by LUT approach, with cells correlations, was few seconds.

V. CONCLUSION

In this work we propose statistical leakage estimation methodology i.e. Look Up Table approach, taking into account cells leakage correlations. LUT approach is based on pre-characterized library cells and uses the cell leakage correlation factor for total variance calculation. This method had been validated using the ISCAS85 Benchmarks circuit C3540. The maximum relative error is 0.4% for correlation factor for bigger circuits. Also computational time for leakage estimation for bigger circuits is reduced by LUT approach.

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