Thermal Runaway Robustness of SiC VJFETs

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Abstract: Silicon Carbide (SiC) Junction-Field Effect Transistors (JFETs) are attractive devices for power electronics. Their high temperature capability should allow them to operate with a reduced cooling system. However, experiments described in this paper conclude to the existence of runaway conditions in which these transistors will reach destructive temperatures.

Introduction

One of the key advantage of SiC power devices over their Si counterparts is their ability to operate at higher temperature (in theory up to 1000°C for a 1000 V-rated SiC device as compared to 200°C for a comparable Si device [1]). Practical tests have already demonstrated operation at elevated temperature. For example, in [2], SiC JFET and diode operate at 450°C ambient temperature, although with considerable de-rating in saturation current and blocking voltage.

The high-junction-temperature uses of power devices can be divided in two sets of applications: operation in harsh environment (aerospace, oil exploration...), and operation with reduced cooling (small heatsink, confined system...). An example of this latter application is given in [3], with a converter designed to operate at an ambient temperature of 150°C with a junction temperature of its power devices as high as 250°C. This large drop between the junction and ambient temperatures allows for the use of a less sophisticated cooling system.

However, it has been demonstrated in [4] that the high temperature advantage of SiC might be limited because of thermal runaway issues. In a recent article [5], we studied this phenomenon on SiC diodes, and showed that purely unipolar diodes are prone to thermal runaway, whereas Merged PiN-Schottky (MPS) diodes are not.

A diagram explaining the thermal run-away mechanism is visible in fig 1: if we consider a simple cooling system (the plain line), it divides the Power/Temperature domain in two regions: in region A,

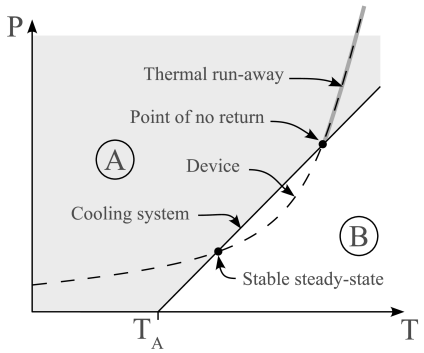

Fig 1: power dissipated by a device as a function of its temperature (dashed line), and cooling performance of its associated cooling system (plain)

above the plain line, the power dissipated is higher than what the cooling system can extract. Any system in region A will then tend to heat-up. On the opposite, a system in region B would tend to cool down, as the power it dissipates is lower that what the cooling system can extract. If we assume the imaginary device plotted in figure 1 (dashed line), we can see that there are two equilibrium points, where the power dissipated by the device is equal to what the cooling system can extract. However, the topmost equilibrium point is unstable: in particular, a small increase in the device junction temperature puts it in region A, where its temperature will increase indefinitely (that is, until the destruction of the device).

In this paper, we will investigate SiC JFET to find out if they are sensitive to such thermal runaway. We will first characterize some existing devices to build a model, and then use this model to simulate the thermal behaviour of the transistors.

Experimental procedure

In this paper, we performed I(V) measurements on two SiC JFETs. Both were manufactured by SiCED, but they correspond to two different generations of devices. The first has a 2.4x2.4 mm² die. The second, is more recent and was designed for higher power operation, with a 4.08x4.08 mm² die. Both have a 1200 V rating.

A special care was given to the test support to enable operation over a wide temperature range (- 70 to 300°C, Fig 1). Several dies were mounted on custom-supports (a piece of ceramic substrate) using sintered silver [6]. A thick (350 µm) copper leadframe was sintered to the substrate to provide convenient connections between the substrate and the test equipment. 4-point (Kelvin) connections to the source and drain were provided to minimize the influence of the support.

This support was connected to a Tektronix 371A high power curve tracer, operating in pulse mode to reduce the self-heating of the SiC JFET. The JFET was placed under the cap of a Thermonics T-2500E/300 temperature conditioner, to enable temperature forcing from -70 to +300°C, with 20°C increments. The temperature was measured on the backside of the substrate using a thermocouple.

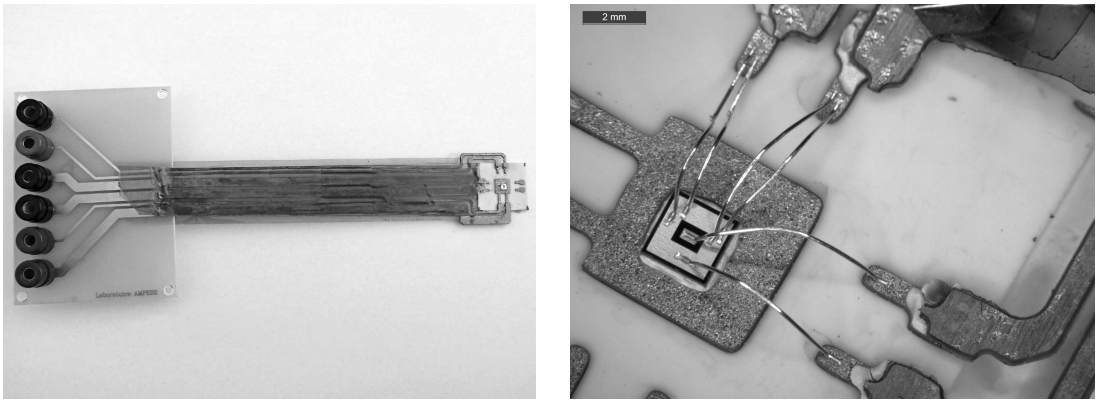

Fig 2: The test support, designed for high temperature operation (left) and a close-up picture of the SiC JFET die, with kelvin connections for more accurate forward characterization.

Empirical Model

Power electronics devices are designed be either fully off or fully on. For this analysis, we will only consider the “on” characteristic of the JFET. As the JFETs studied here are normally-on devices, this corresponds to a gate-to-source voltage (V_{gs}) of 0 V. Therefore, our analysis will focus on the losses and thermal stability of the JFETs in conduction mode only. A similar process can be applied to the blocking or switching losses, but it is beyond the scope of this paper.

A very simple, empirical model was fitted to the forward characteristic of the JFET:

$$I_D = P_0(T)\left(1 - e^{-P_1(T)V_{DS}}\right) \quad (1)$$

Where I_D is the drain current, V_{DS} the drain-to-source voltage, P_0 and P_1 two empirical parameters which depends on the temperature T. This model was fitted successively with the data acquired for each temperature. This resulted in a set of P_0 and P_1 values, one for each temperature. This set was fitted to a second empirical equation:

$$P_0 = \alpha_0 e^{\frac{-(T-\gamma_0)^2}{\delta_0}} + \sigma_0 \quad , \quad P_1 = \alpha_1 e^{\frac{-(T-\gamma_1)^2}{\delta_1}} + \sigma_1 \tag{2}$$

Where α, δ, σ and γ are constants. Note that a simpler model could have been used, but the evolution of P_0 and P_1 with temperature was different between both JFET types. With eq (2), we were able to use the same identification procedure for the 2.4x2.4 and the 4x4 mm² JFETs.

The results of the identification procedure can be seen in figure 3, where measurements and simulated results are superimposed.

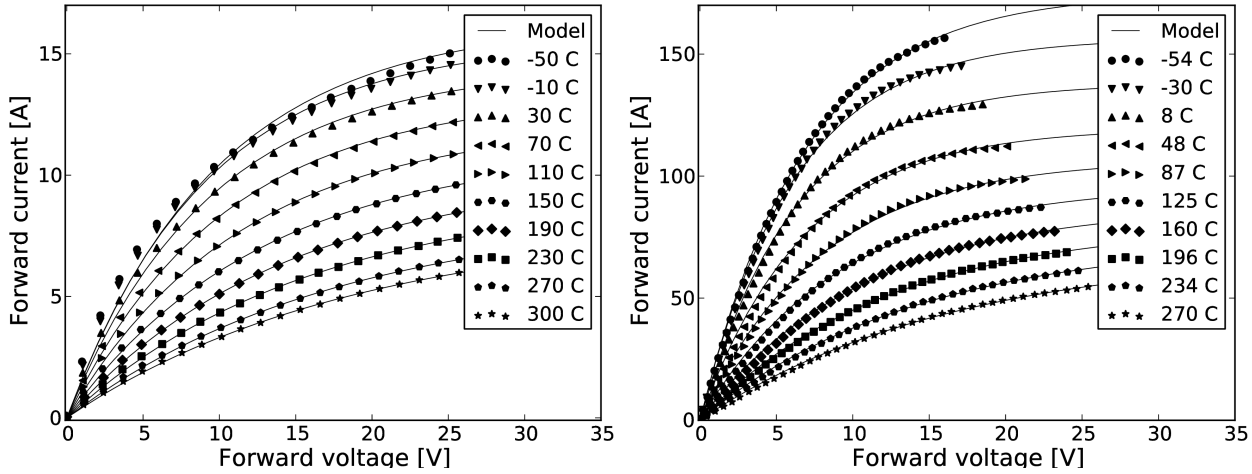

Fig 3: Forward characteristic of a fully-on JFET (i.e Vgs=0V) as a function of the temperature for two JFETs: 2.4x2.4 mm² die size (left) and 4x4 mm² die size (right). Note that the vertical scales are different.

Table 1: Parameters of the JFET models

device	α_0 [W]	δ_0[°C²]	σ_0[W]	γ_0[°C]	α_1[W]	δ_1[°C²]	σ_1[W]	γ_1[°C]
2.4x2.4mm²	10.35	9422	6.61	-130.7	0.0564	0.0510	0.0511	-2.097
4x4mm²	117.10^3	932.10^3	51.89	-2588	0.0994	0.0604	0.0604	-5.918

Thermal behaviour of the JFET

Using this model, we were able to forecast the behaviour of the JFET over a slightly larger (I_D ,V_{DS} ,T) domain than used for the measurements. Fig 4 presents the power dissipated by both JFETs as a function of their drain current and junction temperature. As with fig. 1, we superimposed the characteristic of some cooling systems (thick lines), operating in 25°C ambient, with thermal resistances of 1, 2, 4 and 8 K/W. 1 K/W corresponds to a very efficient cooling system, while 8 K/W is much easier to achieve.

Discussion and Conclusion

As a result, it appears that the thermal runaway phenomenon can be observed (for example, the "6 A" characteristic of the 2.4x2.4 mm² JFET and the "2 K/W" cooling system in figure 4 look very similar to the example in figure 1). Furthermore, the upward bend exhibited by the devices characteristic in figure 4 is more pronounced than expected in theory [4]. In [4], the increase in dissipated power with temperature is associated with the increase in electrical resistivity of the drift layer. For the JFET studied here, the increase in dissipated power (i.e. in voltage drop) is not only

caused by this increase in resistivity, but also by the decrease in the saturation current with the temperature.

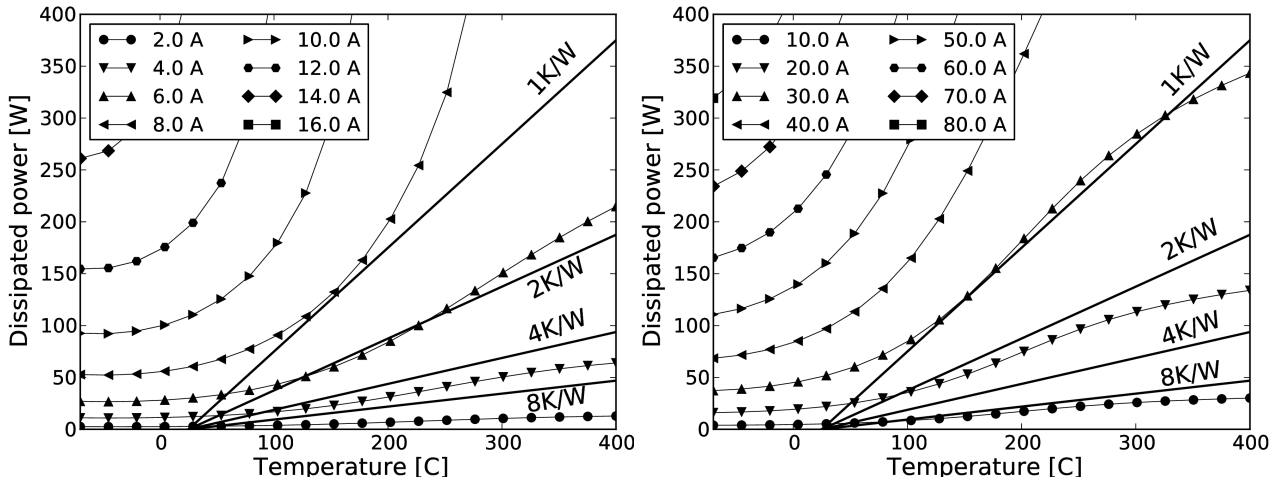

Fig 4: Dissipated power as a function of the forward current for a 2.4x2.4 (left) and a 4x4 mm² (right) JFET. Note that the forward current values are different between graphs

Although able to operate at high junction temperature, SiC JFETs are not insensitive to the thermal runaway mechanism. This means that even in a mild ambient temperature, they should be provided with a proper cooling system. This is especially important in the case of system that can be submitted to transient current or temperature overloads. For example, in the case of a 2.4x2.4 mm² JFET (Fig 4., left) operating with I_D=6 A and a 2 K/W cooling system in a 25°C ambient, any increase in the ambient temperature (i.e any shift of the cooling characteristics towards the right) will trigger the thermal runaway. It would be much safer to limit this transistor to 2 or 4 A.

Another interesting information from fig.4 (right) is the downward bend exhibited (for example) by the 30 A characteristic. This means that it should be possible to design the transistors to minimize their sensitivity to thermal runaway.

Acknowledgement

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