Reducing parasitic effects of actuation and sensing schemes for piezoelectric microelectromechanical resonators

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Abstract

The co-integration of piezoelectric actuation and sensing capabilities on microelectromechanical system-based resonators can be a source of electrical cross-talk that, if not properly taken into account, may dramatically affect the interpretation of the device's output. In this paper, we identify three parasitic electrical effects pertaining to the most commonly used piezoelectric actuation and sensing schemes. **To further investigate the impact of such parasitic effects**, microcantilevers, bridges and membranes integrating a layer of sol-gel lead zirconate titanate (PZT) were fabricated and electrically characterized. Experimental results on the resonant characteristics were compared with simulations of the studied resonators' equivalent electrical models. Methods for reducing the design-dependent parasitic electrical effects such as mutual capacitances of less than 10fF, electrical wiring or static capacitance mismatches of less than 20% of the integrated piezoelectric films are discussed.

Introduction

Piezoelectric materials enable high performance actuator and sensor systems satisfying dimensional integration constraints from the millimeter to the micrometer scale [1-3]. Piezoelectricity is appealing for electromechanical transduction as it allows energy conversion from the mechanical to the electrical domain and vice-versa. Extensive reports are available on the challenges associated with the integration of such materials at the microscale, as well as the direct impact of miniaturization and dimensionality on the electromechanical properties of the resulting devices [4-8]. Starting from H. Tilmans work [9] that laid the foundations for developing equivalent electrical circuits of electro-mechanical transducers and their interconnection to the outside world, Studies [10-13] where lumped element-based modeling is used to predict the behavior of multiphysics microsensors integrating piezoelectric active layers have been carried out. Nonetheless, the provided solutions are most of time application-dependent. Such dependence dramatically constraints the generic aim of the proposed models. In this paper, we propose a simplified electrical modeling of the chip hosting piezoelectric resonators presenting conventional geometries (cantilever, bridge and membrane) and the way in which the "electrical environment" of such integrated resonators may influence their performance.

In the following, a piezoelectric material sandwiched between two metallic electrodes will be called a ***piezo-cell*** and a microdevice integrating piezo-cells for actuation and/or sensing purposes as well as the contacting wires will be called a ***piezo-device***. To address the holistic electrical modeling of piezoelectric MEMS, one has to hierarchically answer three questions:

(1) The **piezo-cell** level: is there a generic way to electrically model a piezo-cell taking into account the influence of the associated parasitic "on chip-electrical wiring"?

(2) The **piezo-device** level: is there an ideal actuation/sensing element topology that minimizes the influence of the parasitic capacitances?

(3) The **system** level: based upon the answers to (1) and (2), is it possible to devise specific sensing electronics that effectively interface to the piezoelectric devices?

The on-chip actuation and sensing schemes studied in this paper along with the use of dedicated electronics developed for this purpose aim to answer these questions. A series of design rules for piezoelectric materials integration is proposed from the standpoint of MEMS-based resonator development.

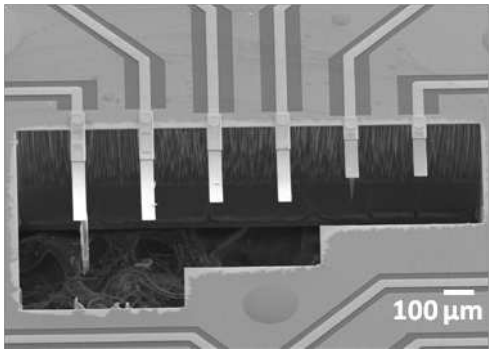
Device Fabrication

The fabrication process for the MEMS resonators is depicted in Fig. S1 (see Supplementary Information file). A double-side polished silicon-on-insulator (SOI) wafer with a 2 µm Si device layer and a 1 µm buried oxide layer was used as the starting substrate. The mask set for the wafer hosts chips bearing cantilevers, bridges and membranes. The cantilevers and bridges are 50-µm wide and paired, with lengths of 300 µm, 500 µm or 700 µm. The piezoelectric layer covers one quarter of the full length of the cantilevers, beginning at the clamping point to the substrate and one eighth of the bridge length at each of the ends. The membranes are circular with diameters of 50µm, 200 µm or 450 µm. The piezoelectric layer covers two distinct regions on each membrane: an inner full circle with a diameter that is half the full membrane diameter, and an outer ring-like area with a width that is 0.25 of the membrane's diameter.

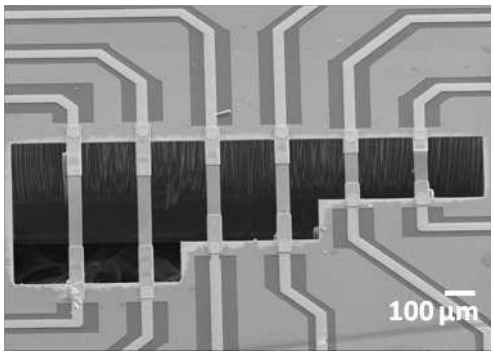
To fabricate these devices, the first step was the growth of a 100-nm-thick thermal silicon dioxide film on the SOI wafer. A metal-complex oxide-metal sandwich structure was then deposited on the thermal SiO_2. A bottom electrode consisting of a 20 nm titanium adhesion layer and 100nm platinum of Pt was then deposited. A 1.6 µm layer of lead zirconate titanate (PZT: $Pb(Zr_{0.52}Ti_{0.48})O_3$) was then spin deposited from a sol gel solution on the bottom electrode as described elsewhere [14]. Finally, a top electrode of 100nm of platinum was sputter deposited on the PZT. Subsequent lithography defined the active device structure. The active device pattern was transferred to the top electrode (100nm Pt) and the 1.6 µm PZT layer by dry etching using a thick resist as a mask (Shipley SPR220). The dry etch process was run in a Tegal 6540 HRe^{-} capacitively coupled plasma chamber using a mixture of Cl_2 and CF_4 gases and a process pressure of ~ 5 mTorr. The PZT etch was stopped on the bottom platinum

electrode. A second set of lithography and plasma etch steps were used to define the bottom electrode patterns. A 400-nm-thick isolation film of silicon dioxide was then sputter deposited to avoid possible hydrogen damage of the PZT piezoelectric layer. Contact lithography and inductively coupled plasma (ICP) oxide etch processes were then used to open contacts to both top and bottom electrodes. The interconnect traces and pads were formed by a liftoff process of an electron beam-evaporated Ti/Au (10/150 nm) metal onto an undercut bi-level resist structure. A separate lithography step was then utilized to define the cantilever device structures; the isolation oxide, device silicon and buried oxide was etched using ICP etch processes (in a PlasmaTherm Versalock cluster tool) to form the beam structures. The cantilever and membrane devices were released utilizing backside thick resist lithography and Bosch etching through the handle wafer. The etching was stopped on the SOI buried oxide layer. During this step, the front-side structures were protected with a thick resist layer. After the handle wafer etch, the protection resist was removed to release both cantilever structures and membrane structures and the device chips were gently extracted from the wafer by applying pressure with tweezers at the separating paths running through the wafer.

Scanning electron microscope (SEM) images of micromachined cantilevers, bridges and membrane devices are shown in Figure 1. Following fabrication, the cantilevers exhibit out-of-plane static deflection as a result of global tensile stresses specific to the multilayer sandwich structure of the devices.



(a)



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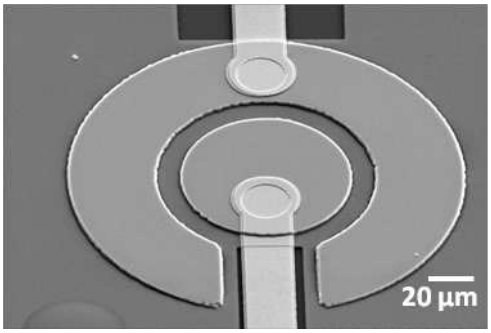


(c)

Figure 1: SEM images of micromachined (a) cantilevers, (b) bridges and (c) membrane devices.

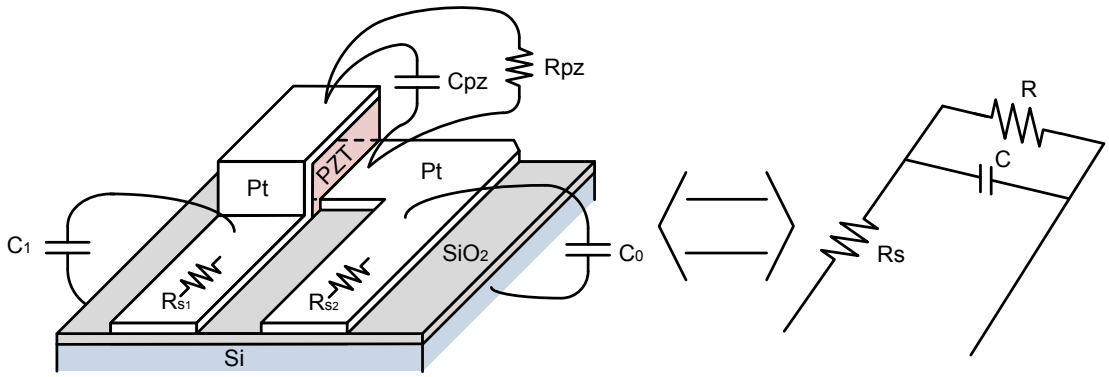
Figure S2 (Supplementary Information file) shows the layout of the cantilevers/bridges and membranes chips as well as the identification of the different actuation/sensing piezoelectric areas corresponding to each device.

Electrical modeling of a generic piezo-cell

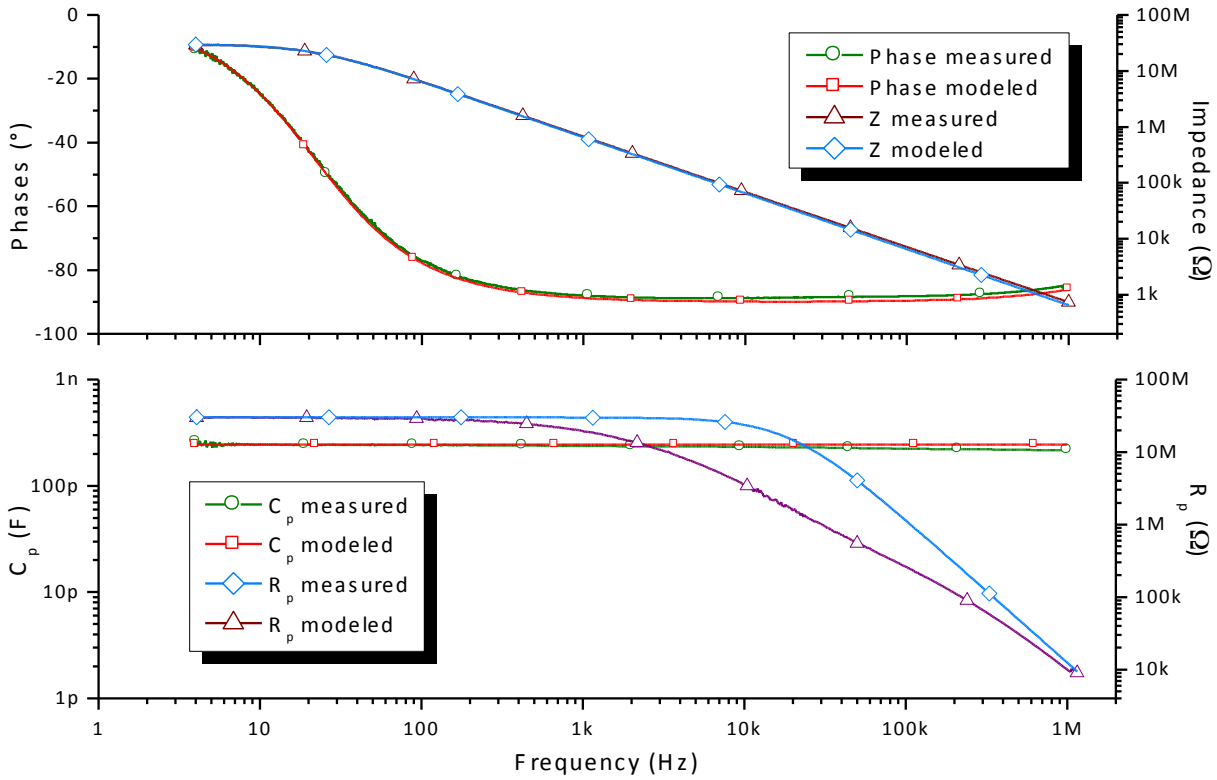
The integration of piezoelectric thin films for different MEMS applications is commonly performed on metalized silicon substrates. Typical doping levels of such substrates (even at low values, i.e. 10^{13} dopant atoms/cm^3) render them rather conductive when compared to ceramic substrates. To electrically isolate piezo-cells from the underlying silicon substrate, one generally grows silicon dioxide onto the substrate prior to the piezo-cell patterning. This SiO_2 (or ZrO_2, HfO_2, etc.) layer also serves to minimize reactions between Pt metallization and the Si at typical process temperatures for perovskite piezoelectrics.

In order to model a simple equivalent electrical circuit, we proceed to a R_p-C_p base transformation of the gain-phase measurement and subsequently identify the equivalent R_s, C and R values (where R_s is the series resistance of the electrical wiring while C and R are respectively the capacitance and resistance of the piezo-device including **R_{pz} – piezocell's resistance and C_{pz} – piezocell's capacitance**), as depicted in Figure 2(a).

The R_p and C_p values are respectively given by $R_p = \frac{|Z|}{cos\theta}$ and $C_p = \frac{-sin\theta}{|Z|\omega}$ whereas the impedance $Z = R_S + \frac{R}{1+jRC\omega}$. Figure 2.(b) compares the measured and modeled data using the extracted parameters for a $S1_i$ circular piezo-cell.



(a)



(b)

Figure 2: (a) Equivalent circuit of a piezo-device; (b) Gain-phase and corresponding R_p-C_p frequency responses of a $S1_i$ circular piezo-cell. The graphs include both measured responses (green and blue colored) and corresponding theoretical fit (red and magenta colored).

The R_s, C and R parameters are extracted as follows: first, on the R_p-C_p response, the C_p value is used for the C value, the low frequency R_p value is defined as the equivalent resistance R of the piezo-cell and the R_s value is extracted from the high-frequency R_p measured response. This strategy is proved to be physically relevant as the as-extracted R_s, R and C values are then implemented in the corresponding gain-phase response and the resulting simulated response is in excellent agreement with the measured characteristics.

We then proceeded in the same way to extract R_s, R and C values for all piezo-cell geometries on two different chips. Values are listed below (Table 1) together with the theoretical C values for comparison.

Table 1: Values of the series resistance for the electrical wiring (R_s), the resistance of the piezo-layer (R) and the global capacitance of the piezo-cell and associated electrical wiring (C_{meas}) extracted from gain-phase measurements similar to Figure 7 and comparison with corresponding global capacitance theoretical value ($C_{calculated}$)

Cantilever/Bridge Chip

Structure	R_s(Ω)	R(GΩ)	C_{meas}(pF)	$C_{calculated}$(pF)
S1	60	50	44	66
S2	70	50	43	59
S3	60	50	63	77
S4	60	50	65	78
S5	50	50	82	99
S6	60	50	86	107
$S7_l$	70	50	43	66
$S7_r$	70	50	45	68
$S8_l$	60	50	46	71
$S8_r$	60	50	43	61
$S9_l$	50	50	69	99
$S9_r$	50	50	63	78
$S10_l$	50	50	70	99

Membrane Chip

Structure	R_s(Ω)	R(MΩ)	C_{meas}(pF)	$C_{calculated}$(pF)
$S1_i$	45	30	245	239
$S1_o$	35	4000	850	718
$S2_i$	30	120	240	238
$S2_o$	18	5000	820	718
$S3_i$	23	800	240	239
$S3_o$	15	2000	830	719
$S4_i$	90	280	55	68
$S4_o$	40	500	160	164
$S5_i$	60	700	60	82
$S5_o$	50	2500	165	178
$S6_i$	50	50	65	96
$S6_o$	50	1500	170	191
$S7_i$	100	15000	11	27

$S10_r$	50	50	62	78	$S7_o$	150	7000	16	33
$S11_l$	50	50	87	111	$S8_i$	150	15000	27	27
$S11_r$	45	50	82	99	$S8_o$	150	20000	27	33
$S12_l$	50	50	85	106	$S9_i$	150	20000	27	30
$S12_r$	45	50	85	104	$S9_o$	100	10000	28	34

A qualitative analysis of the Table 1 values reveals that:

- R systematically takes high resistance values (over tens of MΩ), which is consistent with the high resistivities of the patterned sol-gel PZT (R_{pz}) electrical properties used in this study and may include the leakage substrate resistive effects;
- R_s ranges from 15Ω to 150Ω, which is consistent with the series resistances values of the metallization measured on the Ti/Pt/Au stacks used to connect on-chip devices, resistive contact effects and bonding effects;
- The measured C values are of the same order of magnitude as the calculated values, but are not identical. This confirms the impact of the on-chip electrical wiring on the capacitive behavior of the piezo-cell. The influence of the wiring on the measured capacitance becomes progressively smaller for larger electrode areas on the PZT.

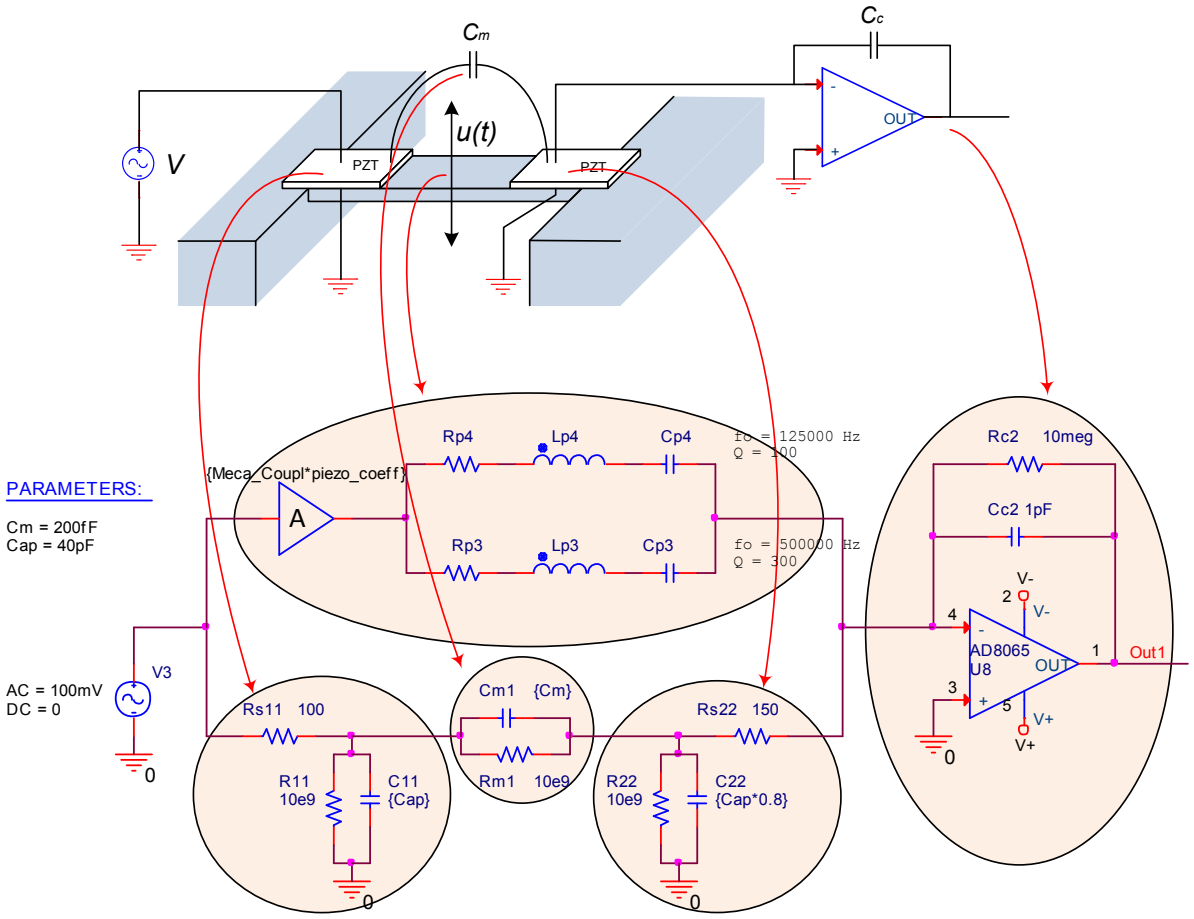
Actuation and sensing strategies: Minimizing the impact of on-chip, design dependent parasitic capacitive effects

The generic equivalent electrical model of a piezo-cell (R_s, R, C) can be subsequently implemented in piezoelectric transduction schemes [4, 7, 15, 16] in order to assess the configuration that minimizes the impact of parasitic capacitance on the actuation and sensing performance at the device level. In the present section, we will discuss two widely used actuation and sensing strategies and comment on the limitations imposed by parasitic effects inherent to silicon chip design. The first is the "***duo-piezo-cell structure***" which includes two separated piezo-cells on a single MEMS resonator, one dedicated to the actuation and the other to the detection. This is often achieved using clamped-clamped structures, such as bridges or membranes. The second is the "***mono-piezo-cell***

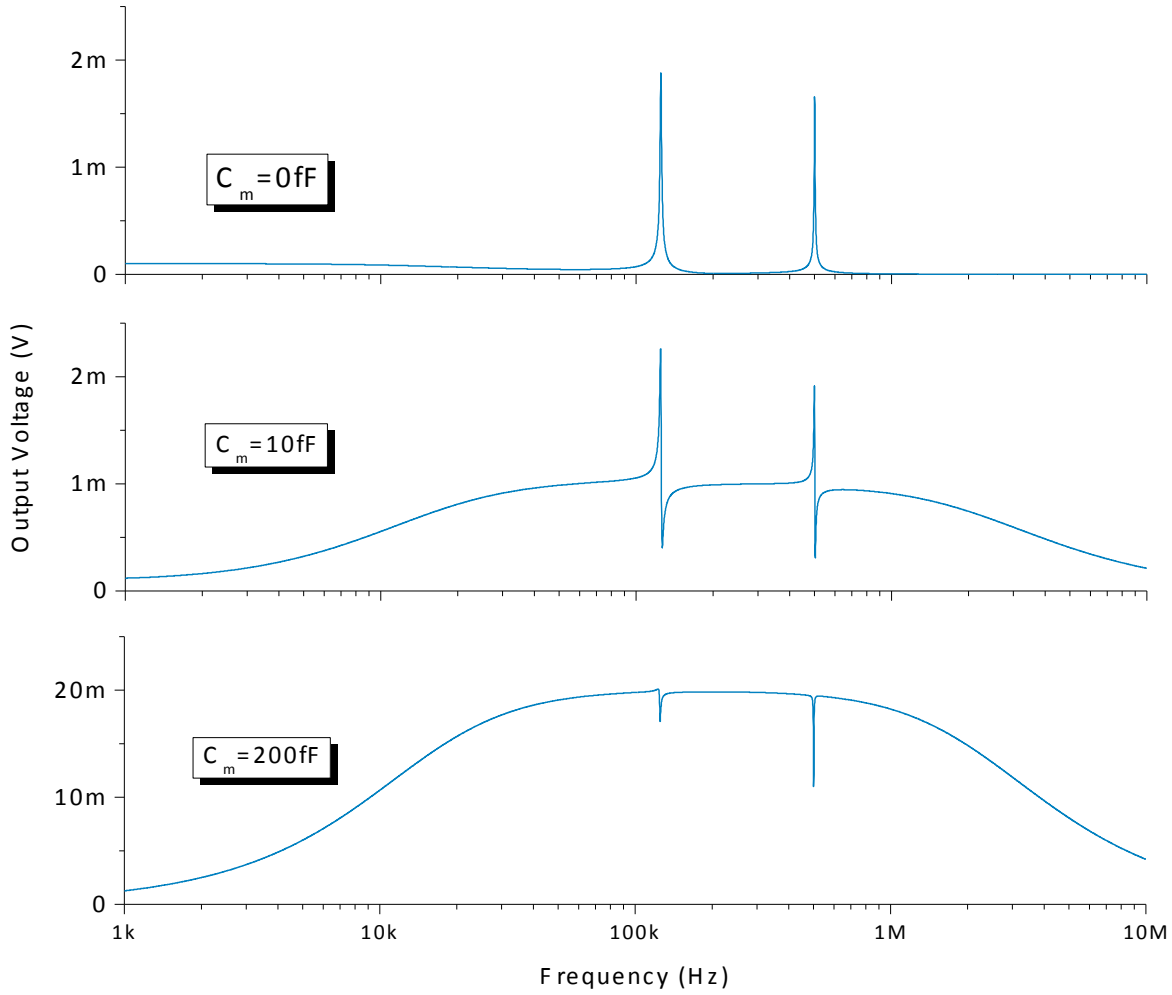
structure" where the MEMS resonator needs only one piezo-cell. A second identical unreleased piezo-cell is placed next to the previous one to be used as reference.

The "duo-piezo-cell structure"

Figure 3.(a) depicts a clamped-clamped resonator bearing two piezo-cells, one of which is used for actuation, while the other is intended for sensing purposes. The electrical charges generated by the sensing piezo-cell can be written as $q(t) = CV_{sense} - xu(t)$ where C takes into account the piezoelectric film and the associated on-chip electrical wiring capacitances, x is a transduction coefficient (C/m) and $u(t)$ is the out-of-plane mechanical displacement of the beam. In this specific configuration, V_{sense} is set to zero, which means that at the output of the charge amplifier, $V_{out} = \frac{xu(t)}{C_c}$ where C_c is the feedback capacitor of the charge amplifier.



(a)



(b)

Figure 3: (a) Schematic and behavioral modeling of a clamped-clamped beam with piezoelectric integrated actuation/sensing piezo-cells. (b) Simulated V_{out}(V) at the output of the charge amplifier as a function of frequency for three different values of mutual capacitance C_m

In order to assess the global electrical behavior of the duo-piezo-cell configuration, an equivalent electrical model for the device shown in Figure 3.(a) scheme was implemented and run using a PSpice simulator. To model the experimental data, two resonant modes of the clamped-clamped beam were represented by two *RLC* equivalent circuits where the gain A corresponds to the electromechanical transduction coefficient The electrical response is simulated on a 1kHz – 10MHz frequency range with a 100mV excitation amplitude. In addition, the mutual capacitance (C_m) between the two piezo-cells was considered to assess the impact of this supplementary parasitic element on the global electrical

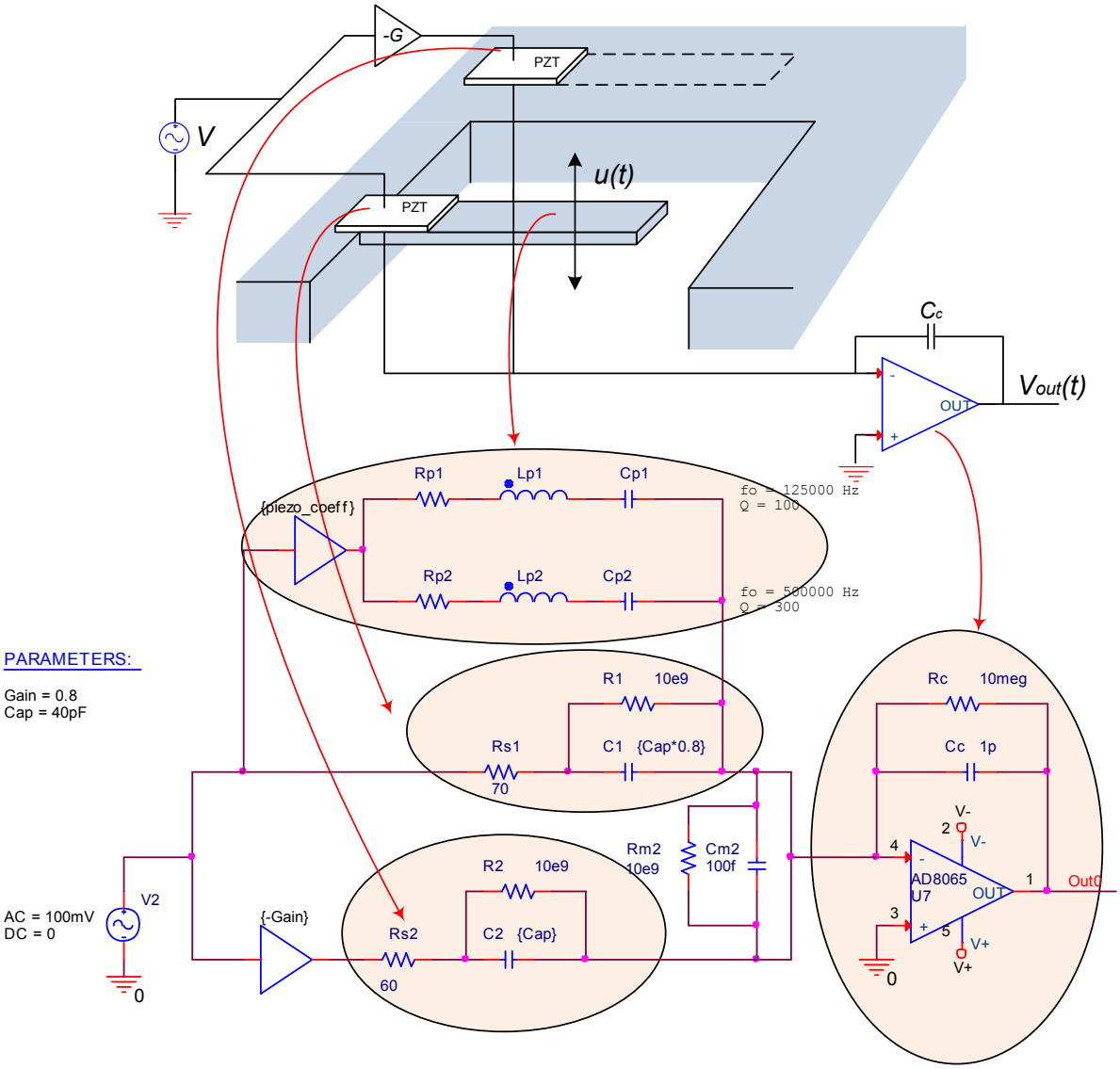
behavior of the resonator. A large resistance R_m (of order 1GΩ) was added to account for surface leakage currents between the two piezo-cells. Practically, this would describe finite leakages associated with environmental conditions such as moisture, or surface defects on the chip. For simplicity, the finite ac field dependence of the permittivity of the PZT films [17] was neglected. The simulation result for three different values of C_m (0, 10fF and 200fF) is presented in Figure 3.(b).

For the low frequency range (*i.e.* below the cutoff frequency of the charge amplifier feedback filter) the output charge amplifier voltage is given by the ratio of the feedback resistance of the charge amplifier and R_m, such as $V_{out} = \frac{R_{c2}}{R_m} V_{in}$. For frequencies above the cutoff frequency, the influence of the mutual capacitance can be assessed by observing the modification of the shape of the resonant frequency peaks. For instance, in Figure 3.(b), in the case of the 200 fF value for C_m, the peaks invert. At these frequencies, the magnitude of the plateau is given by $V_{out} = \frac{C_m}{C_c} V_{in}$. Thus, these parasitic effects result from the influence of C_m and they cannot be avoided. The main advantage of a duo-piezo-cell actuation/sensing scheme is the suppression of the effect of the static capacitance of the sensing piezo-cell. However, the model demonstrates that this comes at a price of considerable impact of the mutual capacitance on the peak shape. This effect becomes increasingly important as the dimensions of the resonator shrink, as will be demonstrated in the experimental validation section of this work.

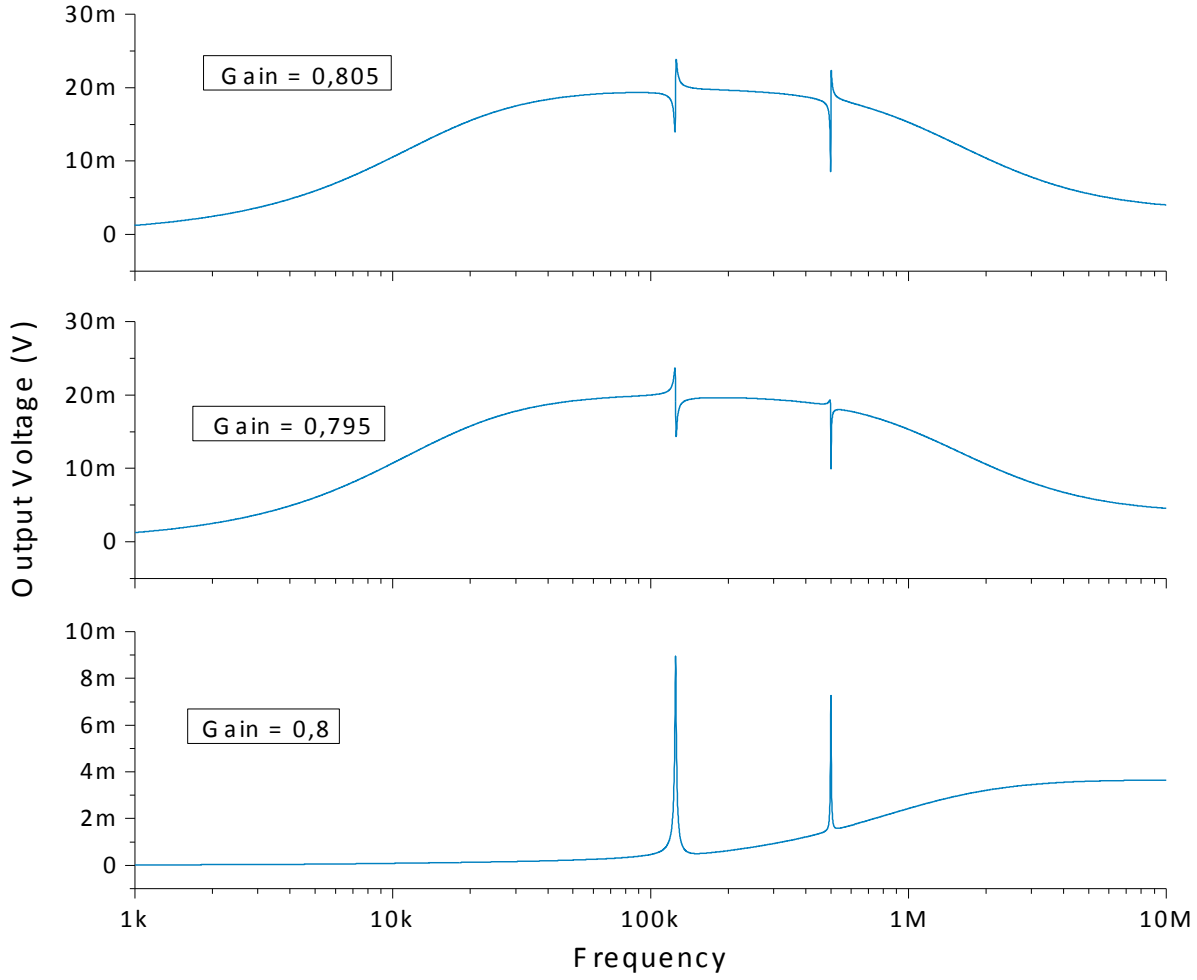
The "mono-piezo-cell structure"

Figure 4.(a) depicts a clamped-free resonator bearing one piezo-cell used for actuation or sensing while a second remote piezo-cell is used as a reference capacitor. Comparable schemes have been used since Lee et al.'s seminal work [4] proposing the first atomic force microscope, where the optical detection scheme was replaced by an equivalent piezoelectric one. In this case, the charge amplifier voltage is given by $V_{out}(t) = \frac{(GC_{p2} - C_{p1})V + xu(t)}{C_c}$ where C_{p1} and C_{p2}, respectively, account for the piezoelectric film and the associated on-chip electrical wiring capacitances for each of the piezo-cells. The gain G allows the piezo-cells to be balanced, so that after tuning G, $V_{out}(t) = \frac{xu(t)}{C_c}$.

In order to assess the global electrical behavior of the mono-piezo-cell configuration, the equivalent electrical model for the device shown in Figure 4.(a) was implemented using a PSpice simulator. Two resonant modes of the clamped-free beam (the same as for the previous case) were represented by the resonances of two *RLC* equivalent circuits. In this configuration, the mutual capacitance between the piezo-cells has no effect on the output. Moreover, this design allows cancellation of the mutual capacitance due to the distance between the piezo-cells. The piezo-cells' capacitances values intentionally differ by 20% in this example in order to assess the role of fabrication variations on the global electrical behavior of the resonator, where $G = 0.8$ cancels the 20% difference between C_{p1} and C_{p2}. The simulation result of slight variations of the gain around its optimal value (*G* being respectively equal to 0.795, 0.8 and 0.805) is shown in Figure 4.(b):


-G
PZT
V
u(t)
PZT
Cc
Vout(t)
OUT
Rp1
Lp1
Cp1
{piezo_coeff}
fo = 125000 Hz
Q = 100
Rp2
Lp2
Cp2
fo = 500000 Hz
Q = 300
PARAMETERS:
Gain = 0.8
Cap = 40pF
R1
10e9
Rs1
C1
{Cap*0.8}
70
Rc
10meg
Cc
1p
V-
V-
AD8065
U7
OUT
Out0
V+
V+
AC = 100mV
DC = 0
V2
0
{-Gain}
R2
10e9
Rs2
C2
{Cap}
60
Rm2
10e9
Cm2
100f
0

(a)



(b)

Figure 4: Schematics and behavioral modeling of a clamped-free beam with a single actuation/sensing piezo-cell with a remote reference piezo-cell, which in this specific configuration remains unreleased from the substrate; (b) Simulated V_{out}(V) at the output of the charge amplifier as a function of frequency for three different values of balance gain G

The simulation was performed for a S_2 cantilever (see Supplementary Information file) with a static equivalent capacitance of 40pF. The generated charge value from the released piezo-cell is equal to 3.2pC compared to 4pC generated by the reference piezo-cell because of the 20% difference of static capacitances. It is clearly seen from Figure 4.(b) that a compensation gain equal to 0.8 perfectly balances the charges of both piezo-cells. A much cleaner resonant characteristic also results from

appropriate compensation of the static capacitances. A slight detuning of G to 0.795 or 0.805 immediately unbalances the piezo-cells compensation and subsequently produces residual corresponding charges of 20fC which increase the off-resonance voltage level to 20mV and hence dramatically impact the resonance shapes. Thus, for such an actuation/sensing scheme where the mutual capacitance effects are canceled by design, the compensation of static capacitance is key to obtain close-to-Lorentzian shaped resonance responses.

Sensing specific electronics set-up and validation

To experimentally confirm the effects of the mutual capacitance and of capacitive variations as described in the previous sections, an electronics set-up was designed and constructed as illustrated in Figure 5.

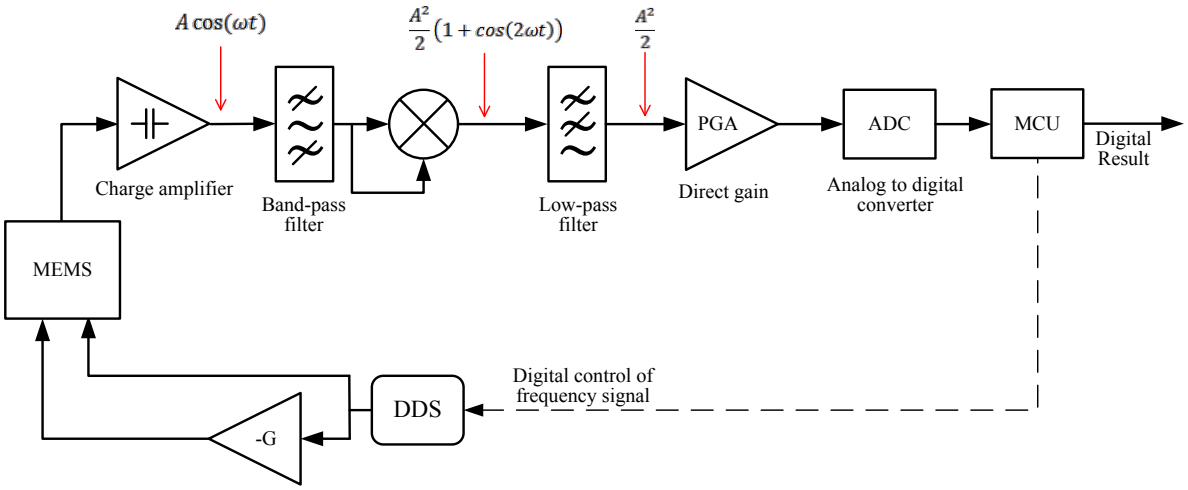


Figure 5: Schematic of the electronic set-up for piezo-MEMS actuation/sensing purposes. A is the amplification factor, PGA stands for Programmable Gate Array, ADC is the Analog-to-Digital Converter used to drive the microcontroller unit (MCU) and DDS is the Direct Digital Synthesizer.

A sinusoidal voltage of constant amplitude (10mV-4V) is applied to the piezo-cells for actuation by a Direct Digital Synthesizer (AD9832, Analog Device, USA). The same signal may be fed through a negative gain amplifier and subsequently applied to the piezo-cells used for compensation (in mono-piezo-cell configuration). The piezo-MEMS output signal is then amplified by a charge amplifier (1

V/pC) and fed through a wide band-pass filter (10 kHz-2 MHz) to eliminate low frequency and digital noise. The signal is then multiplied by itself and low-band filtered to obtain a DC signal corresponding to its amplitude at a given frequency. This square of the signal is amplified by a settable gain (called the direct gain). The resulting analog signal is digitized to perform averaging, digital feedback for the frequency excitation, search for resonance modes in a given frequency band, calculation of the quality factor, and calculation and driving of the optimal direct gain. Data were sent through a USB (Universal Serial Bus) to a PC (Personal Computer) with a custom GUI (Graphical **User** Interface). Further actions can be performed subsequently, including: control and setting of the electronic card, acquisition of wide spectrum response, display of specific resonant modes with associated quality factors assessment, monitoring of a specific resonant mode, etc.

The importance of mutual capacitance effects is amplified when the actuation and sensing piezo-cells are on the same resonating structure. This configuration is met in the case of the circular membranes. The first spectrum in Figure 6 represents the effect of the mutual capacitance on the electrical dynamic response of a membrane (structure S_1 in Figure S3, on the membrane chip). A 30mV voltage is used to actuate the membrane on its inner electrode (the S_{1i} piezo-cell) while sensing is performed using the outer electrode (structure S_{1o} piezo-cell). It is worth noting that in Fig. 6(a) the voltage response presents inverted resonant peaks. In contrast, the mutual capacitance is eliminated when a remote piezo-cell (say, S_{40}) on the same chip, is used for sensing.

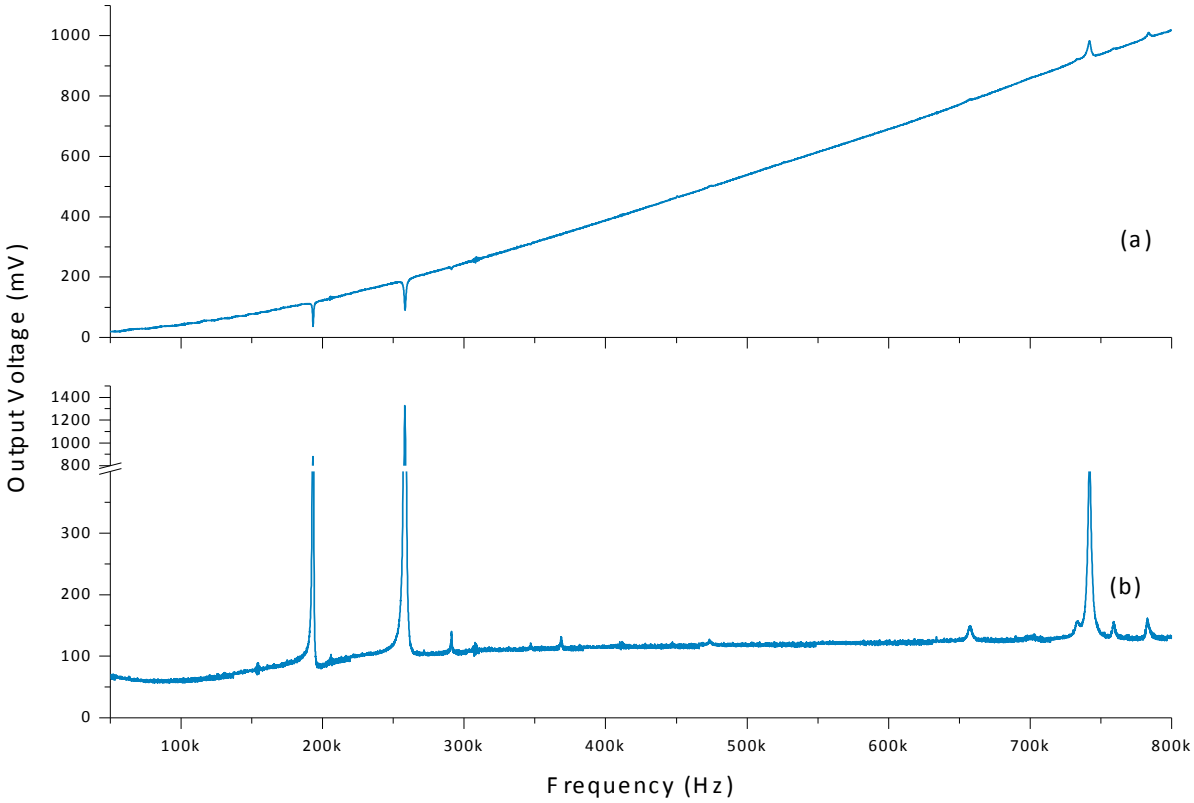


Figure 6: Experimental responses of a piezoelectrically actuated/sensed membrane using (*a*) separated piezo-cells on one membrane for actuation and sensing purposes and (*b*) one single piezo-cell on the membrane balanced with respect to a similar piezo-cell located on a different membrane.

The effect of the mutual capacitance is emphasized by the inverted resonance shapes (Figure 6.a). Once this effect is suppressed by the use of the "mono-piezo-cell" scheme, the dynamic response of the micromembrane becomes Lorentzian-shaped (Figure 6.b).

Making use of the same "mono-piezo-cell" configuration, a clamped-free beam bearing a single piezo-cell for both actuation/sensing purposes (e. g. structure S_3 in Figure S3) was excited using a 40mV voltage. Sensing was done with a piezo-cell reference on a neighboring bridge that was immobilized using a photoresist drop. Three resonant spectra were recorded (Figure 7) with compensation gain values set such that the piezo-cells were either perfectly balanced or up to 3% different.

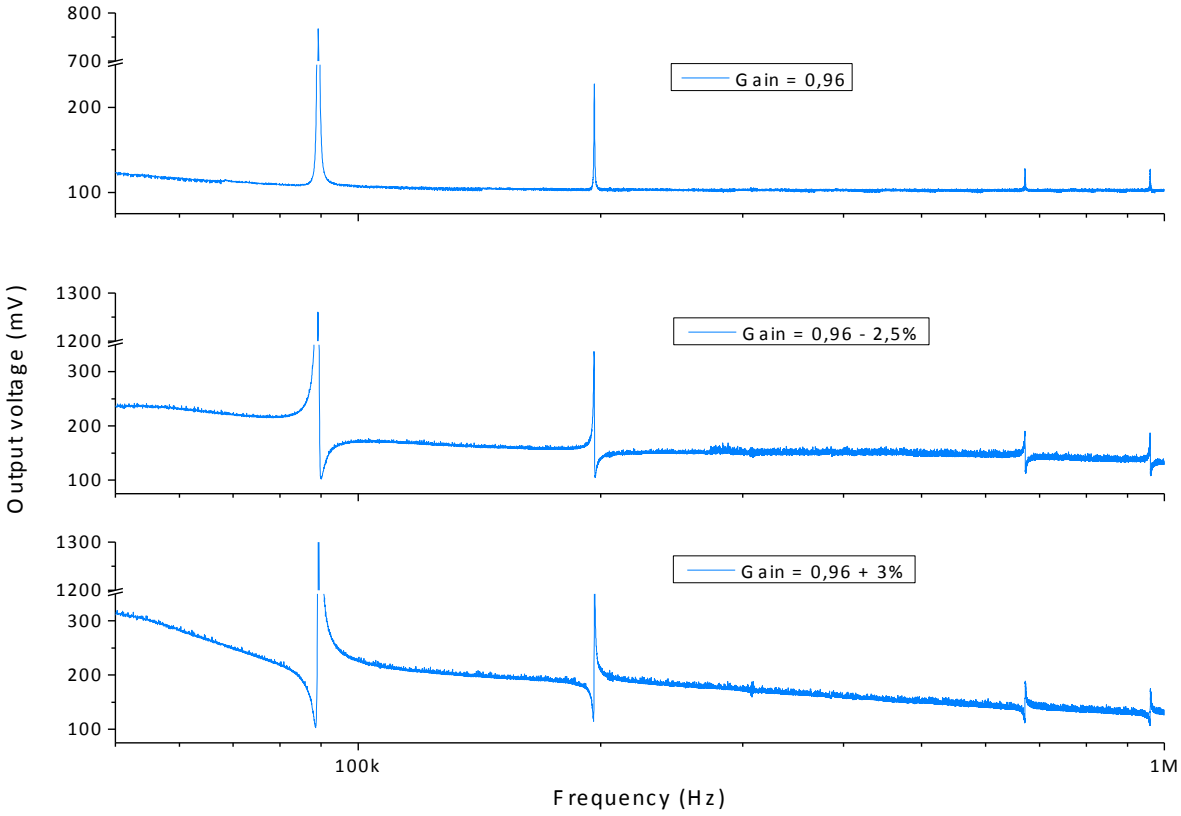


Figure 7: Experimental dynamic responses of a piezoelectrically actuated/sensed cantilever bearing a single piezo-cell. Measurements were performed with respect to a motionless reference piezo-cell by setting gain values used to compensate the differences between the piezo-cells such as they are either up to 3% unbalanced (*b,c*) or perfectly balanced (*a*).

As predicted by the simulations of the mono-piezo-cell configuration, when the gain is set such that both piezo-cells are perfectly compensated, the resonant peaks are close to Lorentzian-shaped dynamic responses. Good agreement is achieved between the experimentally observed changes in the shapes of the resonant peaks and the corresponding simulated behavior (see Figure 4.b). This enables full control of the compensation once the first measurements are collected.

Conclusions

Collective fabrication of different geometries of microresonators (cantilevers, bridges and membranes) bearing piezoelectric film for actuation/sensing purposes on the same wafer has been

done in order to devise design rules that best exploit the capabilities of the integrated piezoelectric thin films, while avoiding parasitic effects inherent to the integration at the micro-scale. Three main parasitic effects, namely the electrical wiring capacitance, the mutual capacitance between actuation/sensing piezo-cells and variations in the capacitance of the actuation/sensing piezo-cells, have been identified, modeled and experimentally investigated. Strategies to minimize their impact on the resonant behavior of the piezo-MEMS were also discussed.

An electrical model of a piezo-cell consisting of piezoelectric thin film sandwiched between two metallic electrodes was considered in order to systematically assess the role of the associated on-chip electrical network. Though this kind of consideration is a basic rule for microelectronics designers, it is often neglected in design of MEMS systems; this, in turn, may induce errors of interpretation of signals from the piezoelectric sensing piezo-cells.

When two independent piezo-cells are co-hosted on the same microscale resonator, mutual capacitance between the piezo-cells induces parasitic effects that influence the net piezo-MEMS electrical behavior. We have proven by simulation that fF-level mutual capacitances may considerably affect the Lorentzian shape of the resonant peaks. It was shown experimentally that on a micromembrane geometry bearing both actuation/sensing piezo-cells, use of a remote, motionless piezo-cell as a reference eliminates this problem.

Finally, the compensation of parasitic effects via a reference, unreleased piezo-cell is effective only if its capacitance value is identical to that of the active piezo-cell. This type of capacitive compensation scheme can be obtained by finely tuning the gain of the amplifier whose output voltage drives the reference piezo-cell.

Hence, it is of paramount importance for MEMS designers to have a holistic approach when dealing with actuation and sensing capabilities integrated at the device level. This is especially true when the measured electrical charge levels reflect the device motion and when the dimensions of the devices are on the micron scale. This kind of considerations will become progressively more important with the development of nano-electromechanical systems integrating actuation/sensing capabilities.

Acknowledgements

This publication was supported by the Pennsylvania State University Materials Research Institute Nanofabrication Lab and the National Science Foundation Cooperative Agreement No. ECS-0335765. The French National Agency for Research (program ANR/PNANO 2008, project NEMSPIEZO ‘‘ANR-08-NANO-015’’) is gratefully acknowledged for financial support.

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