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A new vertical porous stacking structure fabrication process for nanowire/nanotube-based fully-surround gate field effect transistor

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ABSTRACT

A novel vertical nano-porous structure is reported as a starting point for the fabrication of a fully-surround gate field effect transistor (FET) based on well-ordered nanostructures array. The proposed porous stacking is perfectly suited both for the collective organization of nanostructures like nanowires (NWs) or nanotubes (NTs), as high density (up to 10^{11}.cm^{-2}) arrays with calibrated diameters (during growth), as well as for easing the Source, Gate, and Drain electrodes connections for individual or groups of nanostructures. Moreover the unique fully-surround gate architecture enables a quasi-ideal coupling between the gate and the channel, theoretically leading to improved devices performance and reducing the global power consumption.

In this paper we describe the main steps for this versatile and lithography-free technique to fabricate a multi-layer porous template down to the nanometer scale, as well as the first nanostructures (carbon NTs) growth attempts inside such functional template. We highlight the fact that the proposed porous structure acts as a passive template for the growth as well as an active component for the future device.

The proposed approach is in line with bottom-up fabrication approach to provide smaller devices, and is fully-compatible with classical processes used in the silicon industry.

INTRODUCTION

One-dimensional nanostructures have brought a large field of new potentialities in many scientific domains such as microelectronics, photovoltaics, sensing ... Indeed, due to their small dimensions, they exhibit very special particularities that differ from their corresponding bulk materials, and can be used to realize devices with improved properties. Thus, several research groups have realized 1-D nanostructure-based devices like photodetectors [1], [2], FETs [3], [4], solar cells [5], [6], chemical sensors [7], (...) with 1-D nanostructures as building blocks. Despite these promising marches towards nano-devices, it remains a challenging task to combine high density integration and spatial placement control with simple, cost-effective methods.

In the case of NW-based transistors, devices with a planar geometry have been widely presented, but these approaches generally don't make the high-density integration easy. Moreover, the manipulation, orientation and the NWs location definition require time consuming and/or heavy means like dispersion and alignment [8], controlled deposition of colloids [9], [10] or e-beam lithography [11] to finally realize the transistor. Furthermore, the conventional planar transistor configuration may suffer from a poor gate coupling, leading to insufficient electrostatic

efficiency and thus to non-optimized power consumption [12], [13]. The tri-gate transistor [14] and the semi-gate around structure [15] are some of the solutions proposed to improve this coupling. As a natural continuation, a fully-surrounding gate, brought by the vertical geometry of the PAA, proved to provide a quasi-ideal gate coupling [10].

In this paper we demonstrate a simple and reliable method to achieve simultaneously good location control, high density and surrounding gate structure in a NW/NT-based FET, according to the description made in [16]. Using a Porous Anodic Alumina layer as a hard-mask for several successive anisotropic etching steps, we have been able to realize a completely vertical porous structure well-designed to receive vertical 1-D nanostructures. The use of the three-dimensional configuration leads to a more dense transistors array, while the packed, well-organized and tunable structure of the pores provides a good control over the location and geometry of the nanostructures. The nanostructures growth being guided by the porous stacking, an intrinsically-designed surrounding gate allows a good gate-coupling efficiency.

EXPERIMENTAL DETAILS

All the physical characterizations have been done with a Hitachi S-4800 Scanning Electron Microscope.

Porous stacking

As a starting point for the fabrication of vertical NW/NT-based FET, we started from a multi-layer configuration, as depicted in figure 1. The stack consists in an alternation of conductive and insulating layers, namely highly-doped (10^{16} - 10^{17} .cm⁻³) p-type Si substrate, thermal SiO₂, e-beam evaporated Al and porous anodic alumina (PAA).

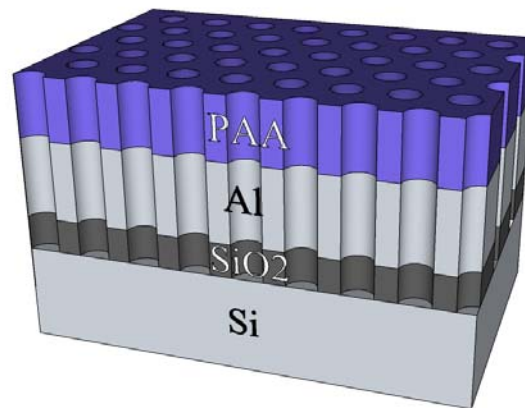


Figure 1. Schematic representation of the porous stacking.

The PAA was realized using 0.3M H₂SO₄ solution and according to the two-step anodization method used in [17], firstly described by Masuda and Fukuda [18]. In our particular case, the anodization of the Al layer is partial, in order to keep a pure Al layer as the future gate between the PAA and the SiO₂ layer. At the end of the anodization, the pores are very narrow and a barrier layer is still present at the bottom of each of them. The sample is therefore immersed in a 0.3M ortho-phosphoric acid (H₃PO₄) solution for 15 min at 30°C in order to

remove this alumina barrier layer which would have been problematic for the subsequent step of the fabrication of the stacking. This wet etching is isotropic and thus inevitably leads to an enlargement of the pores; as can be seen in figure 2, the pores in the PAA have a mean diameter of 35 nm at the end of this step.

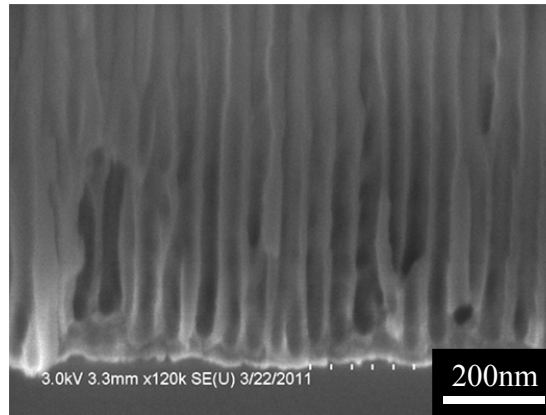


Figure 2. High-magnification of the alumina pores after the pore widening process

In order to achieve the complete porous structure shown in figure 1, we performed two consecutive selective Reactive Ion Etching (RIE) steps using an Inductively Coupled Plasma (ICP) reactor, which is known to provide high-density plasmas. The conditions are listed in Table I.

Table I. Etching conditions for both Al and SiO₂ ICP Reactive Ion Etchings.

	Al etching	SiO₂ etching
Platen/Coil power (W)	240/95	150/300
Pressure (mTorr)	3	4
Gas ratio (sccm)	Ar/Cl ₂ = 8:4	CHF ₃ :SF ₆ :O ₂ = 100:5:2
Etching duration (min)	3	3.5

Electrodeposition

In order to grow NWs/NTs inside the pores, we need to deposit catalysts at the bottom of each pore. In the case of CNT growth, nickel has been chosen as it is known to alloy easily with carbon and has been successfully electrodeposited in PAA since a long time in our team. To that point we performed pulsed electrodeposition (PED) with the acidic nickel aqueous solution commonly called Watts bath. The sample is dipped inside the solution and several -5.5V pulses are applied between the sample and a graphite counter-electrode in order to reduce the Ni²⁺ ions at the bottom of the pores.

Growth

To perform the CNT growths, we used a home-made catalytic Hot-Wire CVD system, supplied with both methane and hydrogen, similar to the one described in [19]. The samples are introduced inside of a quartz furnace surrounded by heating elements. In order to deoxidize the

catalysts and clean the surface of the sample, the latter was exposed to atomic hydrogen for 5 min, provided by the passage of H₂ through a tungsten hot wire, heated up to 1800°C. For further details on the growths conditions, see table II.

Table II. Growth conditions for CNTs inside our tubular quartz furnace.

Growth temperature	600°C
Pressure	95 mbar
Gas ratio	H ₂ :CH ₄ = 50:50 sccm
Hot wire temperature	1800°C
Growth duration	2'20

RESULTS AND DISCUSSION

For use as a vertical FET, the structure described above will act as follows: the highly-doped substrate will be acting as one of the Source/Drain electrodes, while the other S/D electrode (typically Au) can be evaporated and patterned onto the top of the structure once the NW/NT growth is done inside the pores and the NW/NT emerge at the surface of the stacking. Thus the Al layer will play the role of an individual surrounding gate for each NW/NT, the gate oxide being inevitably present on the inner surface of the Al pores (Al native oxide or subsequent thermally grown oxide). Both PAA and SiO₂ layers will prevent parasitic leakages between the electrodes.

One has to note that such a structure can be almost entirely tailored, since everything is realized from the PAA, which dimensions are easily tunable. Indeed, the pores diameter is controlled through the anodization voltage while the Al and PAA thicknesses are related respectively to the first anodization duration and the second anodization duration. The thickness of the SiO₂ layer is controlled for example by the oxidation of the Si substrate. As a first proof of concept, we chose to set on a hundred of nanometers thickness for every layer of our structure, these thicknesses being easily adjustable if later required. It is important to anticipate the inevitable and non-negligeable thinning of the PAA during the two RIE steps due to the ion bombardment, and thus to realize a thicker PAA than the final desired thickness. In our case, the PAA thickness decreased from about 300 nm down to 100 nm during the two RIE steps.

The etching step of the Al layer implies chlorine (Cl₂) and argon (Ar), according to the conditions listed in Table I, and an optimized gas ratio has been used [20] in order to preserve the straight feature of the pores. This etching thus provides a well-defined replica of the PAA, with straight pores having a mean diameter of 35 nm as well. Subsequently, we performed the second RIE step, using a combination of fluor-based gases, which etches SiO₂ much faster than Cl₂ does [21], and provides a Bosch-like etching process [22]. The final result is visible in figure 3.

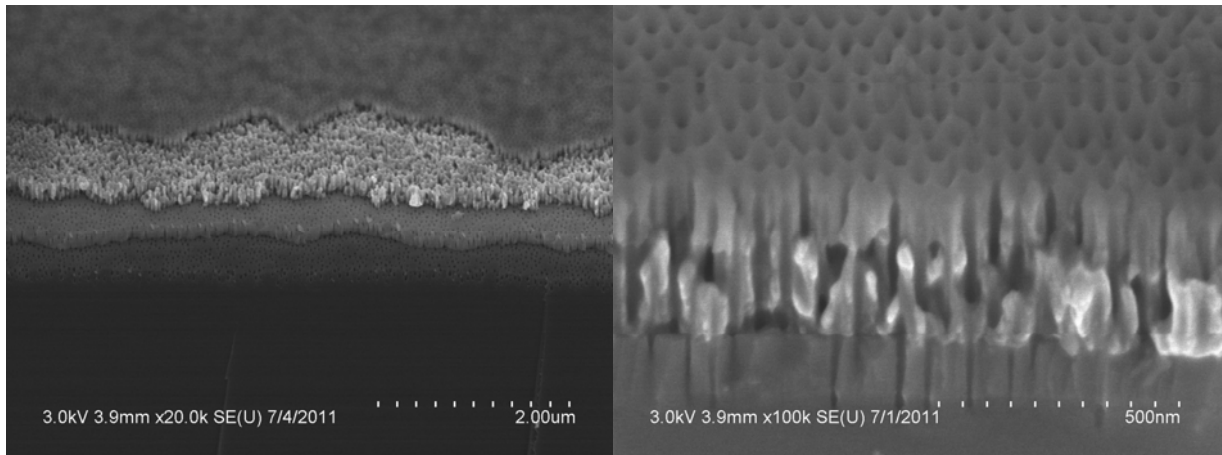


Figure 3. Low (a) and high (b) magnification of the porous stacking after the two ICP Reactive Ion Etchings.

To grow nanostructures from a vapor phase, the catalytic metals that are deposited at the bottom of the pores must be able to form a stable alloy with the material we want to grow. For SiNW growth, gold is typically chosen because of the low eutectic temperature of the Au-Si system, but a lot of other metals can be also used, like Cu [23] or Al [24]. For CNT growth, we chose Ni as a catalyst, but Fe or Co are also widely used. Pulsed electrodeposition (PED) has been chosen as a method to deposit the catalysts because of its easy control over deposition rate [25]. Figure 4 shows the stacking after Ni electrodeposition. Fortunately, on this very particular sample the top and the sides of the three different porous layers are clearly visible, showing the Ni particles deposited on the Si substrate (bright spots).

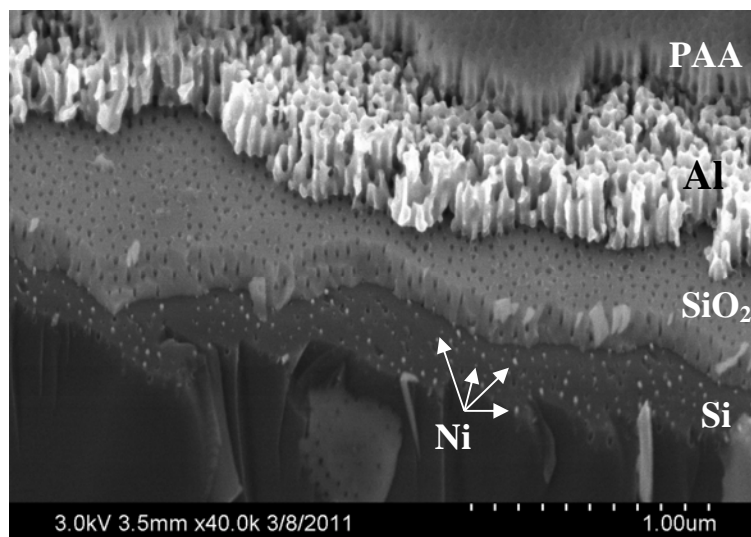


Figure 4. Cross section of the porous stacking after the Ni electrodeposition process. Ni particles appear in bright onto the Si substrate at the bottom of the image.

After the proof of concept described elsewhere [19], consisting in growing SiNWs inside PAA on Si substrate, another challenge is to grow them inside the complete stacking, which is the next step in the fabrication process of the nanostructure-based vertical FET. Nevertheless we

couldn't deposit gold or copper as successfully as we did with Ni, the main difficulties we encountered being inhomogeneity and surface catalysts deposition. Therefore we first tried to grow CNTs, starting from the Ni electrodeposition results shown above. Based on the CNT growth conditions optimization achieved before [26], we determined correct growth duration to observe CNTs protruding out of the porous stacking (see figure 5).

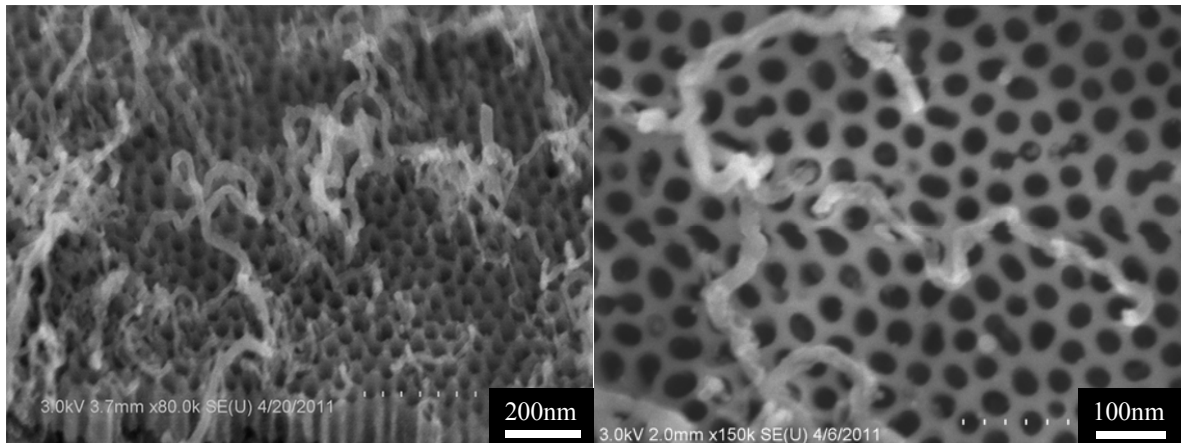


Figure 5. Tilted (a) and top view (b) of the porous stacking after the CNT growth, performed in the conditions listed in Table II.

Two minutes and twenty seconds appeared to be suitable for this, but it is relevant to add that a 1 min growth was not long enough to see anything protrude out of the PAA. We think this is to be related to two mechanisms. First, given the growth temperature that we used and the eutectic temperature of the C-Ni phase diagram (around 1326°C), the Vapor-Solid-Solid (VSS) mechanism is very likely to rule the CNT growth. According to this mechanism, the carbon atoms have to diffuse through Ni particles, which become saturated to finally allow carbon to precipitate and the CNT to grow. This corresponds to an incubation time. Besides, because the catalyst is confined inside the pore, the surface exposed to gases is much more limited than in the classical free surface growth and so the growth rate is slow.

As a reference, we also introduced a sample with no catalyst during a 15 min growth. While the catalyst-filled showed to be quite covered with a large amount of CNTs, no CNT was visible on the sample with no catalyst. This proves that the CNTs definitely grew from the Ni particles deposited beforehand at the bottom of the pores, and that no parasitic growth (from impurities) occur during this process.

CONCLUSIONS

For the first time we report the fabrication of a complete porous structure designed for the integration of a large array of 1-D nanostructure-based vertical FETs, in a very good reproducible way. Though no evidence of electronic device has been supplied, a proof of concept is reported with the growth of CNTs inside the porous template. These results have nevertheless to be extended to SiNW growth, most promising for electronic devices due to their semi-conducting behavior that our CNTs may not show. This will be attempted when Au or Cu electrodeposition is better controlled, especially with samples with no parasitic catalyst surface deposition.

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