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Umesh Kumar Bhaskar, Thomas Pardoen, Vikram Passi, et al.



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Piezoresistance of nano-scale silicon up to 2 GPa in tension

Umesh Kumar Bhaskar,^{1,a)} Thomas Pardoën,² Vikram Passi,³ and Jean-Pierre Raskin¹

¹*Institute of Information and Communication Technologies, Electronics and Applied Mathematics, Université catholique de Louvain, B-1348 Louvain-la-Neuve, Belgium*

²*Institute of Mechanics, Materials and Civil Engineering, Université catholique de Louvain, B-1348 Louvain-la-Neuve, Belgium*

³*Institut d'Electronique, de Microélectronique et de Nanotechnologie IEMN-UMR CNRS 8520, Lille, France*

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The piezo-resistance of 100 nm-thick, [110] oriented, p-type, mono-crystalline Si beams has been investigated under large uniaxial tension up to 2 GPa using an original on-chip tensile testing set-up. The piezo-resistance coefficient (π) was found to increase by a factor of 6 compared with ~ 1.5 for Si bulk, when decreasing the dopant concentration from $N_a \sim 1 \times 10^{19} \text{ cm}^{-3}$ down to $N_a \sim 5 \times 10^{17} \text{ cm}^{-3}$. Reduction of resistance by a factor of 5.8, higher than theoretical maximum of 4.5, is reported for $N_a \sim 5 \times 10^{17} \text{ cm}^{-3}$ under a stress of 1.7 GPa, without any sign of saturation.

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Piezo-resistance (π) is the change in resistance of a crystal upon mechanical deformation. In Si, it primarily originates from a strain induced alteration of the crystal symmetry and electronic band structure.¹⁻⁴ For example, the application of an uniaxial stress along the $\langle 110 \rangle$ direction reduces the original cubic crystal symmetry to orthorhombic symmetry.⁵ This reduction of the symmetry has a pronounced effect on the valence band edge, where the original degeneracy is lifted and split into two distinct heavy hole (HH) and light hole (LH) bands. There is also a significant warping of the energy bands away from the band edge. Since the inverse effective mass ($1/m^*$) of the carriers is determined by the curvature of the band close to the band edge; the strain induced band splitting and warping influences the hole transport properties primarily through a change in m^* .^{5,6}

The π values for bulk Si have been extensively studied at low applied deformation, and shown to vary with orientation,³ impurity concentrations (N_a),⁷ temperature,⁸ and the magnitude of loading.^{9,10} These studies contributed to the micro-electro-mechanical systems (MEMS) revolution making Si piezo-resistors the first integrated electromechanical transducer.¹¹ However, these characterizations were primarily limited by the brittleness of Si exhibiting fracture stress below 300 MPa.

Strain engineering of Si, which aims at enhancing the mobility of charge carriers through controlled deformation of the crystal lattice, has made piezo-resistive research at high applied loads technologically pivotal to the metal oxide semiconductor field effect transistors (MOSFETs) industry.^{12,13} Theoretically,^{5,6} deformation has the potential to increase the mobility (quantified approximately by R_0/R , where R_0 and R are the resistance of the original and deformed crystal respectively), by a factor up to ~ 4.5 in p-channel MOSFETs, and up to ~ 2 in n-channel MOSFETs. These predictions and related experimental works^{14,15} are usually carried out on 2 dimensional inversion layers of holes and electrons in MOSFETs, and is expected to be

lower than for bulk volumetric transport. In a recent study,¹⁶ a strain induced enhancement of $\sim R_0/R$ above theoretical expectations, up to 6.5, without any sign of saturation, was demonstrated on p-type bulk Si wafer under compressive stresses up to 3 GPa.

Si nano-wires (SiNWs) are promising candidates for the next generation of transistors.¹⁷ It has been confirmed theoretically¹⁸ and experimentally¹⁹ that the strain induced enhancement of mobility can be sustained in SiNW transistors. Deformation additionally has the potential to tune SiNW properties as needed for electro-optic²⁰ and photovoltaic²¹ applications. For small diameter SiNWs, a mechanical deformation can be used to reversibly alter the nature of the band-gap from direct to indirect.²²

The high surface to volume ratio of SiNWs makes them also susceptible to surface effects. The interplay between mechanical deformation, surface, and confinement effects could lead to distinct physical phenomena, like for example the demonstration of giant piezo-resistance in suspended SiNWs.²³ In the work by He *et al.*,²³ the piezo-resistivity coefficients (π) of SiNWs were up to two orders of magnitude larger than the expected bulk values, increasing with decreasing SiNW diameter and decreasing N_a . Furthermore, π was sensitive to the surface charge density, through the resulting SiNW space charge region. A hydrofluoric acid (HF)-treatment was found to enhance the value of π , conceivably through the increase of depletion region in the SiNW. The results of He *et al.*²³ and the giant piezo-resistance effect observed in SiNWs were postulated to be a stress induced modulation of the effective width of the SiNW.²⁴ This explanation was supported by the demonstration that π in SiNW could indeed be modulated by up to two orders in magnitude through electrostatic control of the SiNW depletion region.²⁵ However, there are suggestions²⁶ that fluctuations in the SiNW resistance resulting from surface state charge trapping/de-trapping processes could be mis-interpreted as giant piezo-resistance. In a related study, a two fold increase of π was observed for suspended SiNWs²⁷ in comparison with their non-suspended counterparts. These results suggest that the piezo-resistive behavior

^{a)} Author to whom correspondence should be addressed. Electronic mail: umesh.bhaskar@uclouvain.be.

of free-standing structures could be superior to structures under the constraint of the substrate. Only recently, the piezo-resistive properties of [111] oriented p-type SiNWs at large deformations have been explored and anomalous effects have been reported.²⁸ There are thus both fundamental and technological interests in investigating the hole mobility of SiNWs at varying levels of applied deformations.

In this study, [110] oriented p-type Si nano-beams with N_a ranging from 1×10^{16} to $1 \times 10^{19} \text{ cm}^{-3}$ fabricated top down using 100 nm-thick silicon-on-insulator (SOI) wafers have been used to explore the piezo-resistive properties of Si nanostructures up to large deformations. One major challenge for this study is the development of an original on-chip setup²⁹ sufficiently equipped to deform freestanding Si beams up to fracture, while simultaneously permitting investigation of the carrier transport under large lattice deformation. Transport measurements are reported for uniaxial tension up to 2 GPa, limited by fracture in the beams. The conductivity was observed to decrease with an increase in applied tension for all studied N_a . The width of the nano-beams currently used in this work is $2 \mu\text{m}$, and hence, limits direct comparisons with existing results on SiNWs. However, the technique can be extended to the study of nanometer wide beams,³⁰ where applied deformations up to 5% can be achieved.

The mechanical testing technique, as shown in Figure 1(a), relies on a structure made of two beams: a loop-shaped cantilever beam made of single crystal Si sharing a partial overlap with a stiffer cantilever beam of silicon-nitride (SiN). Large internal stresses are present in the SiN beam originating from deposition. The essential idea is to use the displacement induced upon release, owing to internal stress relaxation in the SiN beam, to mechanically deform the attached Si beam.³¹ The two silicon beams forming the loop have anchor pads which are isolated from one another. These regions are heavily p-doped for the realization of Ohmic contacts. An aluminum layer is deposited, on the silicon anchor pads and annealed to form the source and drain terminal. As shown in Figure 1(a), the magnitude of the strain ($\xi = u/L$) imposed on each Si

beam is directly inferred from measuring the displacement u of the released beams using a scanning electron microscope (SEM) and by prior knowledge of the length L of the Si beam. The accuracy³² on the imposed strain is estimated to be less than 0.03%. The strain is transformed into a stress by using the bulk Young's modulus value of 169 GPa. The HF release of the Si beams results in a high transient surface charge density $>10^{13} \text{ cm}^{-2}$. As a consequence, transport characterizations reported in this paper were made at least two weeks after release to allow the dissipation of the transient surface charges and the regrowth of a stable native oxide, as reported in Ref. 33.

For analysis, the resistances of free cantilevers, and specially designed clamp-clamp cantilever beams fabricated with the same geometry, constitute the "un-stressed" resistance measurements. This measured resistance is compared with the resistance of deformed cantilever beams. The validity of this assumption relies on uniformity of the geometry, and conformity of the surface potential of the beams owing to identical condition of fabrication and surface preparation.

Every individual test structure of Figure 1(a) provides a unique $I_d - V_d$ curve with the inverse of the slope corresponding to the resistance at a given deformation. As seen in Figure 1(b), by creating an array of tensile test structures with increasing length of the SiN beam, the $I_d - V_d$ characteristics can be measured for a range of applied deformation up to fracture. Figure 2(a) plots the output characteristics ($I_d - V_d$) measured for an array of test structures with applied stress ranging from ~ 0.2 to 1.5 GPa. This specific structure is a 100 nm-thick, $2 \mu\text{m}$ -wide, and $200 \mu\text{m}$ -long Si beam with $N_a \sim 5 \times 10^{18} \text{ cm}^{-3}$. The π measurement for any given geometry is an average of measurements over two mutually opposite parallel array of structures.³¹ This eliminates or, at least, minimizes the effect of any unsolicited dispersion arising from process variation or other in-correlations on the measured π .

Figure 2(b) summarizes the change in resistance ($\delta R/R_o$) extracted for Si beams with $N_a \sim 1 \times 10^{19} \text{ cm}^{-3}$ as a function of the applied stress. Figure 3(a) compares the ($\delta R/R_o$) as a function of the imposed stress extracted for

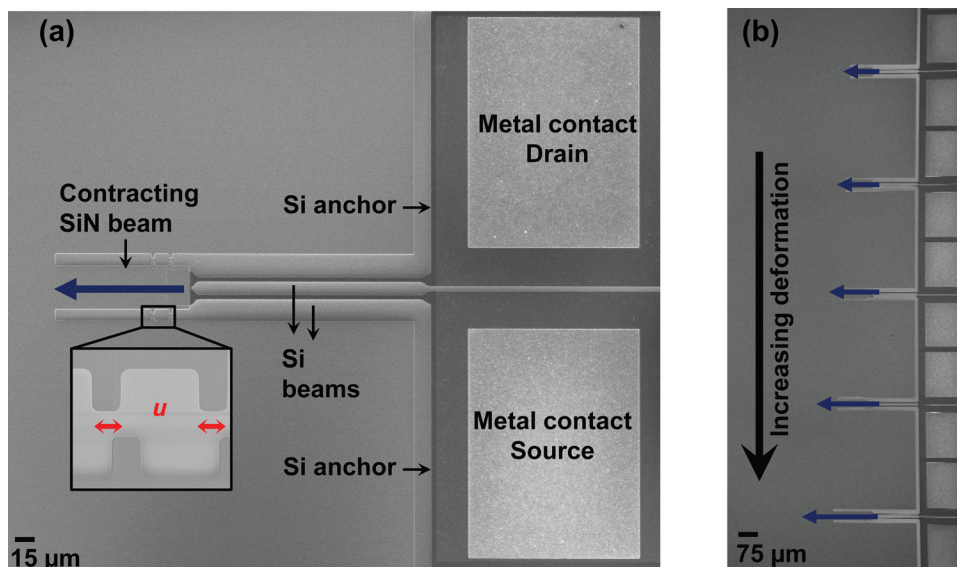


FIG. 1. SEM images of (a) elementary test structure for electro-mechanical characterization of Si nano beams; and (b) an array of elementary test structures with increasing tensile deformation.

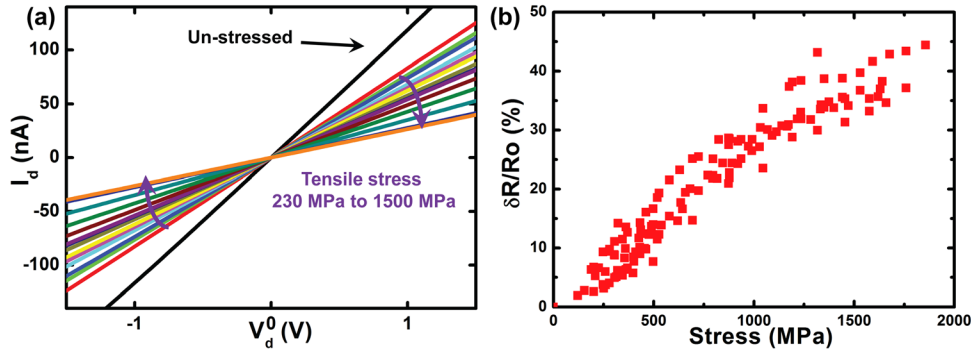


FIG. 2. (a) Output characteristics $I_d - V_d$ for a series of tensile test structures of 100 nm-thick, 2 μm -wide, and 200 μm -long Si geometry with $N_a \sim 5 \times 10^{18} \text{ cm}^{-3}$; (b) Normalized stress induced change in resistance ($\delta R/R_0$) for Si beams, with $N_a \sim 1 \times 10^{19} \text{ cm}^{-3}$ as a function of the tensile stress.

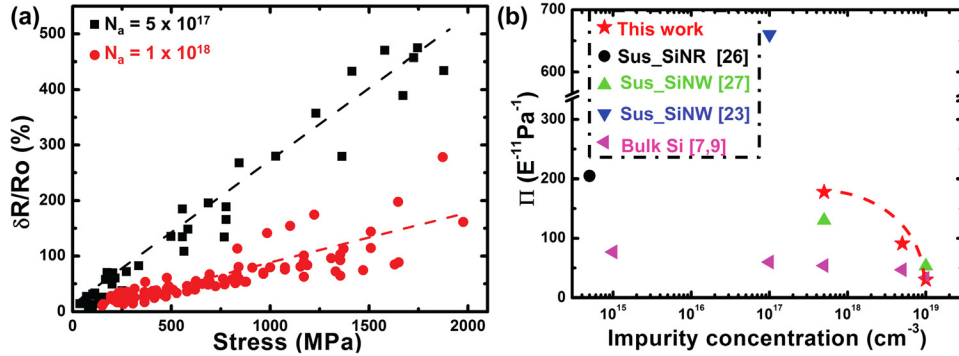


FIG. 3. (a) $\delta R/R_0$ for Si beams with $N_a \sim 1 \times 10^{18}$ and $N_a \sim 5 \times 10^{17} \text{ cm}^{-3}$ as a function of the tensile stress; (b) Comparison of extracted π values with literature on [110] oriented SiNWs and (bulk) Si.

$N_a \sim 1 \times 10^{18}$ and $\sim 5 \times 10^{17} \text{ cm}^{-3}$. The maximum stress induced resistance reduction factor (R/R_0) is summarized in Table I. The modulation of the resistance by a factor of 5.8 for $N_a \sim 5 \times 10^{17} \text{ cm}^{-3}$ is significantly larger than the factor of ~ 4.5 predicted for hole inversion layers.⁵ In addition to the change in m^* , there can also be contribution to δR originating from the modification of carrier mean free path in the deformed crystal. However, since the applied deformation results in a reduction of states at the band edge, it should be expected to increase the carrier mean path and hence, lead to a decrease of the resistivity. This makes the observed continuous increase in resistance with uniaxial tension even more surprising. Qualitatively our results are in support of recent results reported for (110) bulk Si¹⁶ with $N_a \sim 1 \times 10^{16} \text{ cm}^{-3}$. In this study,¹⁶ the resistance measured under 3 GPa of compressive stress was 6.5 times smaller than the “un-stressed” resistance.

Figure 3(b) presents the comparison of extracted π values from our Si suspended beams with literature results on [110] oriented bulk Si and suspended SiNWs. For $N_a \sim 1 \times 10^{19} \text{ cm}^{-3}$, the π value extracted in this study is $\sim 18\%$ and 12% smaller than the value for bulk Si⁷ and for SiNW transistors,¹⁹ respectively. The extracted π was also compared with recent work on top down fabricated [110] oriented

SiNWs²⁷ with the same N_a to reveal that our values are lower (-20%) than and close ($+5\%$) to the values reported on suspended and un-suspended SiNWs, respectively. For $N_a \sim 5 \times 10^{18}$ and $N_a \sim 5 \times 10^{17} \text{ cm}^{-3}$, the extracted π value is $\sim 48\%$ and 66% larger than that of bulk Si. In comparison to SiNWs²⁷ with $N_a \sim 5 \times 10^{17} \text{ cm}^{-3}$, the π values extracted in this study are 20% larger. A large discrepancy (-370%) is observed when comparing the present results, with the work on bottom-up grown, [111] oriented, suspended SiNWs²³ with $N_a \sim 1 \times 10^{17} \text{ cm}^{-3}$.

The results of Table I show that the effect of the stress on both R/R_0 and π decreases with increasing N_a . In contrast to transport in the bulk of a Si crystal, where the effective carrier concentration p is a constant determined by N_a , in the case of MOSFETs, Si thin films and SiNWs, p can be varied through the application of an electrostatic potential at the surface. Surface states³⁴ ensure that there is always an electrostatic potential at the surface. The extent of the resulting space charge region will, however, depend on N_a . A moderate positive surface charge density $N_{it} = 5 \times 10^{11} \text{ cm}^{-2}$ at the native oxide interface would give rise to a negligible total depletion length of $2 \times 0.1 \text{ nm}$ for $N_a \sim 1 \times 10^{19} \text{ cm}^{-3}$. The factor 2 is needed to take into account depletion from both the top and bottom interfaces. For this N_a value, the total depletion region would be negligible, about 0.2% of the total Si film thickness. This could explain that the value of π is comparable with the case of bulk Si. However, for the same N_{it} , the total depletion region would be 10% and the 50% of the Si film thickness for $N_a \sim 1 \times 10^{18}$ and $N_a \sim 5 \times 10^{17} \text{ cm}^{-3}$, respectively. This could be a reason for the enhanced influence of stress on π and R/R_0 . Indeed, the stress induced modulation of SiNW depletion length²⁴ is considered to cause the significant enhancement observed by Refs. 23 and 25 in “fully depleted” SiNWs. Several factors like the intensity of applied load, magnitude of enhancement (few folds in this study), and geometry

TABLE I. Influence of the stress on R/R_0 and π tabulated for different dopant population N_a .

N_a (cm^{-3})	R/R_0	π (10^{-11} Pa^{-1})	Deviation of π from bulk Si ⁷ (%)
1×10^{19}	1.44 at 1.8 GPa	29.2 ± 1	-18
5×10^{18}	3.8 at 1.8 GPa	90.6 ± 4	+48
5×10^{17}	5.8 at 1.8 GPa	177.8 ± 6	+66

(2 μm -wide beams) limit direct comparisons with the two orders enhancement reported for <100 nm-wide SiNWs²³ at very low applied stresses.

In summary, a simple on-chip tensile testing setup allowing electro-mechanical characterization of nano-scale semiconductors has been used to test 100 nm-thick Si beams and to measure the evolution of π and R/R_0 with N_a . Significant reduction of the mobility, higher than existing theoretical prediction, up to a factor of 5.8 is reported for $\sim 5 \times 10^{17} \text{ cm}^{-3}$, at 1.7 GPa. The extracted π increases by a factor of six when decreasing N_a from $\sim 1 \times 10^{19}$ down to $\sim 5 \times 10^{17} \text{ cm}^{-3}$. The results suggest that significant strain induced mobility enhancement could be potentially achieved for lowly-doped nano-scale devices.

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