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Ta/TiN midgap full-metal single gate fabrication using combined chlorine-based plasma and highly selective chemical metal etching for decananometer CMOS technology

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A B S T R A C T

High permittivity dielectric and metal gate are now the most demanded in advanced CMOS technology to overcome conventional polysilicon gate structure drawbacks. However, existing metal gate fabrication approaches are not capable to meet all the demands in terms of material engineering or fabrication process. In this study, we present a two-step dry and wet etching strategy for the integration of tantalum and titanium nitride full-metal single gate, which offers a perfect vertical, roughness-free sidewall and an ultra high metal/dielectric etch rate selectivity.

Keywords:

Full-metal single midgap gate
Combined RIE/highly selective chemical etching process

1. Introduction

In the relentless quest to downscaling of MOSFETs transistors, novel devices that hierarchically combine alternative materials and new architecture concepts are the object of intensive research. In particular, high permittivity dielectric and metal gate are now widely implemented in advanced CMOS technology to overcome two major limitations, namely, gate leakage on one side, as well as polysilicon gate depletion, boron diffusion and prohibitive gate resistance, on the other side [1]. Several existing metal gate fabrication schemes like fully-silicide (FUSI) [2] or dual metal gates [3] intend to satisfy this demand. However, the former suffers from poor thermal stability and dopant penetration while the latter implies complex material compatibility issues to mitigate. A large majority of metal gate integration schemes resort to the deposition of a thin metal layer with desired workfunction capped by a thick degenerately doped polysilicon layer [4] that facilitate gate patterning by reusing reference etch recipes. Although this strategy solves the depletion problem, it does neither tackle the resistivity limitation of polysilicon gate nor does it address the interface resistance with the capping silicide layer that severely limits high frequency operation [5]. In that context, the integration of a full metal gate naturally emerges as the ideal option which is, however, hindered by difficult problems associated to low etching selectivity with respect to the photoresist mask and underlying dielectric materials [6]. Furthermore, metal etching also raises other challenges due to the generation of non volatile residues, anomalous

edge roughening and notching [7,8]. In this paper, a two-step dry and wet etching strategy that produces vertical roughness-free sidewalls and features an ultra high etch rate selectivity (>500) between the metal and the oxide is demonstrated. For that sake, a gate stack comprising a thick Ta capping layer on top of a thin TiN coat is used. Here, TiN serves as midgap workfunction metal [9,10] where its advantages and utilities are explained in Ref. [11]. While the thick Ta cap is seamlessly etched by reactive ion etching (RIE), the underlying TiN is finely removed by controlled wet stripping.

2. Experimental procedures

Initially, a 2.2 nm SiO₂ gate oxide was grown by dry oxidation at 725 °C on a (100) silicon wafer. The wafer cleaning, preparation and thermal oxidation was mentioned in ref. [12]. For alternative high-*k* dielectric samples, 3 nm aluminum oxide (Al₂O₃) is deposited thermally at 300 °C by Atomic Layer Deposition (Beneq TFS200). The metal gate stack (a 10 nm thick TiN then a 140 nm thick Ta cap layer) was subsequently deposited by magnetron cathode sputtering using Ar sputtering gas in 300 W RF(13.56 MHz) source at low pressure (0.002 mbar). Here low pressure prevents the formation of large metal grains which can potentially result in anomalous gate sidewall roughness. Finally, a 100 nm thick SiN hard-mask (HM) was deposited by plasma enhanced chemical vapor deposition (PECVD) at 300 °C followed by the spin-coating of a 200 nm thick inorganic negative-tone electron-beam resist hydrogen silsesquioxane (HSQ) by Dow Corning referred to as FOX-16 on the top at a speed of 5000 rpm for 60 s and baked on a hot plate at 90 °C for 4 min. Gate finger imprints of various lengths (25, 50, 75 and 100 nm) were then defined by

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electron-beam lithography (LEICA EBPG 5000+) at high acceleration voltage (100 kV) and small beam current (300 pA) followed by a development in 25% tetra-methyl ammonium hydroxide (TMAH) solution for 3 min, rinsed in de-ionized water and blown dry by nitrogen.

First, reactive ion etching (RIE) based on a SF_6/Ar chemistry was optimized to transfer the HSQ gate pattern into the SiN HM with near perfect vertical sidewalls measured at 88° with respect to the top surface (Fig. 1). It is worth noting that the SiN HM finds its utility in avoiding anomalous gate sidewall roughness effects as exemplified in Fig. 2. Secondly, the SiN gate fingers were transferred into the Ta layer using chlorine-based ($Cl_2 + SiCl_4$) RIE with optimized parameters (Fig. 3) (low-pressure as 3 mTorr, high-power to 150 W, Ar-assisted) to achieve an 85° anisotropic sidewall profile for 150 nm-thick gate stack. To avoid critical end-point onto the thin gate oxide, etching was stopped in the middle of 10 nm TiN layer, leaving the onset of an isotropic profile which is subsequently rectified using a highly selective and isotropic chemical etching step in a sulfuric peroxide mixture (SPM- H_2SO_4 96%: H_2O_2 30%, 3:1). The solution composition was tuned to complete TiN etching and to ensure soft landing on the underlying gate dielectric. Using this strategy, the final TiN gate length can be accurately controlled by modulating the SPM etching time at a rate of 1 nm/s (Fig. 4). Lastly, uncovered SiO_2 was removed by a Fluoride Acid (HF 1%) dip for 30 s (Fig. 5). (Identical step is carried out to remove our high- k dielectric since Al_2O_3 can be etched at a rate of 50 nm/s in 1% HF while remaining resistant to our SPM solution.)

3. Results and discussion

3.1. Silicon nitride hard mask effect

The presence of a silicon nitride hard-mask during plasma etching eliminates three major drawbacks identified as (i) significant deviation from the designed critical dimension (CD), (ii) tapered

profile of gate fingers and (iii) anomalous line edge roughness (ALER) along the grain boundary [13]. To better understand the utility of the hard mask, gate patterning has been carried out on identical sputtered metal stacks using the same etching condition with sample I using HSQ as metal-etch mask while sample II integrates a SiN hard-mask instead (Fig. 2). HSQ-masked samples exhibit a severe mask deformation which not only leads to a severe degradation of the designed gate dimension (e.g. $1.5\times$ and $0.5\times$ larger for 20 and 100 nm gate fingers, respectively) but also dramatic anisotropy. In contrast, SiN-masked samples show good preservation of the original patterned mask and design dimension along the whole stack depth. In terms of gate line edge roughness, SiN HM samples show perfect roughness-free sidewalls while HSQ-masked samples exhibit prohibitively rough sidewalls. Line deformation of HSQ-masked samples can be explained by the formation and redeposition of non-volatile etching by-products such as tantalum-oxide (Ta_2O_5) or Ta-oxygen-halogen during plasma etching, keeping mind that HSQ constitutes the source of oxygen that leads to the oxidation reaction. It is worth mentioning that its Gibbs free energy of formation (-1911 kJ/mol) indicates Ta_2O_5 forms spontaneously from elemental tantalum and oxygen [7]. A similar justification holds to explain the anomalous line edge roughness phenomenon for HSQ-masked samples, which is due to excessive formation and redeposition of tantalum-oxide etching by-products while for SiN-HM samples, HSQ is also partially etched after SiN etching. For most of the time associated to SiN etching, oxygen-containing by-products are therefore evacuated before being in contact with the underlying Ta layer. We conclude that Ta is much more exposed to oxygen for samples that do not integrate a SiN HM. Besides Ta oxidation in the course of the etching step, Shin et al. [14] suggested that a superficial thin Ta_2O_5 layer is also likely to grow after Ta deposition and exposure to ambient air. In the present study, this effect is expected to take place as the recorded Ta-etching time is relatively long (~ 4 min for 140 nm thick Ta). This constitutes a clue that pleads for depositing a SiN hard-mask layer immediately after metal sputtering, to protect the metal sur-

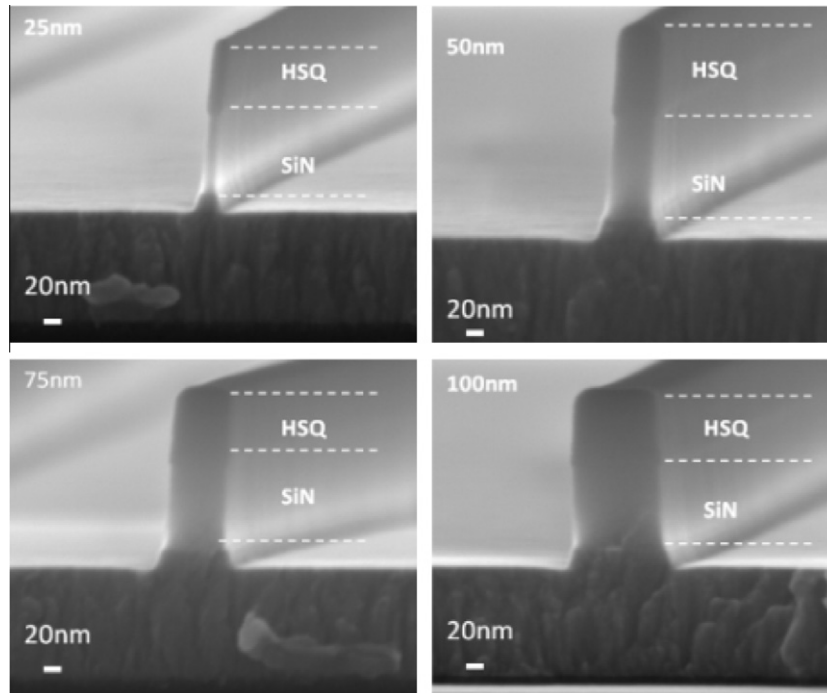


Fig. 1. SEM cross section of a slightly over-etched 100 nm-thick SiN HM resulting from an optimized SF_6/Ar chemistry RIE etching for different gate lengths ranging from 25 nm to 100 nm. Vertical sidewalls with 88 deg. anisotropy and desired dimensions are obtained.

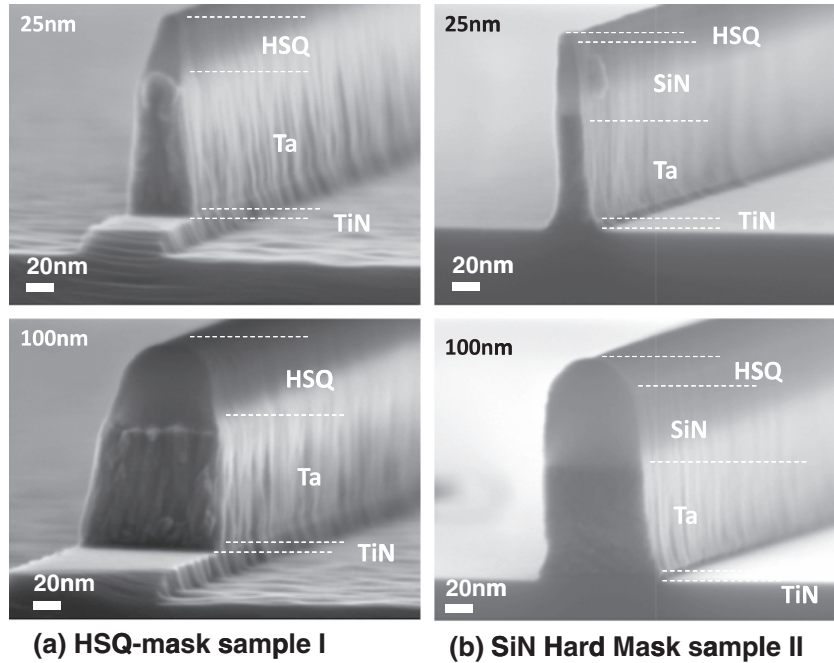


Fig. 2. RIE results comparison: (a) masking using a single HSQ layer suffers from mask deformation, deviation from designed dimensions and severe gate sidewall roughness. (b) masking using a SiN hard-mask shows good preservation of mask dimensions, and smooth sidewalls.

face from exposure to oxidizing atmosphere. For the sake of completeness, the SiN hard-mask is itself etched using a low-pressure (3 mTorr) and low-RIE power (30 W) fluorine-based chemistry (SF_6) for chemical etching combined to argon to introduce anisotropic physical etching. Well controlled SiN patterns with vertical sidewalls (88 deg.) are obtained as shown in Fig. 1 and an adequate etch-rate of 40 nm/min is obtained at a very low pressure of 3 mTorr.

3.2. A combined two-step dry and wet etching

Studies of different gas mixtures and RIE power have been performed to determine the proper etching condition for the best vertical and smooth Ta sidewalls with respect to designed dimensions. Chlorine-based gas mixtures with different RIE power and

gas mixture as Cl_2 , BCl_3 , and SiCl_4 have been investigated since halogenated Ta compounds tend to be volatile [7]. As presented in Fig. 3, high RIE power, and hence high DC-bias, improves the anisotropy of Ta gate-profile to more than 85° and proceeds with an etch-rate sufficiently high to dominate over non-volatile by-product redeposition. Cl_2 and SiCl_4 gas mixtures with Ar ion-assisted physical bombardment is finally proven to optimize etching conditions for Ta sidewall profile control, under a RIE power of 150 W and pressure as low as 3 mTorr. However, chlorine-based plasma etching of Ta tends to form a slightly tapered profile which is possibly due to sidewall passivation and also to the intrinsic isotropic nature of chlorine etching. Thus, over-etching is performed into the TiN layer forming an isotropic etch-stop profile to minimize this defect and to gain on the Ta profile anisotropy. With a taper angle of less than 5° , 140 nm capping Ta layer is well defined based on this process.

To minimize Ta footing-effects and to avoid critical end-point landing onto the thin gate oxide, etching was precisely stopped in the middle of 10 nm TiN layer, leaving the onset of an isotropic profile which is subsequently corrected by a highly selective and isotropic chemical etching step in a sulfuric-peroxide mixture (SPM- H_2SO_4 96%: H_2O_2 30%, 3:1). This solution composition was

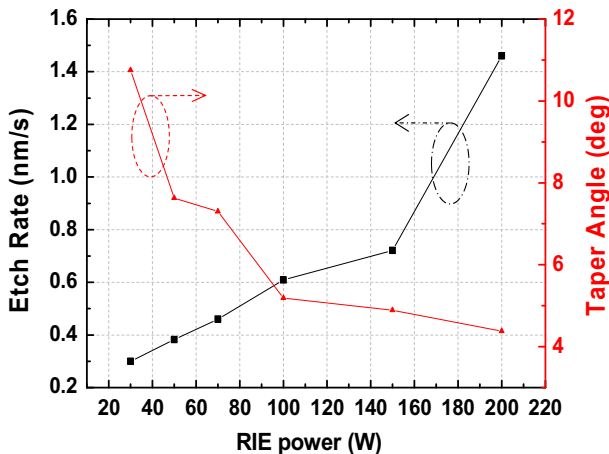


Fig. 3. Variations of Ta gate sidewall profile taper angle and etch rate as a function of RIE power for $\text{Cl}_2 = 10$ sccm/ $\text{SiCl}_4 = 5$ sccm/ $\text{Ar} = 15$ sccm at 3 mTorr. As the RIE power increases, significant improvement is obtained for both taper angle and etch rate.

Table 1

TiN etch rate on full wafer and etch selectivity with respect to the Ta overlayer and the underlying SiO_2 gate dielectric. Various compositions of the SPM solution are reported.

Etcher			Etchant		
SPM composition			Etch rate (nm/s)		
H_2SO_4 (96%)	H_2O_2 (30%)	H_2O	TiN PVD	Ta PVD	SiO_2 dry 725 °C
1	1	0	1.176		
2	1	0	1.111		
3	1	0	0.556	<0.001	<0.001
1	1	1	1.667		
2	1	1	3.333		

Note: Here all the etching tests are performed on full wafer. Here 1 presents 1 volume unity (50 ml of solution).

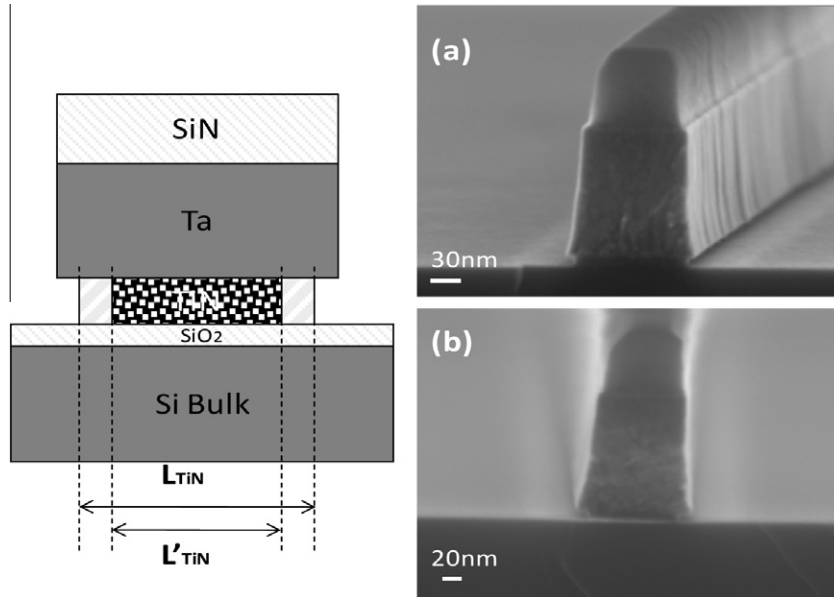


Fig. 4. Schematic and SEM gate line profile for lateral etch rate evaluation in SPM ($\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2 = 3:1$) solution for confined 10 nm thin TiN layer within capped Ta and underlying SiO_2 layers gate stack structure. The difference between (a) 10 s lateral attack L_{TiN} and (b) 15 s lateral attack L'_{TiN} indicates this confined TiN etch rate in SPM solution for about 1 nm/s.

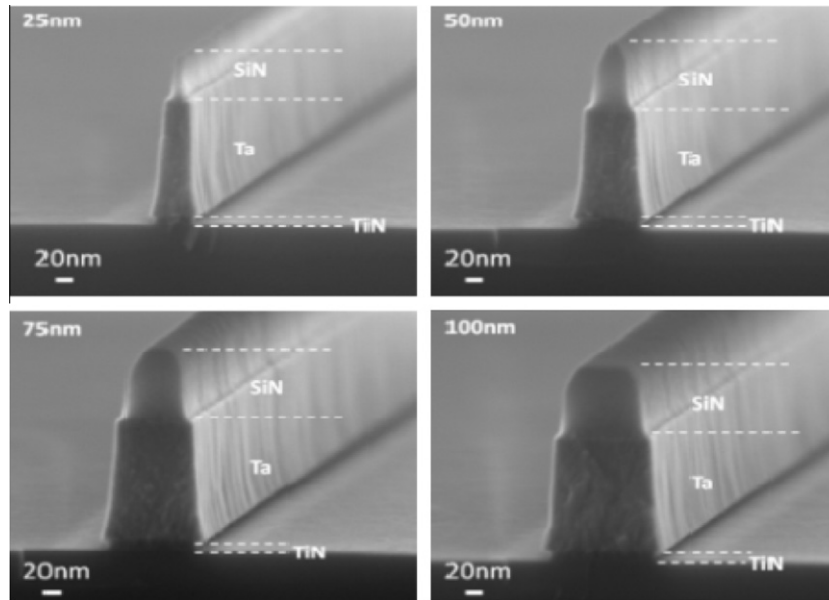


Fig. 5. SEM cross sections of optimized metal etching using combined plasma and wet etching for 25, 50, 75 and 100 nm long gate fingers. A slight footing effect can be observed in Ta capping layer and the desired gate length can be obtained in the bottom midgap TiN layer after the final selective wet etch.

investigated to obtain ultra high etch selectivity (>500) between the TiN layer with respect to the capping Ta layer and the underlying SiO_2 gate dielectric (Table 1).

In order to evaluate the lateral etch-rate of the 10 nm TiN layer confined by the Ta overlayer at the top and by the SiO_2 dielectric at the bottom, two test samples have been processed using the same SiN and Ta plasma etching conditions for which the etch-stop is well controlled in the centre of the TiN layer. The above-specified SPM solution was subsequently applied to over-etch the TiN layer and to form an undercut. The under-etch length varies from L_{TiN} to L'_{TiN} for 10 and 15 s etching time (Fig. 4), giving a 1 nm/s etch-rate for a 10 nm thick confined TiN layer. This figure is about twice faster than in the case of full wafer experiments (Table 1). The fact

that the confined TiN etch rate is superior to that in full wafer is due to the relatively small amount of TiN to remove in only two degrees of freedom. Using this strategy, the final TiN gate length can be accurately controlled by modulating the SPM etching time at a rate of 1 nm/s. Finally, the double-layer full-metal gate fabrication is completed after gate oxide removal in HF 1% solution without damaging the bi-layer metal gate stack or the silicon surface as shown in Fig. 5. Here, the anisotropy of resulting Ta gate profile is 85° and the electrically active TiN midgap gate length after 15 s SPM wet etching exactly matches the original dimension. Quite interestingly, the presented TiN wet etching solution is also compatible for soft and selective landing on a high- k dielectric such as Al_2O_3 .

4. Conclusion

A nanoscale Ta/TiN full-metal single-gate fabrication process using combined dry/wet etching strategy over ultra thin gate dielectric for the integration of gate-first decananometer CMOS technology has been developed in this work. Vertical and smooth Ta capping gate has been demonstrated using a plasma chlorine-based chemistry. It is shown that a SiN hard-mask significantly improves pattern transfer and reduces line edge roughness. A mixture of sulfuric acid and hydrogen peroxide solution is tuned to terminate midgap TiN metal removal offering a soft landing onto gate dielectric and an ultra high selectivity with respect to the capping Ta metal gate and the underlying SiO₂ gate oxide. Moreover, this selective wet gate metal etching process is also compatible for the integration of high-*k* gate dielectrics which should be wet etched in HF as Al₂O₃.

References

- [1] The International Technology Roadmap for Semiconductor (ITRS 2003).
- [2] W.P. Maszara, J. Electrochem. Soc. 152 (7) (2005) G550–G555.
- [3] W.T. Chang et al., J. Vac. Sci. Technol. B 25 (2007) 1265–1269.
- [4] S. Beckx et al., Microelectron. Reliability 45 (2005) 1007–1011.
- [5] A. Litwin, Trans. Electron Dev. 48 (2001) 2179–2181.
- [6] A. Le Gouil et al., J. Vac. Sci. Technol. B 25 (2007) 767–778.
- [7] W.S. Hwang, J. Chen, W.J. Yo, V. Bliznetso, J. Vac. Sci. Technol. A 23 (2005) 964–970.
- [8] W.S. Hwang, B.J. Cho, D.S.H. Chan, V. Bliznetso, W.J. Yo, J. Vac. Sci. Technol. B 24 (2006) 2689–2694.
- [9] T. Skotnicki et al., IEEE Transactions on Electron Devices 55 (2008) 96–130.
- [10] M.M. Hussain et al., Electrochem. Solid-State Lett. 8 (2005) G333–G336.
- [11] H. Shang, M.H. White, Solid-State Electron. 44 (2000) 1621–1625.
- [12] G. Larrieu, E. Dubois, J. Vac. Sci. Technol. B 23 (2005) 2046–2050.
- [13] H. Shimada, K. Maruyama, Jpn. J. Appl. Phys. 43 (2004) 1768–1772.
- [14] M.H. Shin, M.S. Park, N.E. Lee, J. Kim, C.Y. Kim, J. Ahn, J. Vac. Sci. Technol. A 24 (2006) 1373–1379.