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# Thermal performance evaluation of SiC power devices packaging

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## Abstract

Devices based on wide-band gap semiconductors such as SiC, GaN allow high power densities, size reduction, high integration and elevated operating temperatures. In this study, we present solutions for high temperature power packages based on finite element simulations and experimental approach. Analytical methods are used to investigate the best choice among the different selected materials for the substrates, the solder joints and the baseplate. Various power assemblies using SiC diodes have been fabricated. Their thermal performances are evaluated through the measurements of the thermal impedance and the thermal resistance and also finite elements simulations. The correlation between the simulation results and the experimental ones are discussed.

## 1 Introduction

Silicon carbide (SiC) devices are promising components for high performance power system applications, because SiC has a band gap of 3eV which is about three times higher than conventionally used Si. The features of SiC offer the advantage of high temperature operation at more than 150 °C which is higher than the maximum operating temperature of Si devices [1]. A SiC device has been already studied with an operating temperature of 400 °C [2-3]. High temperature operation makes it possible to eliminate the need of a cooling system, resulting in a small system size [4]. A high-density power system is expected to be realized by developing a high temperature module. Then to use SiC devices operating at high temperature, special care will be needed for power package. In this paper, we propose to analyse their thermal performances by experimental and simulation methods.

## 2 High temperature device packaging concepts

The selection of materials for a high temperature package (figure 1) is based on a combination of material properties: conductivity, Coefficient of Thermal Expansion (CTE), elasticity, and cost. CTE is one the most important property: then materials are selected for their high Thermal Conductivity (TC) and low CTE.

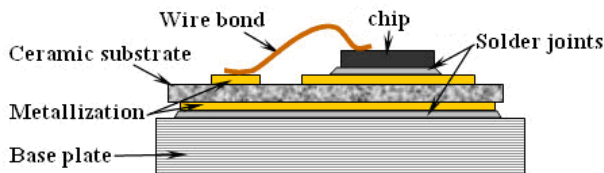


Figure 1 - Structure of power electronic module [5]

We use a selection of materials suitable (table 1) for high temperature package assembly, including die attach ( $\text{Au}_{88}\text{Ge}_{12}$ ,  $\text{Au}_{97}\text{Si}_3$ ,  $\text{SnPb}_{95}$ ), substrate ( $\text{Si}_3\text{N}_4$ ,  $\text{AlN}$ ), wire bonding (Al, Au) and baseplate (CuC, Cu-

diamond). Various materials combinations are proposed in order to try to find and optimize the performance and the reliability of the assembly. From a thermal point of view, the thermal resistance ( $R_{th}$ ) of power package can be considered as one of the key parameters for high temperature device packaging concepts.

	SiC die	Die attach	Substrate	Metallization
TV1	Diode	$\text{SnPb}_{95}$	$\text{Si}_3\text{N}_4$	Cu
TV2	Diode	$\text{AuGe}_{12}$	$\text{Si}_3\text{N}_4$	Cu
TV3	Diode	$\text{AuGe}_{12}$	AlN	Al
TV4	Diode	$\text{AuSi}_3$	$\text{Si}_3\text{N}_4$	Cu
TV5	Diode	$\text{AuSi}_3$	AlN	Al
TV6	Diode	$\text{SnPb}_{95}$	AlN	Al

Table 1 - Matrix of test vehicles with SiC diodes

## 3 Experimental approach

The measurement of thermal resistance takes place in two phases using a thermal analyzer ANATECH PHASE 10 (figure 2). The first one is the calibration of the Temperature Sensitive Parameter (TSP) allowing the measurement of temperature at the level of the voltage  $V_d$ , and the second is the measure of the thermal resistance. This will be explained more in detail hereafter.

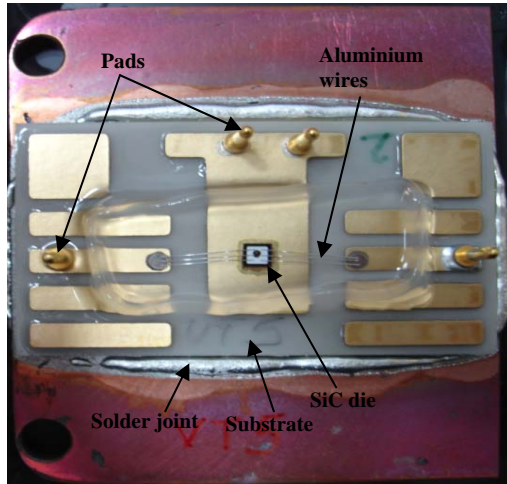




$$V_d = \frac{KT}{q} \ln \left[ \frac{I_d}{I_s} \right] \quad (1)$$

**Figure 2 - Test bench of thermal resistance measurement**

We used the test vehicle of the whole packaging to measure the thermal resistance. The test vehicles are made by the silicon carbide diode, the die attach, the ceramic substrate with different metallization (table 1), the solder joints (SnAg<sub>3</sub>) between the substrate and the baseplate, and the baseplate (CuC<sub>40</sub>). The silicon carbide diode is wired by 6 aluminium wires (figure 3).



**Figure 3 - Test vehicle of the whole package**

The geometrical parameters of the test vehicle are indicated in the table below:

	Material	Surface (mm <sup>2</sup> )	Thickness (μm)
wire bond	Al	125μm diameter	-
SiC chip	SiC	3.64*3.64	400
die attach	AuGe <sub>12</sub> /AuSi <sub>3</sub> / /SnPb <sub>95</sub>	3.8*3.8	50
substrate	Si <sub>3</sub> N <sub>4</sub>	30*30	320
	AlN	30*30	1000
metallization	Cu	-	300
	Al	-	400
solder joint	SnAg <sub>3</sub>	30*30	100
baseplate	CuC <sub>40</sub>	40*40	4000

**Table 2 - The geometric parameters of the test vehicle**

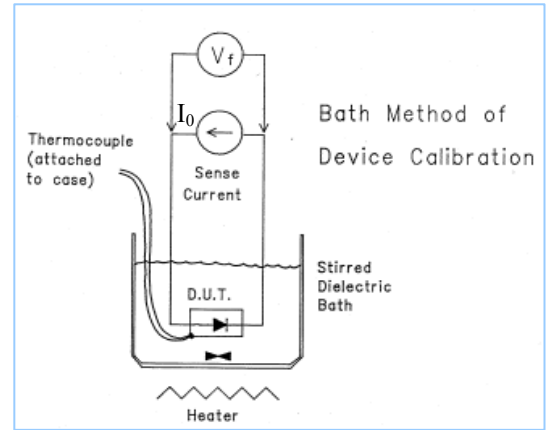
### 3.1 The calibration of the Temperature Sensitive Parameter (TSP)

The thermal resistance measurement of power semiconductor is based on the calibration of the TSP. In the case of silicon carbide diode, there is a linear relationship between the on-state voltage drop across a P-N junction and temperature (Equation 1) [6].

With,  $V_d$  : voltage across the P-N junction (V)  
 $I_d$  : direct current through the P-N junction (A)  
 $I_s$  : saturation current (A)  
 $K$  : Boltzman constant (eV.K<sup>-1</sup>)  
 $T$  : local temperature (K)  
 $q$  : charge (e)

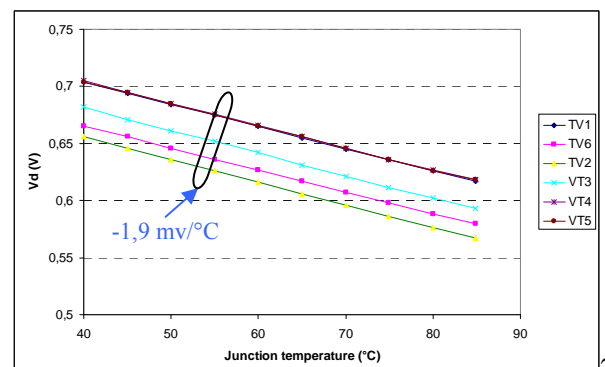
When the calibration is finished, we know the exact equation of  $V_d = f(T)$ , and it is possible to obtain at any time the junction temperature from the value of the voltage  $V_d$ .

The SiC diode is connected to a current generator, a constant current “ $I_0$ ” of 1mA which can avoid the self-heating is injected into the diode. The test vehicles are placed in a dielectric liquid bath GALDEN D02, and a thermocouple is placed nearby the TV (figure 4).



**Figure 4 - Schematic description of the calibration of the TSP [7]**

Firstly, the temperature of the dielectric liquid is increased gradually by the heater to 90°C. Once this temperature is reached, the heating of the bath is stopped. Then, the step of cooling down is carried out by a fan to come down to room temperature (25°C). During this period which may last several hours, several measurements are obtained at every 5°C step of temperature from 90°C down to 40°C and the voltage across the junction. We obtain the results of the calibration of TSP (figure 5)





**Figure 5 - Calibration results of TSP**  
(voltage-temperature relationship)

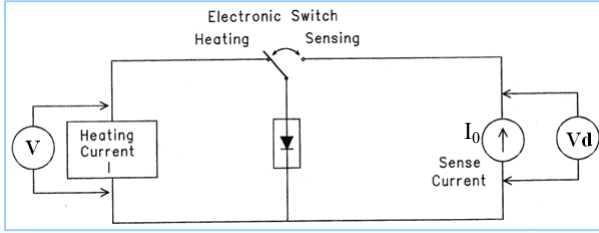
We can observe that the voltage  $V_d$  decreases when the junction temperature ( $T_j$ ) increases. The relationship between the junction temperature ( $T_j$ ) and the voltage ( $V_d$ ) can be expressed mathematically by the equation 2, the slope line is -1,9 mV/°C for SiC device:

$$V_d = m \cdot T_j + V_0 \quad (2)$$

With,  $T_j$  : junction temperature (°C)  
 $m$  : slope of the line (V.°C<sup>-1</sup>)  
 $V_d$  : voltage across the P-N junction (V)  
 $V_0$  : voltage of the source coordinate (V)

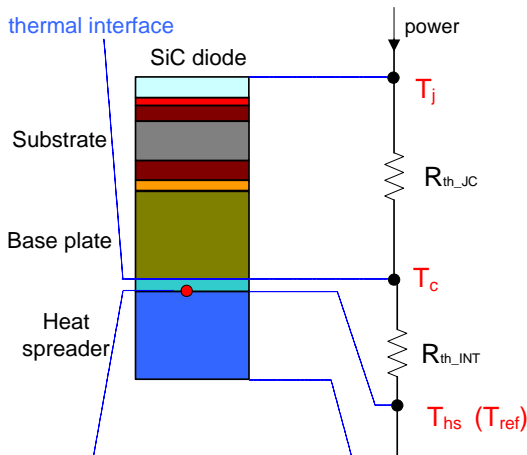
### 3.2 Thermal resistance measurement

Once the calibration of TSP is finished, we can begin measuring the thermal resistance, which consists in two phases: one is the phase of heating the SiC diode; the other is the measurement of the thermal resistance (figure 6).



**Figure 6 - Schematic descriptions of two phases to measure thermal resistance [7]**

It is important to consider the safe operating area of the component, a power of about 9 W is applied by a generator to SiC diode. The test vehicle is connected by an electronic card interface to measure the thermal resistance of whole package. A thermocouple is placed between the controlled cold plate ( $T_{ref} = 25^\circ\text{C}$ ) and the interlayer double sided adhesive. The thermal resistance of the assembly is the sum of all thermal resistances of each material (figure 7).



**Figure 7 - schematic descriptions of different thermal resistances for a test vehicle (heat transfer by conduction)**

We can define:

- $R_{th-JC}$  as the junction to case thermal resistance. It is defined between the junction temperature  $T_j$  (maximum temperature in the chip) and temperature  $T_c$  (bottom surface temperature of the baseplate).
- $R_{th-INT}$  as the thermal resistance of the adhesive layer. The test vehicle is fixed on the heat spreader with an interlayer double-sided adhesive.
- $R_{th-HS}$  as the thermal resistance between the heat spreader and the air.

The table below presents the technical characteristics of an interlayer double-sided adhesive:

Thermal conductivity :	1 W/m.K
Thickness :	0.15 mm
Thermal resistance :	0.17 °C/W *
Operating temperature :	-45°C / +170°C
Isolation voltage :	3 kV

\*we take into account the substrate surface.

**Table 3 - Specifications for the thermal interface double-sided adhesive [8]**

### 3.3 Experimental results

#### Thermal resistance

We obtain the results of thermal resistance for the matrix (Table 1) of test vehicles, and have been summarized in the table 4:

TVs	Power (W)	$T_j$ (°C)	$T_{ref}$ (°C)	$V_j$ (V)	$R_{th}$ (°C/W)
1	8.93	45.22	26	0.7	2.15
2	8.96	42.94	26.6	0.65	1.82
3	9.12	42.74	25.8	0.68	1.86
4	8.93	42.92	25.7	0.69	1.93
5	8.99	43.67	26.1	0.7	1.96
6	8.96	46.07	25.8	0.66	2.26

TVs: Test Vehicles;  $T_j$ : Junction Temperature;  $T_{ref}$ : Reference Temperature;  $V_j$ : Junction Voltage;  $R_{th}$ : Thermal Resistance

**Table 4 - Experimental results of thermal resistance for different models of assemblies**



The thermal resistance results (table 4) illustrate that TV2 model (with die attach solder AuGe<sub>12</sub>, substrate ceramic Si<sub>3</sub>N<sub>4</sub> Cu metallization) has a low thermal resistance (1.82°C/W), it might have a good performance assembly. TV6 model (with die attach solder SnPb<sub>95</sub>, substrate ceramic AlN Al metallization) shows the heat dissipation is less effective compared to others. So it appears that the solder AuGe<sub>12</sub> seems to be the best choice in terms of thermal performance for configurations of identical metallic substrates.

## 4 Numerical simulations approach

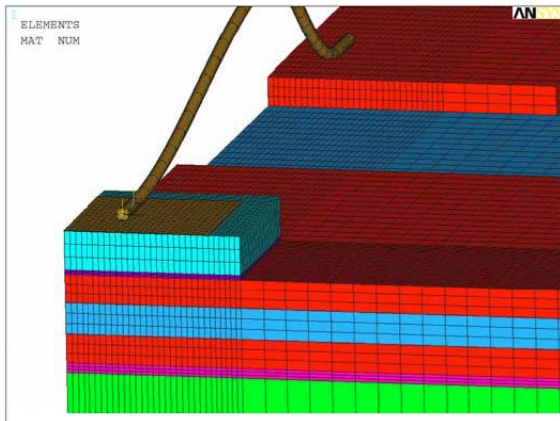
The general design strategy is to choose a set of materials that appears to match by looking at the material properties (table 5), and then develop a package which drives these properties to the best use.

	Material	S.H.C (J/Kg.K)	T.C (W/m.K)	Density (Kg/m <sup>3</sup> )
wire bond	Al	900	210	2700
SiC chip	SiC	750	450	3100
die attach	AuGe <sub>12</sub>	150	44	14670
	AuSi <sub>3</sub>	150	27	15400
	SnPb <sub>95</sub>	133.8	23	11060
substrate	Si <sub>3</sub> N <sub>4</sub>	800	60	3290
	AlN	750	190	3300
metallization	Cu	385	398	8930
	Al	900	210	2700
solder joint	SnAg <sub>3</sub>	200	33	7360
baseplate	CuCu <sub>40</sub>	430.2	360	6256

S.H.C: Specific Heat Capacity; T.C: Thermal Conductivity;

**Table 5 - Thermal properties of the elements [9-10]**

Using ANSYS finite elements software, a 3D thermal simulation of power assembly has been built. For reducing simulation time, only a quarter of the power assembly is simulated. Three-dimensional solid elements (linear brick and tetrahedron) were used for meshing the geometry (figure 11). The interfaces being supposed perfect. The boundary condition is imposed on the bottom surface of the assembly (baseplate) with a constant temperature 25°C, this temperature is the reference temperature T<sub>ref</sub>. A power of about 9 W is injected into SiC diode.



**Figure 11 - Meshed geometric model assembly**

### 4.1 Thermal simulations results

The junction temperature T<sub>j</sub> is the maximum temperature in the die, localized at centre of upper part of the SiC device (figure 12).

The heat flux balance across assemblies and the thermal resistances were evaluated from the thermal simulations. The thermal resistances were calculated from the chip maximal temperature and the reference temperature, measured when the steady state is reached (Equation 4).

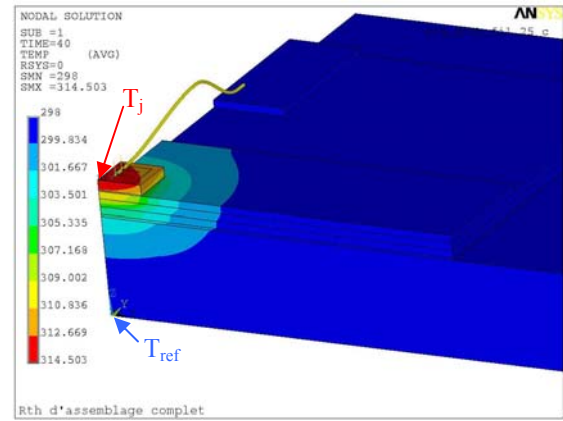
$$R_{th} = \frac{T_j - T_{ref}}{Q} \quad (4)$$

With, R<sub>th</sub>: thermal resistance of assembly (°C/W)

T<sub>j</sub>: junction temperature (°C)

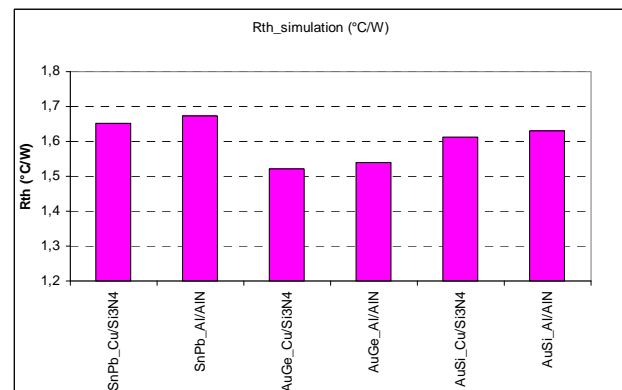
T<sub>ref</sub>: reference temperature (25°C)

Q: power dissipation (W)



**Figure 12 - Temperature distributions in Kelvin in 3D model assembly**

Thermal simulation results (R<sub>th</sub>) with different selections of materials (table 1) is summarized in the figure 13.



**Figure 13 - Simulation results of R<sub>th</sub> with different models**

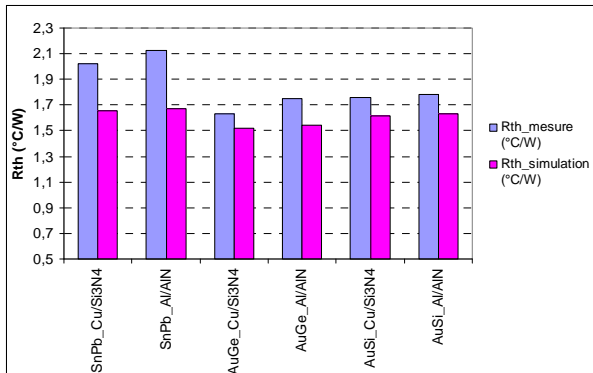
The simulation results of the thermal resistance also show that the TV2 model (with die attach solder AuGe<sub>12</sub>, substrate ceramic Si<sub>3</sub>N<sub>4</sub> Cu metallization) shows the



lower thermal resistance leading to think that this configuration might have the best thermal performance.

## 4.2 Correlation between the simulation results and the experimental results

Figure 14 shows the comparison between experimental results and simulation ones for different models of thermal resistance assembly.



**Figure 14 - Comparison between experimental results and simulation ones for different models of thermal resistance assembly**

The two curves show that they have the same trend for the different models. But the experimental results have higher values than the simulation results due to the thermal resistance of double-sided adhesive thermal interface not include in the simulation. Additionally, the interfaces of assembly are not perfect, it also increases the thermal resistance values.

## 5 Conclusion

This study is to develop high temperature packaging technologies based on available materials, using ANSYS finite elements software to propose design rules and carry out the thermal simulation. We have taken into account the different selections of materials with the most critical design parameters to define the model. Thermal resistances are calculated by thermal simulation and have been measured by experimental approach in order to

verify the simulation results and thermal performances. Thermal impedance method is used to determine the failure of the assembly after aging test showing the sensibility of test vehicle to thermal fatigue and the weakness of the substrate to baseplate report process.

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