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Efficient physical-thermal model for thermal effects in AlGaN/GaN high electron mobility transistors

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This letter describes the thermal behavior of AlGaN/GaN high electron mobility transistors on different substrates thanks to a fully consistent physical-thermal model. Self-heating explains the drastic reduction in the current flowing from drain to source. It is shown that, in order to keep the material from significantly degrading at the gate exit, the maximum dissipated power must be limited to 7 W/mm, 13 W/mm, and 38 W/mm for silicon, silicon carbide, and diamond substrates, respectively. These results have been validated from experimental thermal measurements. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4753815>]

AlGaN/GaN high electron mobility transistors (HEMTs) are good candidates for high power and high frequency operation due to a wide band gap, a high saturation velocity, and piezoelectric effects leading to a two dimensional electron gas with a high sheet carrier density without any doping impurities. Up to now, due to the lack of semi-insulating GaN substrates, major studies and developments are performed on SiC substrates,¹ Si substrates,² and composite substrates^{3,4} and more recently on diamond substrates.⁵ SiC substrates lead to the most relevant performance but are expensive. Therefore, silicon or composite substrates constitute an interesting possibility for low cost applications. Very high output power densities can be achieved with such a component.⁶⁻⁸ However, these high densities involve an important self-heating leading to significant operating temperatures and thus reducing the performance and reliability of the device. Previous studies on thermal effect analysis based on Monte-Carlo model,⁹ pure thermal analysis,¹⁰ or drift diffusion thermal model¹¹ have already been published. Though the first one is very accurate, it needs very long central processing unit (CPU) times and is consequently not fully suitable for the topology design of a component. The second needs short CPU times but the heat source is not accurately defined and the result is not self-consistent. The third one does not allow studying the behavior of HEMT with short gate length.

Our investigation is based on a fully two-dimensional (2D) physical-thermal model resulting from the coupling of an energy balance model describing electron transport in the active area of the transistor and a thermal model solved in the whole structure, including the substrate. The energy balance model is based on a set of conservation equations coupled with Poisson's equation. Such a model involves three conservation equations: the continuity equation for electrons, the momentum conservation equation, and the energy conservation equation. These equations are based on Euler equations, with additional source terms taking collisions and electric field into account. In the continuity equation, the source term is set to zero as long as generation and recombination effects are neglected. In the momentum conservation equation, inertia effects are neglected, which leads to an approximate but analytical expression of the carrier velocity. This is a common assumption in energy balance models. In the energy balance

equation, the first source term describes the gain of energy under the effect of an electric field while the second one describes the loss of energy in the electron gas resulting from inelastic collisions with the lattice. This mechanism is responsible for the local heating of the lattice and the corresponding source term is considered as the heat source for the thermal equation. In our model, this term is treated employing a relaxation time approximation. Moreover, non stationary effects arising in HEMTs with short gate length can be taken into account thanks to this model as long as we use energy dependent physical transport properties. These physical transport properties such as electron mobility, effective mass, and energy relaxation time stem from Monte-Carlo calculations performed for lattice temperatures ranging from 300 K to 700 K. Using Monte-Carlo results, each physical parameter is expressed as a function of both electron temperature and lattice temperature. For a lattice temperature equal to 300 K, the obtained results are close to those published by Farahmand *et al.*¹² Low field mobility, peak velocity, and saturated velocity decrease significantly when the lattice temperature rises. The thermal model is based on Fourier's Law with temperature dependent lattice thermal conductivities, expressed by a similar power law for all materials. Lattice thermal conductivities are influenced by many factors like residual impurity concentration, layer thickness, strain, orientation, and crystalline type. We selected mean values currently published for the different substrates we used for the measurements: (111) Si and 4H-SiC semi-insulating substrates. The equations we used are listed below for silicon carbide,¹³ gallium nitride,¹³ silicon,¹⁴ and diamond:¹⁵

$$K_{GaN}(T) = 160. \left(\frac{300}{T} \right)^{1.4} \text{ (W/mK)},$$

$$K_{SiC}(T) = 340. \left(\frac{300}{T} \right)^{1.5} \text{ (W/mK)},$$

$$K_{Si}(T) = 150. \left(\frac{300}{T} \right)^{1.3} \text{ (W/mK)},$$

$$K_{diamond}(T) = 2000. \left(\frac{300}{T} \right)^{1.15} \text{ (W/mK)}.$$

As the details of the model have already been described in a previous paper,¹⁶ we only describe the coupling of both models, which are implemented using the Comsol Multiphysics software, designed to solve coupled partial differential equations involved in numerous fields of physics. The energy balance model and the thermal model having very different time constants, we have to follow the transient behavior of the thermal model whose time constant is much larger. At each time step of the thermal model, the transport parameters are updated and the energy balance model is solved up to convergence, thus giving an updated value of the heat source. This is repeated until both models converge. Taking the local lattice temperature everywhere in the device into account, and considering a feedback between the increase of the lattice temperature and the evolution of the heat source are the most important features of the model.

Measurements of local temperature have been performed using the Infrascopie temperature mapping system, MWIR512, developed by Quantum Focus Instruments Corporation. When a surface gets hot, it emits an amount of thermal radiation which is a function of its temperature. Most of this radiation is in the infrared region of the electromagnetic spectrum. Most surfaces do not behave as blackbody emitters and only emit some of the thermal radiation that a blackbody does. This is characterized by an emissivity. Infrared radiations are measured by an InSb detector which operates at cryogenic temperature. The Infrascopie measures the emissivity at each pixel location using a calibration phase during which the component remains non-polarized at a fixed, known temperature. Then, bias voltages are applied to the component, self-heating occurs and the amount of infrared radiations is measured at each pixel location by the InSb detector, enabling the determination of the local temperature.

Thanks to this self-consistent physical-thermal model, the thermal behavior of an AlGaIn/GaN HEMT is investigated on different substrates namely silicon, silicon carbide, and diamond. The performances obtained on different substrates are studied and compared with those resulting from an isothermal modeling. Isothermal calculations provide the best results as far as the output current is concerned. Isothermal working can be seen as the best operating condition, could the degradation of the transport properties resulting from self heating be suppressed. The studied epitaxy consists of a 0.4 μm thick GaN layer, on which a 25 nm thick AlGaIn barrier layer is deposited. The simulated substrate is 400 μm wide and 500 μm high. The gate-source distance is 0.5 μm , the source-drain distance is 1.5 μm , and the gate length is 0.3 μm .

Figure 1(a) shows a two dimensional distribution of the electron temperature in the active area for a transistor on a silicon carbide substrate, and for applied voltages $V_{DS} = 12$ V and $V_{GS} = 0$ V. The figure clearly highlights a large area at the gate exit where the electron energy and thus the electron temperature are very high. In this case, the maximum electron energy is close to 1 eV for a silicon carbide substrate, thus inducing a large source term in the channel resulting from this high electron temperature and a high electron density in the channel at the gate exit. Figure 1(b) shows the corresponding two dimensional distribution of the lattice temperature in the structure. The highest lattice temperature, close to 530 K, is

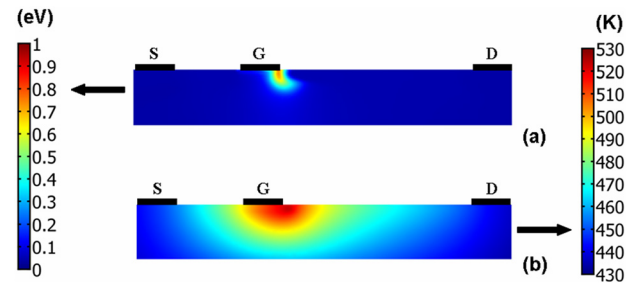


FIG. 1. (a) 2D distribution of electron energy in the active area. (b) 2D distribution of the lattice temperature in the active area.

located in the channel, at the gate exit. It can be also noticed that there is a large difference, close to 80 K, between the highest and the lowest temperatures in the active area, due to the strong localization of the source term.

Output characteristics at open channel ($V_{GS} = 0$ V) obtained for the same transistor on different substrates as well as isothermal calculations as a basis for comparison, are gathered in Figure 2. The highest current is obtained for isothermal calculations in which self heating is neglected, thus keeping the best transport properties obtained for a uniform lattice temperature equal to 300 K. The current is close to 1.9 A/mm for a drain-source voltage equal to 10 V. Taking self heating into account, and for the same voltages, the current drop is close to 12% for a diamond substrate, around 34% for a silicon carbide substrate and as high as 50% for a silicon substrate. As far as the current is concerned, self heating is very harmful due to a drastic lowering of transport properties when the lattice temperature increases.

The evolution of the lattice temperature for each substrate as a function of the dissipated power is shown in Figure 3. Some experimental results are gathered on the same figure stemming from our measurements and from literature. A good agreement is obtained with results from Felbinger¹⁷ for both SiC and diamond substrates. For silicon and silicon carbide substrates, our experimental results are in very good agreement with our theoretical results, which validates the model as a reliable and predictive model. Regarding silicon substrates, as the dissipated power increases the lattice temperature drastically rises because of the relatively poor thermal conductivity of silicon. This thermal conductivity being higher for silicon carbide, the lattice temperature increases more slowly. The monocrystalline diamond substrate with an

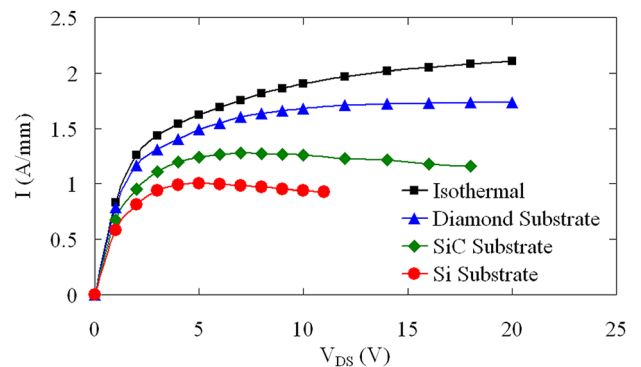


FIG. 2. Comparison of the $I(V_{DS})$ characteristics obtained for different substrates with an isothermal result. Results are shown for $V_{GS} = 0$ V.

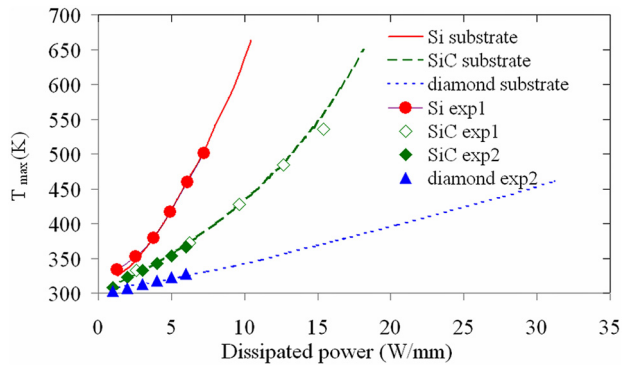


FIG. 3. Comparison of the maximal lattice temperatures obtained with the physical-thermal model and experimental results: (1) IEMN measured results on silicon (Si exp1) and on SiC (SiC exp1) substrates. (2) Published results⁸ on SiC (SiC exp2) and on diamond (diamond exp2) substrates.

outstanding thermal conductivity leads to the lowest lattice temperatures. In order to prevent high temperatures from inducing degradation in the transistor, it will be interesting to limit the increase of temperature in the active area to 200 K. Therefore, the dissipated power in the active area should be lower than 7 W/mm for a silicon substrate, 13 W/mm for a SiC substrate and close to 38 W/mm for a diamond substrate. Considering the evolution of the thermal resistances versus the dissipated power shown in Figure 4, a slight increase from 3.2 to 5.2 Kmm/W is observed for the diamond substrate. A more significant increase for a silicon carbide substrate from 9 to 19 Kmm/W and a drastic increase for the silicon substrate from 16 to 34 Kmm/W are noted.

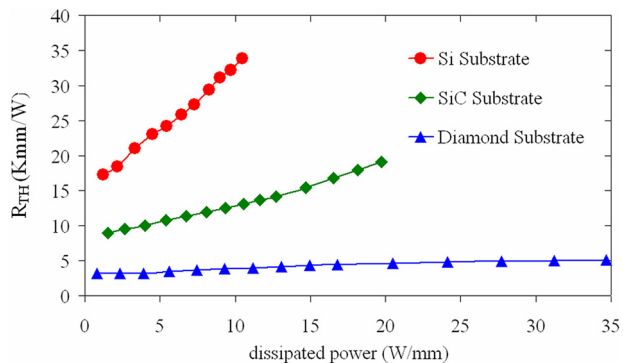


FIG. 4. Evolution of the thermal resistance R_{TH} versus dissipated power for the different substrates.

This physical-thermal model is a useful, reliable tool to design an AlGaIn/GaN HEMT for power applications, taking self heating effects into account. This model validated by experimental results is predictive and, as such, can be used to design transistors for power microwave applications. It is based on the physical quantities and does not need any empirical fitting parameters, which is its main advantage. The CPU times required on a XEON processor are close to 750 s for the energy balance model and only 200 s for the thermal model when solving the physical model for 10 ps and the thermal one for 1 ms. The convergence only needs three or four iterations for a diamond substrate and typically eight or nine iterations for silicon.

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