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Anomaly and defects characterization by I-V and current deep level transient spectroscopy of $Al_{0.25}Ga_{0.75}N$/GaN/SiC high electron-mobility transistors

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In this paper, we report static electric drain-source current-voltage measurements for different gate voltages and at different temperatures, performed on $Al_{0.25}Ga_{0.75}N$/GaN/SiC high electron-mobility transistors (HEMT). The results show the presence of kink and collapse effects. We have demonstrated that these effects are significant in the temperature range varying from 150 to 400 K with a maximum around 300 K. This parasitic effect was correlated with the presence of deep levels in our transistor. Indeed, we have noticed the presence of two electron traps named A_1 and A_2, and one hole trap named H_1; their respective activation energies, which are determined using current deep level transient spectroscopy (CDLTS), are, respectively, 0.56, 0.82, and 0.75 eV. Traps H_1 and A_1 are shown to be extended defects in the $Al_{0.25}Ga_{0.75}N$/GaN heterostructure; they are supposed to be the origin of the kink and collapse effects. However, the punctual defect A_2 seems to be located either in the free gate-drain surface, in the metal/AlGaN interface, or in the AlGaN/GaN interface. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3702458]

I. INTRODUCTION

AlGaN/GaN high electron-mobility transistors (HEMTs) were initially developed for power applications. The GaN and SiC thermal conductivities (190 and 400 W m^{-1} K^{-1}, respectively, at 300 K) allow good dissipation of heat generated in the channel. These good thermal properties make the GaN-based HEMTs grown on the SiC substrate very promising for power applications. The AlGaN/GaN devices already show excellent performance in cell phone base stations and are promising candidates for power switching applications.[1–6] Most research concerning HEMTs have focused on improving power output and power added efficiency. These improvements will probably make these devices the most used in telecommunication applications. But there are still few unsolved problems, such as the presence of electronic traps, limiting the performance of AlGaN/GaN HEMT devices for next generation high power and high frequency electronics. Some studies revealed that the drain current collapse and Kink effect in HEMT devices were correlated to the presence of traps.[7,8] Therefore, it is necessary to perform basic investigations of deep level defects in AlGaN/GaN heterostructures. To date, a number of researchers have investigated the deep level defects in AlGaN/GaN heterostructures using various characterization techniques, such as photo-ionization spectroscopy,[9] charge-based deep level transient spectroscopy (QDLTS),[10] deep level optical spectroscopy (DLOS),[11] current deep level transient spectroscopy (CDLTS),[12,13] and deep level transient spectroscopy (DLTS).[14,15]

In previous work,[15] we had started the study of the $Al_{0.25}Ga_{0.75}N$/GaN/SiC structure by realizing Ig(Vg), C(V) and capacitance DLTS measurements on the (Ni/Au) $Al_{0.25}Ga_{0.75}N$/GaN/SiC Schottky barrier diode because it is very crucial to understand the influence of defects on the carrier transport in such heterostructures. From these measurements, we had observed abnormal behaviors in the Ig(Vg) and C(V) characteristics like the temperature dependence of the barrier height, important leakage current, and the capacitance hysteresis phenomenon.[15] We correlated them with the presence of an extended hole trap having an activation energy of 0.75 eV. As a continuation of this study, we will try to emphasize other parasitic effects which may have an influence on the carrier control in the channel. Therefore, we will move from a diode to a transistor, both fabricated on the same heterostructure ($Al_{0.25}Ga_{0.75}N$/GaN/SiC), in order to realize drain-source current voltage measurements.

In this paper, we report specific deep levels related to $Al_{0.25}Ga_{0.75}N$/GaN HEMT grown on the SiC substrate, using the CDLTS technique and Ids(Vds) measurements at various temperatures and for different values of the gate-source voltage (Vgs).

II. SAMPLE DESCRIPTION AND EXPERIMENTAL DETAILS

The AlGaN/GaN heterostructure was grown by metal organic chemical vapor deposition (MOCVD) on the SiC substrate. The epilayers consist of a 100 nm AlN nucleation

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layer followed by a 1.2 μm unintentionally doped (Uid) GaN and a 30 nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer Si doped (3×10^{18} cm^{-3}). The device has a gate width of 100 μm, a gate length of 0.3 μm, a gate-drain and gate-source spacing of 2 and 1 μm, respectively. The Schottky contact was made with an optimized metallization of Ni/Au with respective thicknesses of 200 Å/2000 Å. The ohmic contacts are made with the metallization optimized Ti/Al/Ni/Au with respective thicknesses of 120/2000/400/1000 Å.

The CDLTS technique consists of changing the equilibrium occupancy of the deep level states by successive voltage pulses applied to the gate. According to the bias applied between the source and the drain, electrons are moved and trapped by the different empty centers. When the voltage excitation is turned off, a transient current corresponding to the thermal emission of the traps is observed. The value of the transient current I(t) is measured at two sampling times t_1 and t_2 and the difference $(I(t_1)–I(t_2))$ is continuously recorded as a function of temperature as it is used in normal DLTS analysis.[16] The drain-source current transients are recorded using a numerical multimeter (HP34401 A). A liquid nitrogen cooled cryostat is used for temperature dependent measurements which are carried out between 10 and 550 K.

The emission rate, which is defined as the probability per unit time as an electron is emitted from a trap, is

$$e_n = \sigma_n \gamma_n T^2 \exp\left(-\frac{E_a}{k_B T}\right),$$

where σ_n is the electron capture cross section, γ_n is a temperature independent term that contains the density and thermal velocity of electrons, E_a is the trap activation energy, and k_B the Boltzmann constant.

III. DRAIN CURRENT-VOLTAGE MEASUREMENTS

Static electric drain-source current voltage Ids(Vds) measurements of the $Al_{0.25}Ga_{0.75}N$/GaN/SiC HEMT, for various gate-source voltage values (Vgs = 0 V to Vgs = −7 V, step of −1 V) were performed between 100 and 550 K (three examples at 100 K, 300 K, and at 450 K are given in Figs. 1(a), 1(b), and 1(c), respectively).

The Ids(Vds) characteristics, measured after varying up and down the drain source voltages on $Al_{0.25}Ga_{0.75}N$/GaN/SiC HEMT, allow us to notice the presence of the Kink effect. The latter appears on the Ids(Vds) characteristics when Vds increases from 0 to 12 V. This effect represents a sudden increase in the drain current at a certain value of drain-source voltage ($V_{ds} = V_{kink}$). This drain current variation induces an increase of the drain/source output conductance (g_{ds}) and a compression of the transconductance g_m, then degrading the performance of the field-effect transistors. To explain the Kink effect, many works[17–19] comment on the direct link between impact ionization and trap effects as a function of temperature. According to Meneghesso *et al.*,[7,20] the Kink effect is produced by the trapping of negative charges under the gate, possibly in the GaN buffer layer for low Vds values and followed by liberation of these charges for high Vds. This effect generates a shift of the pinch voltage Vp toward a more negative value (in our case Vp varies from −6.35 to −6.9 V at room temperature) and induces the sudden increase of the drain current Ids. For a better understanding of the origin of this effect in our component, electrical measurements were first realized as a function of Vds direction (see Fig. 1). The Ids(Vds) curve shows the kink effect appearance in the upward Vds direction (from

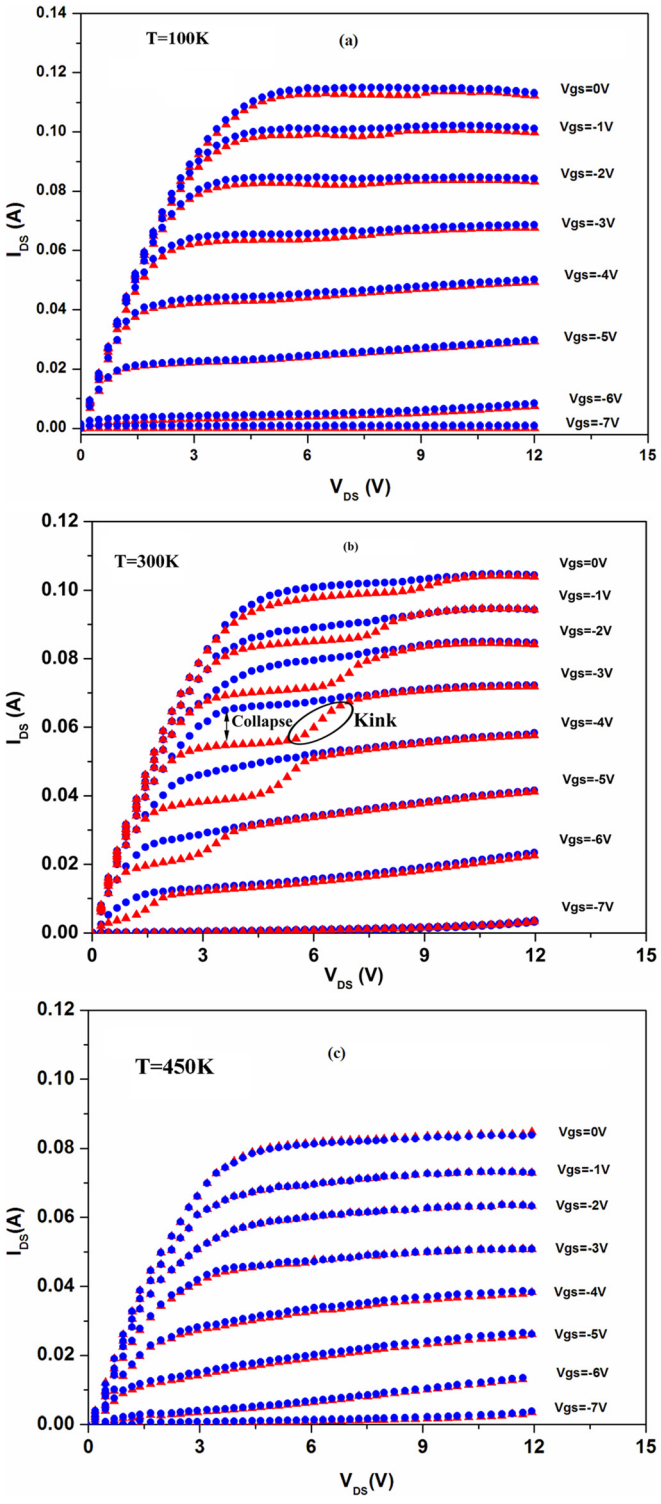

FIG. 1. Ids(Vds) characteristics measured at T = 100 K (a), T = 300 K (b), and T = 450 K (c). The drain bias has first been increased from 0 to 12 V (red curves) and then decreased from 12 to 0 V (blue curves).

0 to 12 V), while it partially disappears in the downward Vds direction (from 12 to 0 V). This electrical behavior reflects the activation of the traps localized in the epitaxial structure. Second electrical measurements were realized as a function of temperature (from 100 to 550 K), as shown in Fig. 1. We notice that the Kink effect is observed in the temperature range varying from 100 to 350 K, especially at room temperature; whereas it is absent at high temperatures ($T \geq 400$ K). Thus, the kink effect ought to be related to the presence of deep level traps in the same temperature range.

In addition, we observe another parasitic effect on the Ids(Vds) output characteristics known as current collapse. The output characteristics Ids(Vds) (Fig. 1) show a decrease of the drain current together with an increase in knee voltage, this occurs for $V_{knee} \leq Vds \leq V_{Kink}$. This observation is in a good agreement with Fu *et al.*[21] who have mentioned that the current collapse turns up in the pre-Kink region ($Vds < Vkink$) and the drain current recovers to its normal value in the post-Kink region ($Vds > Vkink$). Klein *et al.*[9] have also shown that the loss of channel carriers leads to a collapse of the DC I-V characteristic, which exhibits a reduced drain current and an increase in the knee voltage. Further investigations, using pulsed I(V)/dynamic radio frequency (RF) measurements, should be held in order to explain this electrical behavior and will be opened to future discussions.

Static electrical characteristics Ids(Vds) at different temperatures show also that this effect increases with temperature in the range varying from 100–300 K. While it decreases until it disappears at $T = 450$ K (see Fig. 1). Up to 550 K, the characteristics are similar to those measured at 450 K, with a very low variation of the current when the temperature increases. This behavior can be correlated with the thermal emission of deep traps.[22]

The collapse effect was already observed on GaN-based FET grown by metal-organic vapor phase epitaxy (MOVPE) and explained by the presence of traps in the GaN buffer layer or structural defects in this layer.[23] However, this suggestion does not conclusively rule out the possibility that trapping in the AlGaN layer is a contributing fact.[23] This idea is supported by Nakajima *et al.*,[24] who claims that the current collapse is due to the hot electrons trapped by deep levels at the AlGaN surface. Indeed, the hot carriers are injected from the conducting channel to an adjacent region of the device, which contains a high concentration of deep trapping centers. The subsequent trapped carriers leads to the reduced drain current. According to Pavlidis *et al.*,[25] the current collapse is associated with the hot electron trapped in the gate-drain space, under the gate in the AlGaN barrier layer or at the surface, which induced the 2DEG channel depletion and an increase of the channel resistance between the gate and the drain. Figure 2 shows a schematic section of an AlGaN/GaN HEMT, indicating the possible localization of trap likely to interact with the hot carriers at the edges of the gate.[26] The carriers trapped in the gate edge at the drain side leads to a knee-voltage walkout. Then, trapping carriers in the gate edge at source side induces a current saturation decrease in the channel. Both trapping areas generally induce an increase of the channel resistance.

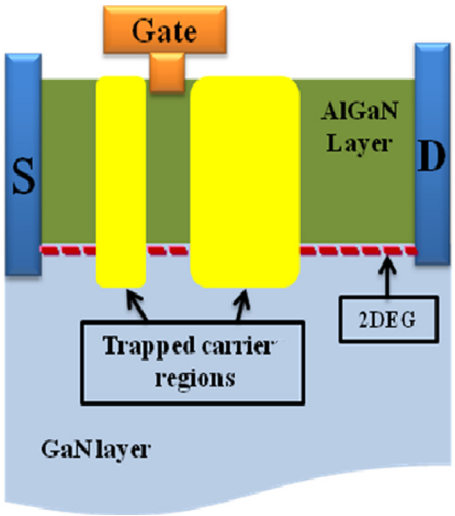

FIG. 2. A schematic section of the HEMT structure showing the regions near the gate edges where the hot electron trapping is most significant (not to scale).

Another hypothesis was presented by Vetury *et al.*,[27] showing that the mechanism responsible for current collapse is related to the formation of a virtual gate that participates in the reduction of the surface-positive charges, by electron trapping. They have shown that this effect can be mitigated or eliminated by using a SiN_x passivation layer, proving that surface states are responsible for this effect. On the contrary, Simin *et al.*,[28] have shown, by pulsed measurements on the gate, that the current collapse is directly linked to the increase of the gate-source and gate-drain series resistances and not to the increase of the channel resistance under the gate. They proposed a model combining the increase of these series resistances with the decrease of the piezoelectric effect resulting from the gate polarization, which induces a non-uniformity of the tensile strain of the AlGaN layer. Based on these hypotheses, it is clear that there are some difficulties to locate and identify the traps responsible for this effect.

In order to understand the possible origin of these parasitic effects (kink and collapse effects) observed in our structure, CDLTS measurements have been realized.

IV. CDLTS MEASUREMENTS AND DISCUSSION

Drain CDLTS is a more reliable technique for deep level analysis than the capacitance DLTS because of the small gate capacitance of our transistor. Furthermore, CDLTS under a gate pulse enables one to detect the traps susceptible to be present in the AlGaN barrier layer, at the AlGaN/GaN interface, and also laterally in the access zones between gate-source and gate-drain.

CDLTS measurements were performed by applying a gate pulse V_{gs}, on the $Al_{0.25}Ga_{0.75}N/GaN/SiC$ HEMT, switching from 0 to -3 V at $Vds = 5$ V with a rate window (e_n) of $39.8\ s^{-1}$ and a filling pulse width $t_p = 100$ ms. As shown in Fig. 3, we notice the presence of two electron traps named A_1 and A_2, and one hole trap labeled H_1. To determine the apparent activation energy and the capture cross section for each trap, the temperature dependence of the thermal emission rate (Arrhenius diagram) was plotted, as shown

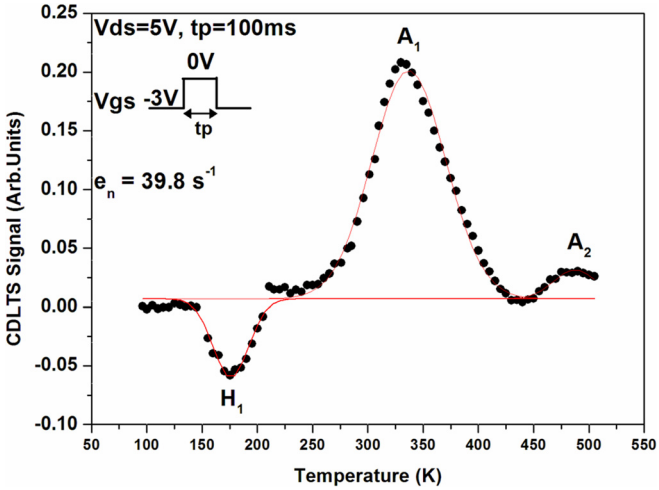

FIG. 3. CDLTS spectra measured after a gate pulse on the AlGaN/GaN/SiC HEMT, showing the presence of three levels H_1, A_1, and A_2.

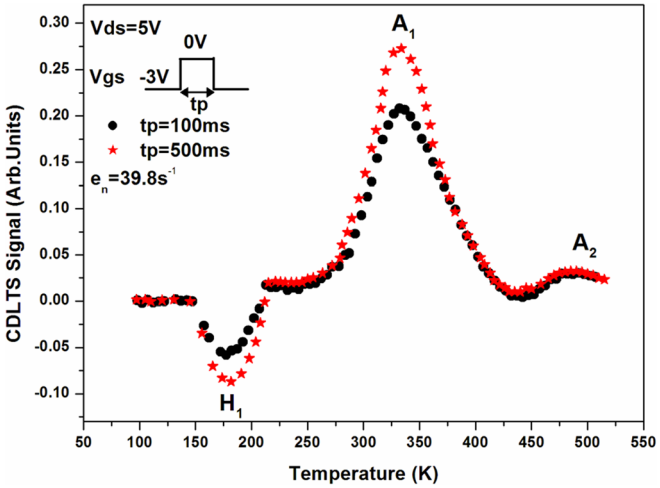

FIG. 5. CDLTS signal for different filling pulse widths (tp).

in Fig. 4. The activation energies (Ea) and the capture cross-sections (σ) of these traps evaluated from these Arrhenius diagrams are 0.56 eV and 2.35×10^{-14} cm^2 for A_1, 0.82 eV and 2.62×10^{-15} cm^2 for A_2, 0.75 eV and 2.80×10^{-15} cm^2 for H_1.

For a correct estimation of the trap nature, it is important to realize CDLTS measurements for different filling pulse width (t_p). Indeed, if there is a variation in the trap concentration when the filling pulse width increases, it can be inferred that the trap has a specific behavior, such as time-dependent Coulomb barrier that limits the electron capture by traps distributed along line defects (dislocations) in the crystal.[29]

By varying the filling pulse width (t_p) from 100 to 500 ms, CDLTS spectra [Fig. 5] indicate that trap A_2 behaves as a punctual defect (impurity or intrinsic defect) because there is no change in the CDLTS peak height when t_p increases. However, the two peak heights of A_1 and H_1 have increased with the filling pulse width. This behavior is due to the extended character of these defects (threading dislocations or stacking faults) which may be introduced into the structure during the growth process.

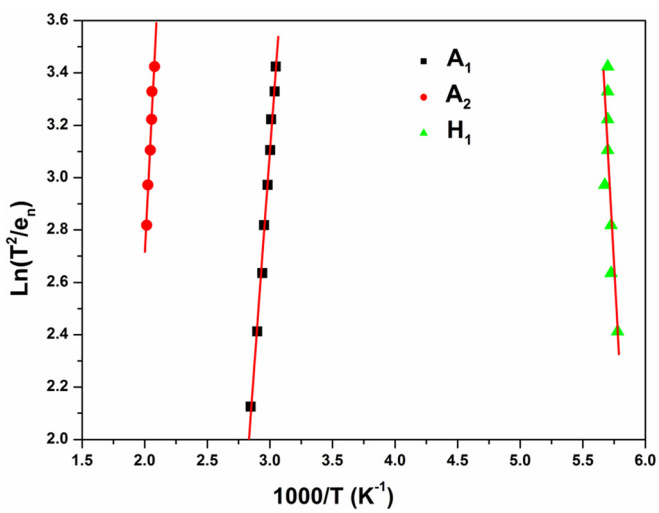

FIG. 4. Arrhenius diagrams plotted for the three levels observed on the CDLTS spectrum.

The Arrhenius fit, shown in Fig. 4, indicates an activation energy of 0.56 eV for the electron trap A_1. This level was also observed by Legodi *et al.*,[30] in $Al_xGa_{1-x}N$ with an activation energy of 0.567 eV for $x = 0.41$ and 0.537 eV for $x = 0.12$. Joh *et al.*,[31] have found this electron trap in the AlGaN layer with an activation energy of 0.57 eV and suggest that it is responsible for the device performance degradation. Indeed this trap becomes a pathway for electrons to flow from the gate down to the channel. If this trap gets filled with electrons, their electrostatic influence partially depletes the electron charge in the channel and decreases the maximum drain current. This defect is associated to an extended defect, such as line defect which is probably due to threading dislocations in the AlGaN/GaN heterostructure. On the other hand, the Kink current evolution as a function of temperature at $Vgs = -3$ V [Fig. 6(a)], shows the presence of one peak observed at 300 K. At the same time, the current collapse values at each temperature (from 100 to 550 K) for $Vgs = -3$ V and $Vds = 5$ V, as shown in Fig. 6(b), reveals that this effect is more significant in the temperature range from 150 to 400 K with a maximum approximately at 325 K. Knowing that A_1 appears at the same temperature where the current collapse and the Kink effect are more significant, we can then deduce that this level seems to be responsible for the appearance of these phenomena.

The detected defect, labeled A_2 (Ea = 0.82 eV) is similar to the electron trap observed by Kindl *et al.*[32] (Ea = 0.83 eV) in GaN/AlGaN/SiC heterostructures obtained by the capacitance DLTS technique. This level was also detected by Gassoumi *et al.*[33] (Ea = 0.83 eV) in AlGaN/GaN/Si HEMT using the current DLTS technique. Götz *et al.*,[34] have also reported this defect with an activation energy of 0.83 eV, found in Si-doped $Al_{0.12}Ga_{0.88}N$ grown on the SiC substrate, which is associated with a native defect. Based on the experimental conditions $Vds = 5$ V and $Vgs = -3$ V, we have suggested that the analyzed region was located from the gate/AlGaN interface up to the channel from the drain side. Also, we have demonstrated that the trap A_2 presents a punctual

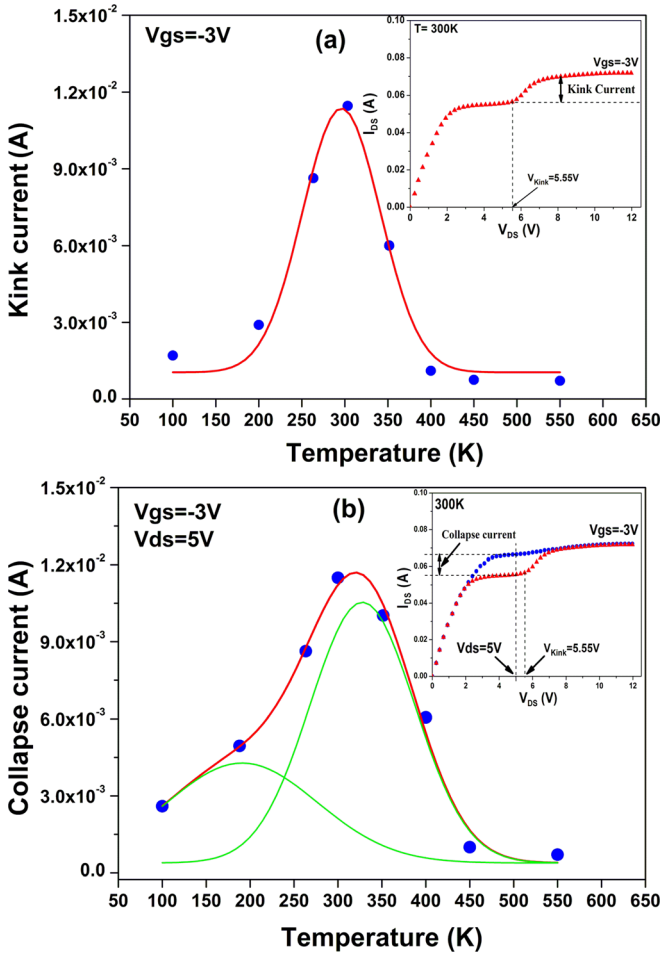

FIG. 6. Variation of the kink current at Vgs = −3 V (a) and the current collapse obtained at Vgs = −3 V and Vds = 5 V (b) as a function of the temperature. Inset: diagrams showing the kink current (a) and the collapse current (b).

character, i.e., it can be located either on the free gate-drain surface, metal/AlGaN interface or in the AlGaN/GaN interface.

Finally, to our knowledge it is the first time that the H_1 (Ea = 0.75 eV) hole trap was observed in the AlGaN/GaN heterostructures using the current DLTS technique and which appears at a temperature varying from 155 to 210 K. From the evolution of the current collapse as a function of the temperature [Fig. 6(b)], we notice the presence of a second peak in the same range of temperature. We can then attribute the collapse effect to the presence of this defect. Additionally, this level may be related to an extended defect in the $Al_{0.25}Ga_{0.75}N$/GaN heterostructure, such as threading dislocations. This idea was proved by the increase of the H_1 peak height appreciably by changing the filling pulse width from 100 to 500 ms.

This defect may only be the level observed by Saadaoui *et al.*,[15] in the $Al_{0.25}Ga_{0.75}N$/GaN/SiC Schottky barrier diode using the capacitance DLTS technique. We have shown[15] that this defect is the main cause of the appearance of the capacitance hysteresis phenomenon and the large leakage current. This serious gate leakage current observed in the Schottky-gate (Ni/Au)/AlGaN/GaN heterostructure field-effect transistors can assist the electron injection into surface states in the region between the gate and the drain, causing the virtual gating effect on the AlGaN surface which reduces the two-dimensional electron gas density and causes a serious current collapse.[35,36] Knowing that this trap was associated to electron injection from the gate and which will be trapped either inside the AlGaN barrier or at the surface close to the gate, may lead us to highlight the relationship between the capacitance hysteresis phenomenon, the leakage current, the current collapse, and the H_1 hole trap. This explication can be confirmed by the mitigation of the hysteresis phenomenon[37] and the suppression of the leakage current and the current collapse[35] after adding an Al_2O_3 dielectric layer between the (Ni/Au) metal and the AlGaN barrier and in the surface region gate-drain and gate-source. This dielectric layer leads to reduce the surface defect trap and the surface state in the AlGaN barrier.

V. CONCLUSION

To sum up, we have investigated electrical static measurements and defect analysis on the $Al_{0.25}Ga_{0.75}N$/GaN/SiC HEMT transistor. Current voltage drain-source characteristics Ids(Vds) show the apparition of two anomalies: kink and collapse effects. The variation of these parasitic effects as a function of temperature shows that these effects are significant in the temperature range varying from 150 to 400 K with a maximum approximately at 325 K. Defect analysis performed on this transistor by the current DLTS technique proves the presence of three traps labeled H_1, A_1, and A_2. The traps H_1 and A_1, supposed to be the origin of the collapse effect, are extended defects in the $Al_{0.25}Ga_{0.75}N$/GaN heterostructure. However, the trap A_2 is a punctual defect which seems to be located either in the free gate-drain surface, in the metal/AlGaN interface or in the AlGaN/GaN interface. These deep levels, present in the AlGaN/GaN/SiC HEMT transistor, are the main cause of the kink and the current collapse effects observed on the Ids(Vds) output characteristics.

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