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E. Lampin, Q.-H. Nguyen, P. A. Francioso, and F. Cleri
Institut d'Electronique, Microelectronique et Nanotechnologie (IEMN, UMR CNRS 8520), Université de Lille I, 59652 Villeneuve d'Ascq, France

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We use molecular dynamics simulations to study the heat transfer at the interface between crystalline Si and amorphous silica. In order to quantify the thermal boundary resistance, we compare the results of two simulation methods: one in which we apply a stationary thermal gradient across the interface, trying to extract the thermal resistance from the temperature jump; the other based on the exponential approach to thermal equilibrium, by monitoring the relaxation times of the heat flux exchanged across the interface. We compare crystalline Si/amorphous Si vs. crystalline Si/amorphous silica interfaces to assess the relative importance of structural disordering vs. chemistry difference. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3698325]

Power consumption and heat dissipation from integrated circuits is a major factor affecting the performance of microelectronics devices and represents an important concern for energy management and technology development (see e.g., Refs. 1 and 2 and references therein). Although the amount of energy per logic operation is still decreasing, the increasing miniaturization of the transistor elements towards the nanoscale, and the attending increase of clock cycles to tens of GHz, inevitably leads to an explosion of the power density for logic circuits, communication devices, and memory cells. Notably, on its path from source to drain and eventually to the heat sink, the heat flux in a modern device crosses a multitude of materials interfaces, some separated just by nanometric amounts of matter, thus leading to the even more complex subject of heat management at the nanoscale.[3]

Among the many questions that arise in this context, an extremely important one is how the interfaces between electronic material overlayers, with different atomic and chemical structures (most notably, their large differences in density and dielectric constants) could affect the microscopic phonon diffusion and scattering, and thereby the heat flux. It is a widely accepted concept that when a heat flux crosses a bi-material interface, a discontinuity develops in the temperature distribution signaling the existence of a thermal boundary resistance, also called the Kapitza resistance.[4] However, a direct experimental determination of such an effect is often difficult to achieve, because of the need to extract a single interface contribution from a device including several (and equally poorly known) interfaces in series, notably with the metal contacts. For example, the determination of the thermal boundary resistance at Si/SiO_2 interfaces is affected by a rather large scatter of values, going from about 2×10^{-8},[5] to $1.3–0.5 \times 10^{-8}$,[6] down to about 2×10^{-9} K m^2 W^{-1},[7] as a function of the different experimental arrangement. Theoretical estimates, only available within the acoustic-mismatch (AMM) or the diffuse-mismatch (DMM) models,[8] tend to favor the smaller values, 2.4 to 3.5×10^{-9} K m^2 W^{-1}. It is likely that part of the experimental (and theoretical) difficulty in this special case also originates from the very large difference between thermal conductivities of crystalline Si (*c*Si) and amorphous silica (aSiO$_2$), which differ by about two orders of magnitude, $\kappa = 140$ W K^{-1} m^{-1} for *c*Si (Ref. 9) and $\sim$1.5 W K^{-1} m^{-1} for aSiO$_2$ (Ref. 10) at T = 300 K. One first question, therefore, is whether a more definitive value for the thermal boundary resistance of the Si/SiO_2 interface can be assessed.

When noting, furthermore, that the thermal conductivity of aSiO$_2$ is very close to that of amorphous Si (*a*Si), $\kappa \sim 2$ W K^{-1} m^{-1},[11] a second question that could be asked is whether the thermal boundary resistance would be mainly determined by purely microstructural factors (the order-disorder phase change from crystal to amorphous which, in the case of *c*Si to *a*Si, have very similar density and bonding), or by the physico-chemical properties (the quite different density and bonding character of aSiO$_2$ compared to *a*Si). Such observations motivated the present study, in which we used atomistic molecular dynamics computer simulations, to extract and compare the thermal boundary resistance of model *c*Si/aSiO$_2$ and *c*Si/*a*Si planar interfaces.

To describe interatomic forces, we chose one of the Si–Si potentials proposed by Tersoff[12] and extended to Si–O and O–O interactions by Munetoh *et al.*[13] Although not explicitly including information about the ionic character of oxygen bonding, this parameterization is found to give a very good description of aSiO$_2$. The bulk aSiO$_2$ structure was obtained from a β-cristobalite SiO$_2$ supercell, upon annealing at very high temperature ($T > 4000$ K) followed by rapid quenching from the melt.[14] The radial and angular bond distributions in bulk aSiO$_2$ at equilibrium are very close both to the theoretical calculations by Munetoh,[13] and by the well assessed van Beest, Kramer, and van Santen (BKS) potential.[14,15]

We constructed our *c*Si/aSiO$_2$ planar interface structures as a periodic-slab geometry, by putting into contact two halves of a supercell made, respectively, of bulk *c*Si and bulk aSiO$_2$, with identical cross section in *xy*, and much elongated along the perpendicular *z* direction. Periodic borders were imposed along the *x*, *y*, and *z* directions. In order to allow the formation of a well-equilibrated interface, the initial *z*-distance between the *xy* planar surfaces of the *c*Si

block (oriented along {001}) and the aSiO$_2$ block was set to 2 Å. A succession of {NPT} and {NσT} equilibration runs was performed, during which interatomic bonds formed at the interface, while the total z-length of the supercell was minimized independently from the rest of the canonical variables. Each of these annealing cycles was made of a ramp-up from 0 to 2000 K and a ramp-down to 500 K, in steps of 100 K, for a total simulation time of 35 ns, for each supercell size. After the equilibration procedure, oxygen atoms could be found at a symmetric position between two Si atoms, both at the cSi surface, forming a so-called Si–O–Si bridge;[14,16,17] or, an oxygen atom can connect a Si atom from the cSi surface to a Si in the aSiO$_2$ matrix. According to our previous study,[14] we call these latter Si–O*–Si bridges, to underscore the fact that the O atom in this case may be displaced in a non symmetric position with respect to the two Si atoms.

For the subsequent comparison, cSi/aSi interface structures were also constructed by using the same procedure above, except that the amorphous block was formed by quenching a molten silicon crystal, with a procedure known to result in bulk aSi of good quality.[18]

In a first attempt to determine the thermal boundary conductance of the interface, we performed standard non-equilibrium molecular dynamics (NEMD) calculations.[19] Elongated samples were constructed, half of the total length in the z direction being cSi, while the remaining half being either aSi or aSiO$_2$. After each sample was equilibrated at 500 K, a heat source ($T = 550$ K, z-thickness 22 Å) was introduced at mid-length of the cSi block, while a heat sink ($T = 450$ K and 22 Å) was set at mid-length of the amorphous block. After another 100 ps of stabilization of the thermal gradient along the z-direction of the supercell, the temperature profile was recorded in slices of 2 Å-width, and averaged during 1 ns, to ensure a good convergence. Figure 1 displays the temperature profiles for the two interfaces for a 98 nm-long system with cross-section of 19 nm^2 (~114 000 and ~91 000 atoms for cSi/aSiO$_2$ and cSi/aSi, respectively). The temperature profile is nearly flat in the cSi part and exhibits a steep slope in aSi or aSiO$_2$, due to the much higher thermal conductivity of cSi compared to both aSi and aSiO$_2$. The latter material shows a substantial nonlinearity of the temperature profile close to the interface. However, neither of the two temperature profiles shows an appreciable drop at the interface, differently from what is usually observed for other interfaces.[19,20] This could be due to the large difference in thermal conductivity on each side of the interface, leading to a larger temperature difference in the less conductive block (aSi or aSiO$_2$), which could hide the effect of the interface itself. Another possibility would be that the temperature drop does not exist at all, in this case. Notably, the only previous attempt of MD simulation of thermal resistance for the Si/SiO$_2$ interface[21] (however carried out on much smaller and rather poorly equilibrated atomic systems, and for much shorter simulation times) obtained similarly dubious results, reporting an upper limit of $\sim 0.5 \times 10^{-9}$ K m^2 W^{-1}. Indeed, the extraction of an interface temperature in such extreme conditions shows one of the limitations of the NEMD method, namely the need to define temperature differences over lengths much smaller than the typical phonon mean free path, besides the difficulty of imagining a physical gradient of $>10^9$ K/m over such a nm-thin region, and the need to estimate the absolute thermal energy flux during the same simulation.

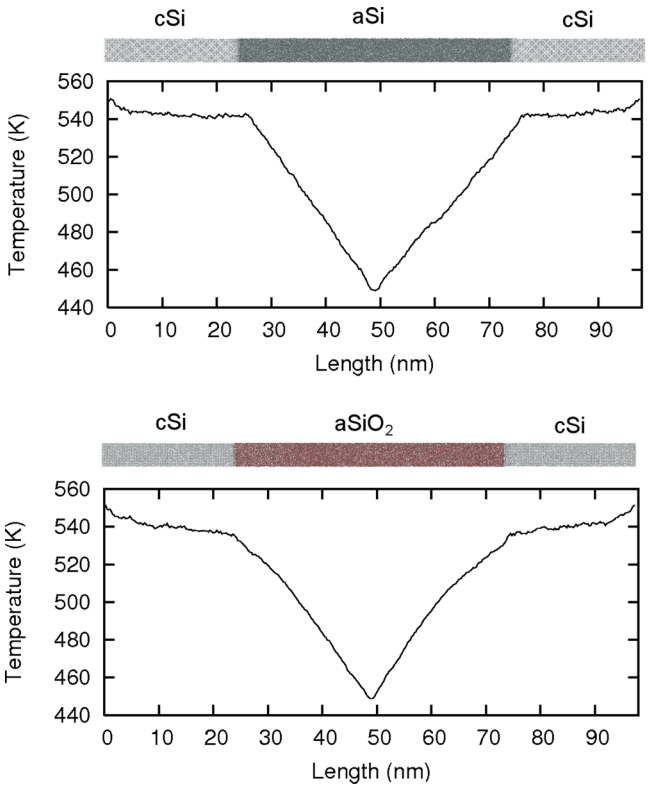

FIG. 1. Temperature profile along the direction perpendicular to the interface, averaged over 1 ns NEMD. Upper panel: cSi/aSi. Lower panel: cSi/aSiO$_2$.

In order to circumvent at least some of the above difficulties, we introduced a different kind of MD simulations, which rather relies on the extraction of the bulk temperature from each of the two homogeneous half-blocks, therefore averaging over much larger regions, up to about 150 nm. Ideally, we start by instantaneously bringing one of the two sides of the interface at a higher temperature than the other, $\Delta T = T_2 - T_1$ at $t = 0$ (note that, in MD simulations, "instantaneously" means anyway a time of the order of fractions of ns). Subsequently, the transitory equilibration of ΔT to a common temperature value is followed, as a result of the heat transfer through the interface. Such a procedure is akin to the experimental laser-flash method[22] (applicable with some variant also down to nanostructured materials[23]) in which a highly-localized temperature transient is impulsively created and monitored in time.

For this "approach-to-equilibrium" MD (or AEMD) method, the cSi block was first equilibrated at 600K and the aSi or aSiO$_2$ block at 400 K, during 100 ps. The bi-material system was then left free to attain the thermal equilibrium under {NVE} constraints. Therefore. the total energy was conserved, and the system could reach an average temperature determined by the ratio of the total mass times the heat capacity of the two materials. In practice, the ensemble-averaged, instantaneous temperature of each subsystem (cSi, aSi, and aSiO$_2$) was recorded during each AEMD simulation, and the decay of the temperature difference, $\Delta T(t) = T_C(t) - T_X(t)$ ($C = c$Si; $X = a$Si or aSiO$_2$), could be estimated after each AEMD run. In the single-exponential limit,

$\Delta T(t) \propto \exp(-t/\tau)$, it can be shown that the overall thermal boundary conductivity is obtained as

$$\frac{1}{g} = \frac{1}{C_V}\int_0^\infty \frac{\Delta T(t)}{\Delta T(0)}dt = \frac{\tau}{\bar{q}(3Nk_B)}. \quad (1)$$

The dimensionless heat capacity, $\bar{q} = C_V/3Nk_B$, accounts for the quantum-mechanical corrections to the specific heat capacity C_V, for temperatures $T < \Theta_D$ below the Debye limit. Note that we wrote Eq. (1) for the conductivity, rather than for the resistance, since g is the fundamental property of the interface (see the analogy between *incident* phonon flux on the two sides of the interface, and the radiation equilibrium between two blackbodies, as nicely discussed in Ref. 24).

For a given system size in our geometry, the total thermal conductance G of the system (conductivity normalized by the cross section S) is the sum of three contributions, assumed to act in series

$$\frac{1}{G} = \frac{L_C}{\kappa_C} + 2R_i + \frac{L_A}{\kappa_A} \quad (2)$$

namely, the thermal resistance of the crystalline Si block, with z-length L_C and thermal conductivity κ_C; the thermal resistance of the amorphous block, with thermal conductivity κ_A and z-length L_A; and the thermal boundary resistance, R_i, doubled because of the periodic border conditions. The thermal conductivity of crystalline Si being much larger than any of the amorphous blocks, for $L_A \sim L_C$ the contribution of the last term in Eq. (2) becomes predominant, and hides the interface resistance. Therefore, in order to extract the value of R_i, the length of the amorphous block was made variable and limited to relatively small values ($L_A = 5$, 10, 15, and 36 nm, in a series of different AEMD simulations), whereas the length of the crystal block was kept constant, at a size comparable with the phonon mean free path in pure Si ($L_C \sim 150$ nm). In this way, the data for $1/G$ can be plotted versus the length L_A, with the linear fitting giving the amorphous conductivity, κ_A, as the slope of the straight line, while the extrapolated intercept at $L_A = 0$ gives the term $L_C/\kappa_C + 2R_i$.

Examples of the time-decay of the temperature difference for the cSi/aSiO$_2$ interface are shown in Fig. 2 in a semi-log plot, for the four values of L_A. The approach to equilibrium appears to follow a single decaying exponential, within the statistical noise. In retrospect, the straight lines of Fig. 2 demonstrate that the conditions for the applicability of Eq. (1) are indeed met, for our bi-material interfaces.

In Figure 3, we report the linear fits of the $1/G$ values obtained for the two kind of interfaces, plotted versus L_A. The heat capacities to be plugged in Eq. (1) are evaluated in the Debye model framework, using Debye temperatures of 645 K for cSi, 528 K for aSi (Ref. 25), and 511 K for aSiO$_2$.[26] The error bar associated to the extraction of R_i by the AEMD method is of the order of $\sim$1%, since the determination of the key value in Eq. (2), the decay time τ, is carried out on the logarithmic evolution of $\Delta T(t)$ over more than a decade and is therefore quite accurate. Tests performed on different atomic structures of the cSi/aSiO$_2$ interface (obtained by different annealing and relaxation cycles, with different initial conditions) showed but a very minor impact on the actual value of thermal boundary resistance.

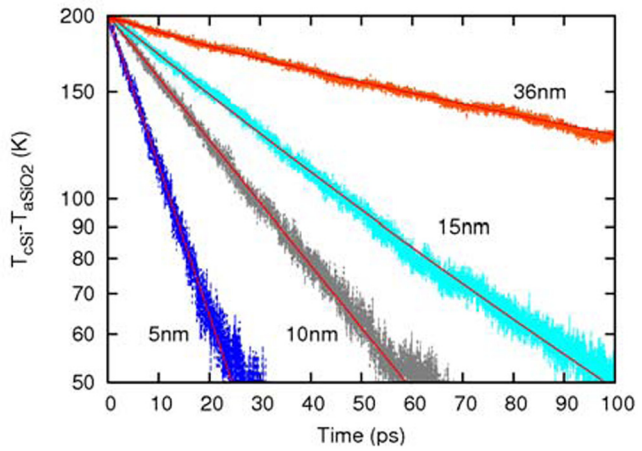

FIG. 2. Semi-log plot of the temperature difference ΔT *vs.* time, from {NVE} molecular dynamics with the AEMD method, after initial equilibration at 600K (cSi) and 400 K (aSiO$_2$). Cross section 19.4 nm^2; constant crystal block length, $L_C = 150$ nm; variable silica block length, $L_A = 5$, 10, 15, and 36 nm. The single-exponential decay times extracted by linear fit (red lines) are: $\tau = 18$ps for $L_A = 5$ nm; 42 ps for 10 nm; 71 ps for 15 nm; and 245 ps for 36 nm.

The linear dependence of $1/G$ against L_A is quite well verified in Fig. 3, except for the smallest sizes where the simple approach of series resistance summation assumed in Eq. (2) is no longer valid. The slope of the linear fit is the inverse of κ_A and gives similarly low values for both amorphous materials, i.e., $\kappa_A = 7.3$ W K^{-1} m^{-1} for aSiO$_2$ and 6.5 W K^{-1} m^{-1} for aSi ($T = 500$ K). While being in the right order of magnitude, both such values overestimate the experimental data cited above, likely because of the non-ideal purity of experimental samples. In the same figure, we also report the equivalent thermal resistance $R_C = L_C/\kappa_C = 0.937 \times 10^{-9}$ K m^2 W^{-1}, of a cSi block having the same length ($L_C = 150$ nm), with $\kappa_C = 165$ W K^{-1} m^{-1} obtained from a separate bulk cSi simulation at $T = 500$ K. Such a slightly higher value of κ_C, compared to the experimentally accepted one for bulk Si, $\kappa_C = 120$ W K^{-1} m^{-1}, is consistent with the

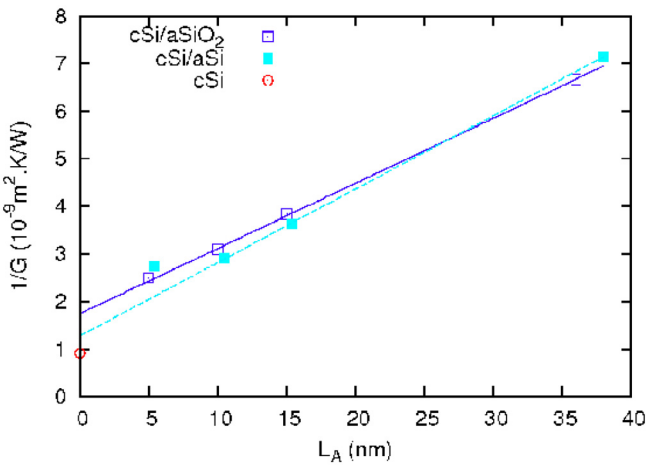

FIG. 3. Inverse conductance ($1/G$) of cSi/aSiO$_2$ (□) and cSi/aSi (■) interfaces, plotted vs. the length of the amorphous block L_A. The red circle at $L_A = 0$ indicates the thermal resistance of a perfect bulk cSi slab with $L_C = 150$ nm.

fact that L_C is not yet at the convergence limit for the maximum phonon mean free path. We note that this discrepancy, however, does not affect the extraction of the R_i value from the sum in Eq. (2).

By looking again at Fig. 3, the thermal boundary resistance is the difference between the $1/G$ value extrapolated at $L_A = 0$ and the R_C previously defined, clearly showing the existence of a finite, *albeit* small, thermal boundary resistance. The value of R_i is very low for both interfaces: 0.4×10^{-9} K m^2 W^{-1} for cSi/aSiO$_2$ and 0.2×10^{-9} K m^2 W^{-1} for cSi/aSi. Such small values are compatible with the difficulty of identifying a temperature drop by using the NEMD approach and with the DMM model estimate,[8] when considering that the latter usually represents an upper bound to the thermal boundary resistance. As difficult as it is to discriminate between the roles of atomic structure and chemistry, it seems however that the change of density and chemistry between amorphous-Si and amorphous-SiO$_2$ has a relevant impact, since the respective values of thermal resistance differ by a factor of 2.

The equivalent thickness of aSiO$_2$ corresponding to the thermal boundary resistance can be estimated from the product $\kappa_A R_i \sim 3$ nm and will be negligible for most of silicon-on-insulator (SOI) technologies using 100 to 400 nm-thick buried oxide (BOX). The impact will be significant for most advanced technologies, such as UTB^2 (ultra-thin body and box) SOI (Ref. 27) with an increase of the effective thickness of the barrier for heat path from 10 nm (oxide thickness) to about 16 nm (oxide thickness + equivalent thickness of the double cSi/aSiO$_2$ interface). In this extreme case, however, the total thickness will remain low and the heat dissipation efficient enough.

In conclusion, we introduced an alternative approach for atomistic molecular dynamics simulations (AEMD) based on the study of the transient response to a large-scale thermal discontinuity. The method, inspired to laser-flash measurements of thermal diffusivity and generally applicable under Newtonian heat flow conditions, was employed to extract the thermal boundary resistance in the difficult case of a bi-material interface between a very good and a very poor thermal conductor. The AEMD method turns out to be simpler than other methods requiring the estimation of the absolute thermal flux and avoids the need to define a local "temperature," over a nanometric quantity of matter much smaller than the phonon mean fee path. Moreover, it is computationally faster than other relaxation-time methods based, e.g., on the calculation of autocorrelation functions, and numerically very precise, since the key value is the exponential decay time of a quantity measured over several decades. Therefore, the AEMD approach could be an interesting alternative to extract thermal boundary resistance in other, more general cases. When applied to the technologically important cSi/aSiO$_2$ interface, a very low value of the thermal boundary resistance is found, but large enough to significantly alter the heat dissipation characteristics in the case of ultra-thin buried oxide layers.

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