Low-frequency noise in Schottky-barrier-based nanoscale field-effect transistors

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Nicolas Clément, Guilhem Larrieu, and Emmanuel Dubois

***Abstract*—Investigation of low-frequency noise in nanoscale Schottky-barrier (SB)-based field-effect transistors (SB-FETs) is of prime importance due to its large amplitude in emerging bottom-up devices. In addition, noise can give additional information on charge transport mechanisms. In this paper, we study the $1/f$ noise in nanoscale silicon-on-insulator SB-FETs. An unexpected feature is the clear contribution of the SB to the noise even if the barrier height is lower than 100 meV. Barrier modulation techniques such as dopant segregation are used to tune the barrier height. We propose a generic formulation for low-frequency noise that is applicable to any diffusive SB-FETs.**

***Index Terms*—Low-frequency noise, nanodevices, Schottky barriers (SBs), silicon-on-insulator (SOI).**

I. Introduction

AMONG THE MAIN difficulties to overcome toward decananometer metal–oxide–semiconductor (MOS) field-effect transistor (FET) (MOSFET) technologies, many challenges concentrate on source/drain (S/D) regions. As mentioned in the Emerging Research Materials section of the 2009 International Technology Roadmap for Semiconductors [1], when devices approach the nanometer scale, electrical contacts may need to be formed without degenerately doping the semiconductor contacts. This challenging problem has reactivated a considerable interest on low Schottky barriers (SBs) for the formation of reliable contacts to semiconductor nanowires and extremely thin bodies [1]. In that context, SB-based FETs (SB-FETs) constitute a seducing approach because of the significant process simplification (no ion-implantation strategy and high-temperature activation) [2]. Beyond the sole consideration of MOS device downscaling, most of emerging bottom-up devices that have been identified as potential "beyond CMOS" solutions, including carbon nanotubes [3], [4], graphene sheets [5], and semiconductor-nanowire-based transistors [6], belong to the family of SB-FETs. Because of the renewed interest in Schottky S/D technology, deep understanding of electron/hole transport at the Schottky junction in a transistor configuration becomes of prime importance. In this paper, we demonstrate that the analysis of low-frequency noise in silicon-on-insulator (SOI)-based SB diodes and SB MOSFETs unveils new insights in physical mechanisms related to electronic transport through SBs. In addition, low-frequency noise in SB Si MOSFETs has barely been studied [7]. For that sake, unmodified and dopant-segregated Schottky junctions that reduce SB height are considered. Although an extra noise contribution comes from the SB, the noise level is comparable to usual MOSFETs at high-enough drain voltage (> 0.2 V). We propose a generic formulation for low-frequency noise that is applicable to any diffusive SB-FETs.

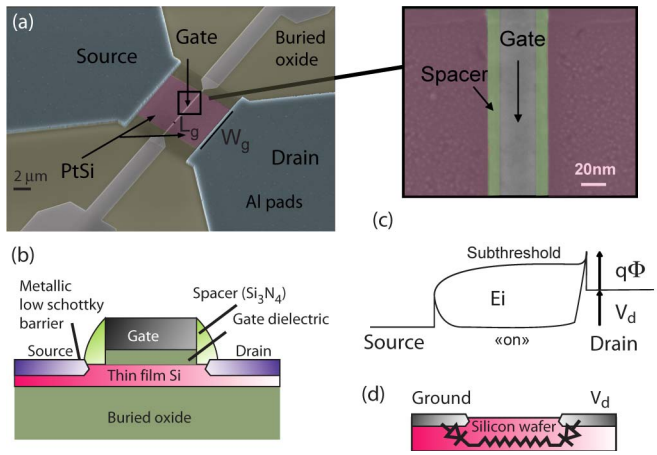

Fig. 1. (a) Scanning electron microscope image of an SOI SB-FET used in this study. The gate length L_g is tuned from 30 nm to 1 μm. A zoom centered on the gate shows the tungsten gate separated to the PtSi S/D contact by slim silicon nitride spacers. (b) Cut view of the transistor. The SBs are located at the transition between the metallic S/D and the thin Si film. (c) Schematic energy band diagram for an n-type SB-FET in the subthreshold and "on" regimes. ϕ is the SB height; V_d is the drain voltage. The source is grounded. (d) Schematic view of the Schottky junction test structure.

II. Experimental Section

A. Sample Manufacturing

A scanning electron microscope image of an SB MOSFET used in this study is shown in Fig. 1(a), and the related schematic cross-sectional view is shown in Fig. 1(b). The fabricated transistors (n- and p-types) feature a tungsten metal gate with a length L_g between 30 nm and 1 μm and a fixed

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TABLE I
ESTIMATED VALUES OF ϕ (IN MILLIELECTRONVOLTS) FOR THE MEASURED DEVICES

Symbol	N	P
Pure Schottky	860	150
With dopant segregation	80	50

width W_g of 6 μm. The gate dielectric is a thermally grown 2.3-nm-thick SiO_2 oxide.

The 15-nm-thick lowly doped (5×10^{15}) SOI film is contacted with the metallic PtSi SBs to form the source and drain contacts. SBs based on platinum silicide offer both a low SB on p-type silicon and a high SB on n-type silicon. Barrier engineering using the dopant segregation technique [8], [9] is also implemented to get a reduced SB height using an implant-through-silicide approach where dopants are confined in the silicide layer coupled with a thermal postactivation (600 °C) to segregate the impurities at the silicide/silicon interface. Arsenic- [9] and boron-segregated [8] PtSi contacts have been implemented for n- and p-type contacts, respectively. Detailed description of the fabrication process is reported elsewhere [10].

A typical energy band diagram for an n-type SB-FET in the subthreshold regime and in the ON state is shown in Fig. 1(c). The key parameters are the SB heights to electrons ($\phi_{\rm bn}$) and to holes ($\phi_{\rm bp}$) that are complementary over the semiconductor bandgap. The injection of carriers takes place through thermionic and tunneling emissions over and through the barrier, respectively. The experimental protocol used for the barrier height extraction couples experimental data from back-to-back diode structures with a transport model including thermionic emission, tunneling emission, and barrier lowering due to image charge induction [11]. To simplify the notation, ϕ refers to the electron ($\phi_{\rm bn}$) or the hole ($\phi_{\rm bp}$) SBs depending on the n- or p-type doping of the underlying substrate. A schematic view of the Schottky junction test structure is shown in Fig. 1(d). It is composed of two back-to-back diodes separated by a series resistor corresponding to the micrometer gap (~ 5 μm) separating the contact edges. By sweeping V_d from a negative to a positive voltage, the system permanently involves one forward-biased junction while the other operates in reverse mode. The values for ϕ are reported in Table I.

B. Low-Frequency Noise Measurements

Electrical measurements were performed at room temperature under vacuum ($< 10^{-5}$ mbar). Drain voltage V_d, gate voltage V_g, and back-gate voltage $V_{\rm bg} = 0$ V were applied with an ultralow-noise dc power supply (Shibasoku PA15A1). The source current was amplified with a DL 1211 current preamplifier supplied with batteries. Random telegraph signal (RTS) data and noise spectra were acquired with an Agilent 35670 dynamic signal analyzer. A detailed protocol for our noise measurements is shown in [12].

III. LOW-FREQUENCY NOISE MODELS

A. Equations for $1/f$ Noise in FETs

The relation known as the Hooge formula was proposed decades ago to describe the $1/f$ noise in metals and semiconductors [13]

$$\frac{S_I}{I^2} = \frac{\alpha_H}{Nf} \tag{1}$$

where S_I is the power spectrum current noise, I is the dc current, α_H is Hooge's empirical parameter, N is the total number of carriers, and f is the frequency. α_H is often used as a figure of merit to compare devices. In high-quality materials such as epitaxial layers [14], α_H ranges in the $[10^{-6}, 10^{-4}]$ interval. In nonoptimized materials, including emerging materials, $\alpha_H = 2 \times 10^{-3}$ is a representative average figure [15]. Strictly speaking, Hooge's parameter is suitable only in the case of mobility fluctuation of carriers, e.g., noise coming from the scattering of free electrons [16].

Due to interfacial effects with gate oxide, noise in MOSFETs at low frequency is often described by [17]–[19]

$$\frac{S_I}{g_m^2} = \frac{q^2 N_{\rm ot}}{C_g^2 W_g L_g} \frac{1}{f} \tag{2}$$

where g_m is the transconductance, q is the elementary charge, $N_{\rm ot}$ is the oxide trap density, C_g is the gate capacitance per surface unit, and W_g and L_g are the gate width and length, respectively. It is generally interpreted as a superposition of random events of charge trapping and detrapping from defects randomly distributed in the gate oxide near the semiconductor channel (the so-called number-fluctuation theory).

In scaled MOSFETs, the number of electrically active defects is reduced, and the low-frequency noise begins to deviate from the $1/f$ characteristics [20], [21]. In the ideal case where there is no active trap, the dielectric polarization noise can be observed [21]–[23] with S_I scaling also with g_m^2

$$\frac{S_I}{g_m^2} = \frac{2kTtg\delta}{\pi C_g W_g L_g} \frac{1}{f} \tag{3}$$

where k is the Boltzmann constant, T is the temperature, and $tg\delta$ is the dielectric loss tangent. Note that, in (2) and (3), for nanotubes/nanowires, border effects may increase the capacitance [23], and W_g should be replaced by a precisely evaluated effective width.

SB-FETs correspond to a relatively complex case for noise analysis because of the additional presence of SBs. The role of series resistances to $1/f$ noise in FETs has been initially mentioned in [24] and becomes of prime importance as transport in the channel becomes ballistic [25]. Surprisingly, $1/f$ noise in SB MOSFETs has been more studied for emerging materials than for Si SB MOSFETs [7]. In any case, the crucial role of drain voltage has not been pointed out. Here, we derive simple equations for $1/f$ noise in SB diodes and SB-FETs and interpret the result for SOI-based devices at the light of these equations.

B. Equation for Low-Frequency Noise in SB Diodes

Starting from the Richardson expression for thermionic emission [26] and considering that noise is related to a voltage fluctuation across the SB as in the case of tunnel barriers [27], we derive the following expression (see the Appendix for more details):

$$\frac{S_I}{I^2} = A\eta^2 \left(\frac{q}{kT}\right)^2 \frac{1}{\left(1 - e^{-q\eta \frac{V_d}{kT}}\right)^2} \frac{1}{f} + (1-\eta)^2 \frac{\alpha_H}{Nf} \quad (4)$$

where A (in square volts) is a parameter for noise amplitude comparison (see the Appendix). $\eta = R_{\rm SB}/(R_{\rm SB} + R_C)$, where $R_{\rm SB}$ and R_C are the SB and channel resistances, respectively. $\eta = 1$ for n-type SB diodes, and $\eta < 1$ for others, with an exponential increase with ϕ. The first term corresponds to the contribution of the SB to the normalized noise, and the second term corresponds to the contribution of the Si bulk series resistance between diodes (1).

C. Equation for Low-Frequency Noise in SB-FETs

The equation for SB-FETs should not differ much from that of an SB diode in series with a resistor

$$\frac{S_I}{I^2} = A\eta^2 \left(\frac{q}{kT}\right)^2 \frac{1}{\left(1 - e^{-q\eta \frac{V_d}{kT}}\right)^2} \frac{1}{f} + (1-\eta)^2 \frac{S_{\rm Ich}}{I^2} \quad (5)$$

where $S_{\rm Ich}$ is the power spectrum noise of the channel in a FET configuration. Depending on devices' dimensions and quality/material, (1)–(3) could be used as the second term. We select (2) which is often the case for small MOSFETs but not small enough to avoid trapping–detrapping noise contribution (3)

$$\frac{S_I}{I^2} = (1-\eta)^2 \frac{g_m^2 q^2 N_{\rm ot}}{I^2 C_g^2 W_g L_g} \frac{1}{f} + A\eta^2 \left(\frac{q}{kT}\right)^2 \frac{1}{\left(1 - e^{-q\eta \frac{V_d}{kT}}\right)^2} \frac{1}{f}. \quad (6)$$

If we make the hypothesis that the noise is dominated by the very large channel resistance in the subthreshold regime and by the SB in the linear regime, (6) can be simplified to

$$\frac{S_I}{I^2} = (1-\eta)^2 \left(\frac{\ln 10}{S}\right)^2 \frac{q^2 N_{\rm ot}}{C_g^2 W_g L_g} \frac{1}{f} + A\eta^2 \left(\frac{q}{kT}\right)^2 \frac{1}{\left(1 - e^{-q\eta \frac{V_d}{kT}}\right)^2} \frac{1}{f} \quad (7)$$

where the subthreshold swing $S = \ln 10 \cdot nkT/q$ with n is a parameter to account for parasitic capacitances.

IV. Results

A. Low-Frequency Noise in SB Diodes

The typical I–V_d characteristics are shown in Fig. 2(a). Only n-type SB diodes ($\phi \approx 800$ meV) exhibit a clear rectification effect. For the p-type counterpart, the overall conductance of the system remains limited by the silicon series resistance [11], owing to a very low SB height ($\phi < 150$ meV). The power spectrum current noise normalized by I^2 for all diode types is shown in Fig. 2(b). Typical $1/f$ noise is observed for p-type SB without dopant segregation and n-type SB with/without dopant segregation. Conversely, dopant-segregated p-type junctions show a $1/f^2$ dependence at a very low frequency that is often explained in terms of generation–recombination and trapping noise due to the effect of centers located in the space-charge region of the diode [28]. In this study, centers may be related to fluorine coming from the p-type dopant segregation with BF_2 implantation [29], [30] or from Pt50 and Pt60 donor defects [10]. For n-type SB diodes, a white noise corresponding to full shot noise ($2qI$) is superimposed to the $1/f$ noise (further discussed in the Appendix).

Fig. 2(c) shows the normalized noise at 10 Hz for the four types of SB diodes. Considering only the three devices following the $1/f$ law, reasonable fits are obtained with (4) with a set of parameters detailed in caption. The contribution from the resistor's noise $\alpha_H/Nf \sim 6 \times 10^{-20}$ Hz^{-1}, which is much lower than the measured noise, is estimated considering $\alpha_H = 3 \times 10^{-3}$, $N = 5 \times 10^{15}$ cm^{-3} (doping level of SOI), and $f = 10$ Hz. Since the contribution from SB noise (first term) is dominant (strong V_d dependence), we conclude that, even if the resistance is dominated by the silicon substrate [Fig. 2(a)], the noise is coming from the SB. The model proposed in (4) shows a reasonable V_d and ϕ dependence. Higher noise is observed with higher SB height, and the noise can be reduced by increasing V_d.

B. Low-Frequency Noise in SB-FETs

SBs studied above can be inserted at an S/D in a transistor configuration. Due to the very high SB that electrons have to overcome in the case of PtSi-based junctions, n-type transistors feature a very low drive current. Hereafter, only the device that integrates low SB height contacts will be considered. Fig. 3(a) shows an example of static characteristic (I_d–V_g) for a 90-nm gate length measured on dopant-segregated SB n- and p-type transistors. A set of data representative of the noise characteristics of SB-FETs is shown in Fig. 3(b)–(d). It corresponds to a dopant-segregated n-type transistor with a 90-nm gate length. The power spectrum current noise S_I is shown in Fig. 3(b) for various V_g's ranging from 0.1 to 1.5 V and $V_d = 1$ mV. Regardless of the V_g bias, a $1/f$ dependence is observed. Noise at 10 Hz normalized by dc I^2 and g_m^2 is shown in Fig. 3(c) (the I–V curve in the inset). Above the threshold voltage $V_{\rm th} \approx 0.7$ V, this figure outlines that S_I/g_m^2 is not constant, revealing that (2) is not appropriate. A reasonable fit is obtained by considering (7). From the subthreshold region, we estimate $N_{\rm ot} = 7.6 \times 10^{10}$ cm^{-2} considering $C_g \cdot W_g \cdot L_g = 8.6 \times 10^{-15}$ F, $S = 250$ meV, and $f = 10$ Hz, which is a fairly low density of oxide traps. The second term in (7) is confirmed by the regime above the threshold voltage in Fig. 3(c) and by the exponential noise decay with drain voltage in Fig. 3(d), although the I–V_d curve is linear. Note that S_I/I^2 would have been constant in Fig. 3(d) [31] using transistor equations with ohmic contacts (1)–(3).

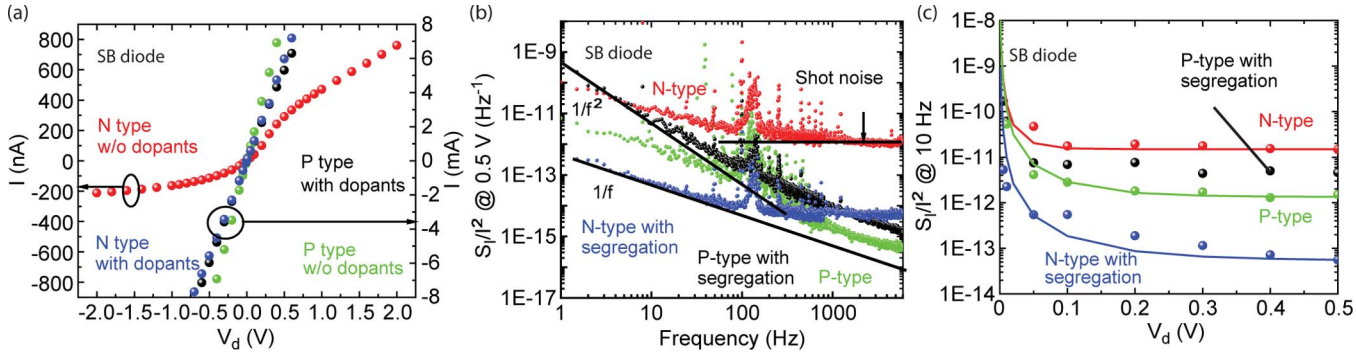

Fig. 2. (a) Current–voltage I–V measurements for the four types of SB diodes with ϕ values reported in Table I. (b) Normalized power spectrum current noise for the four SB diodes. (c) Normalized noise as a function of V_d for the four types of SB diodes at $T = 293$ K. The fits are obtained using (4) with $\eta = 1$ and $A = 3.2 \times 10^{-7}$ for normal n-type SB diodes, $\eta = 0.3$ and $A = 3.2 \times 10^{-7}$ for normal p-type SB diodes, $\eta = 0.2$ and $A = 9.5 \times 10^{-8}$ for n-type SB diodes with dopant segregation, and $\eta = 0.15$ and $A = 7.9 \times 10^{-7}$ for p-type SB diodes with dopant segregation. $\alpha_H = 3 \times 10^{-3}$, $N = 5 \times 10^{15}$ cm^{-3}, and $f = 10$ Hz.

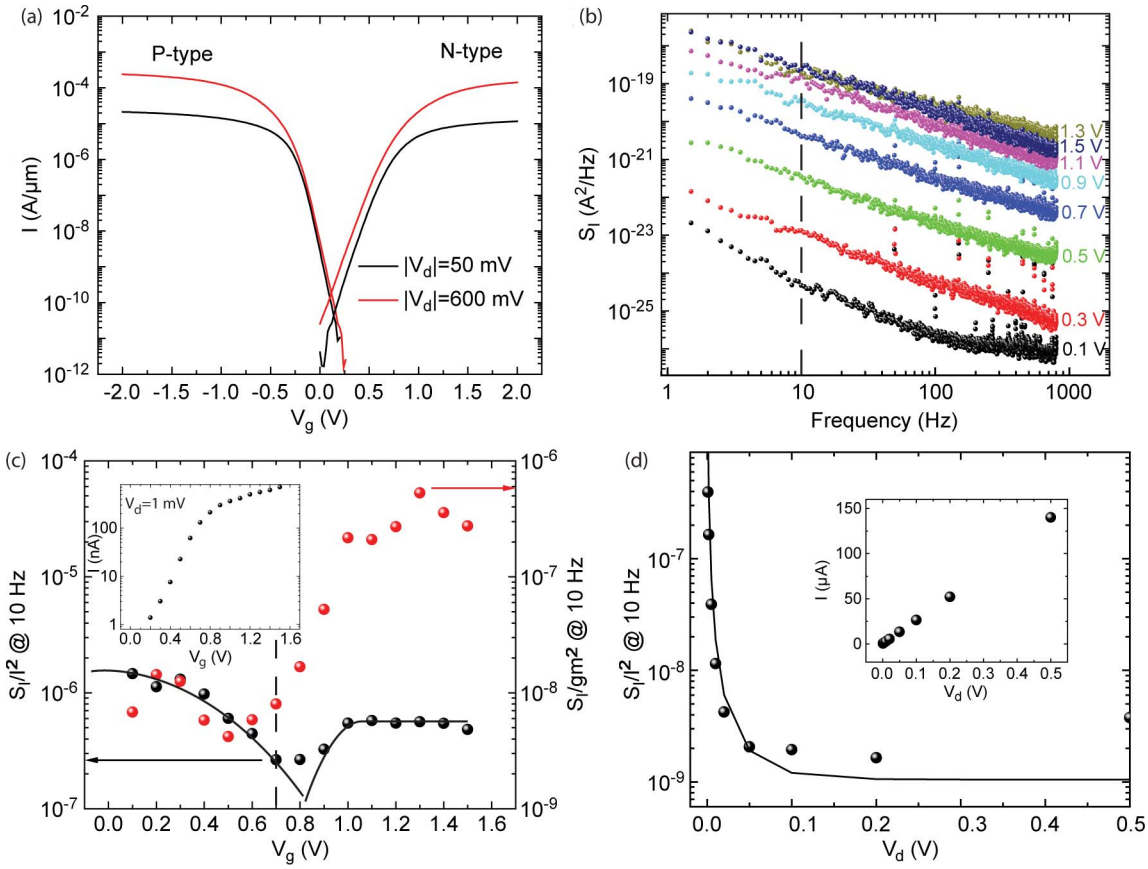

Fig. 3. (a) I–V_g curves for segregated SB-FETs with $L_g = 90$ nm and $V_d = 50$ and 600 mV. (b) Power spectrum current noise S_I for an n-type SB-FET with dopant segregation ($L_g = 90$ nm and $W_g = 6\ \mu$m). (c) S_I, normalized by (black) I^2 and (red) g_m^2, is plotted as a function of V_g. $V_d = 1$ mV. The corresponding I–V_g curve is shown in the inset. The fit is obtained using (7) with η a fitting parameter ranging from 0 to 0.5 in the subthreshold regime and from 0.5 to 0.7 in the "on" regime. $A = 3.8 \times 10^{-6}$. The dashed line indicates the threshold voltage. (d) S_I/I^2 as a function of V_d. $V_g = 1.2$ V. The fit is obtained using (7). The corresponding I–V_d curve is shown in the inset. The same parameters as those in (c) are considered: $\eta = 0.7$ and $A = 3.8 \times 10^{-6}$.

In order to investigate the dominant source of noise at high-enough drain voltage (when V_d dependence is suppressed), we plot I_d [Fig. 4(a)] and normalized noise [Fig. 4(b)] for various L_g's at fixed (V_d, L_g). As shown in Fig. 4(a), the current increases inversely with the gate length for the two SB-FETs with dopant segregation [8], as expected for small barrier heights. Normalized noise dependence with scaling is different between segregated n- and p-type devices. There is almost no dependence for the n-type ($\phi \approx 80$ meV), but for the p-type ($\phi \approx 50$ meV), it scales inversely with L_g. The natural explanation for such difference is that the SB is the limiting noise source for the n-type even at high-enough drain voltage (0.2 V), which is not the case for segregated p-type SB-FETs, with a conventional L_g dependence.

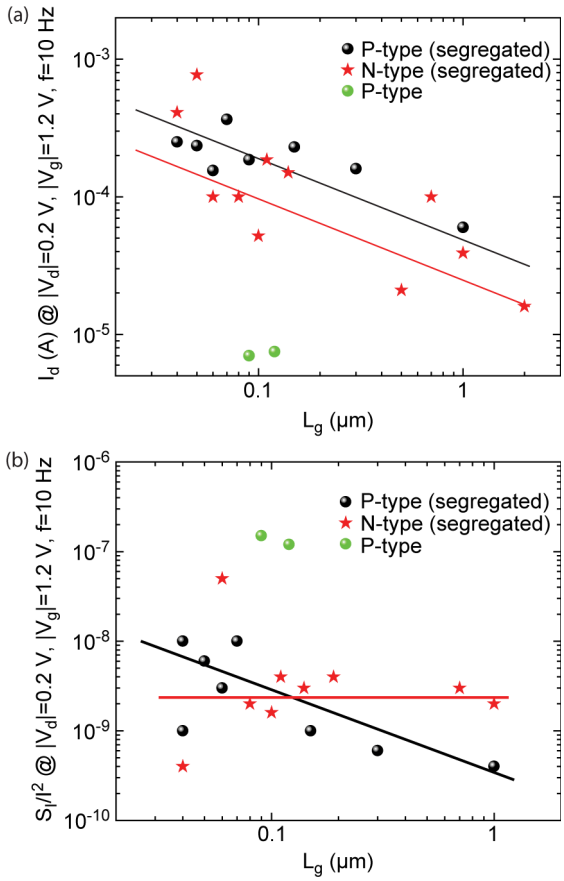

Fig. 4. (a) I at $|V_d| = 0.2$ V and $|V_g| = 1.2$ V for p-type SB-FETs with/without dopant segregation and n-type SB-FETs with dopant segregation is plotted as a function of the gate length L_g. (b) Normalized noise S_I/I^2 at 10 Hz related to I shown in (a).

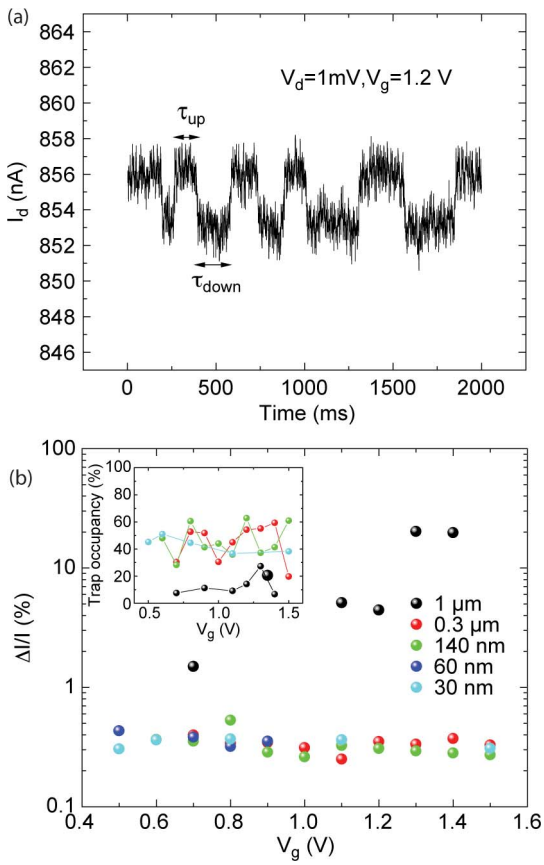

Fig. 5. (a) RTS observed for a p-type SB-FET with dopant segregation. $L_g = 300$ nm. (b) Normalized RTS amplitude as a function of V_g for 30 nm $< L_g < 1$ μm for p-type SB-FETs with dopant segregation. (Inset) Related trap occupancy probability. No difference is noticed for devices with $L_g \leq 300$ nm.

The difference in normalized noise amplitude between n-type SB-FETs with dopant segregation and p-type SB-FETs [the green dots in Fig. 4(b)] is similar to that of SB diodes. However, this difference is reduced for dopant-segregated p-type SB-FETs. It can be explained by the number of defects, leading to generation–recombination and trapping noise. Indeed, the section for the SB capacitance in the transistor configuration is the SOI thickness ($t_{\mathrm{SOI}} = 12$ nm) $\times W_g$, which is orders of magnitude lower than that for SB diodes.

Therefore, only few traps that were at the origin of the $1/f^2$ noise in the SB diode configuration may be active. Fluctuation of the current in the time domain confirms this hypothesis. At low V_d, RTS is always observed in segregated p-type devices, even for gate lengths of 1 μm. It is a two-level fluctuation of the current as shown in Fig. 5(a), usually considered as a consequence of a single-electron trapping/detrapping process at the gate oxide interface. Normalized RTS amplitude barely varies with V_g for all devices except for $L_g = 1$ μm. A more important point, which is very different from conventional FETs, is that the trap occupancy probability $\tau_{\mathrm{up}}/\tau_{\mathrm{up}} + \tau_{\mathrm{down}}$ does not vary with V_g, with τ_{up} and τ_{down} being the average times for the upper and lower levels. This points out that the defect type is inside the SB, which is in agreement with the generation–recombination noise observed for SB diodes.

V. Discussion

A. Models and Impact on the Charge Transport Mechanism

Models that we have proposed for SB diodes and FETs account for the exponential increase of normalized noise at low V_d, even for linear I_d–V_d curves. It evidences a contribution of SB to the noise even if the resistance is dominated by the silicon channel. As far as we know, other models for FETs do not include such V_d dependence.

For p-type devices with dopant segregation, an additional generation–recombination noise is observed. For SB diodes, noise features $1/f^2$, and for SB-FETs, a peculiar RTS is observed (trap occupancy probability independent of the gate voltage). Technological issues related to fluorine coming either from the p-type dopant segregation with BF_2 implantation or from Pt50 and Pt60 donor defects may be solved by consideration of these signatures.

From RTS amplitudes of p-type segregated SB-FETs and considering the fluctuation of the voltage across SB capacitor C ($\Delta I/(\partial I/\partial V_d) = q/C$) related to the trapping of a single electron, we estimate the SB thickness (in a parallel-plate configuration) to a few angstroms, which is a feasible value.

Considering an average SB capacitor thickness of 1 nm and $A = 3.8 \times 10^{-6}$ V^2 for n-type SB-FETs with segregation, (9) gives $N_t = 10^{13}$ cm^{-2}. A is reduced to 9.5×10^{-8} V^2 in a diode configuration due to the increase of the diode section.

Effective section is however difficult to evaluate due to our planar process.

B. Comparison With Other SB-FETs

As mentioned previously, $1/f$ noise in SB-FETs has been more studied for emerging devices than for Si or SOI-based SB-FETs. In [7], it has been shown that $1/f$ noise of PtSi SOI SB-FETs ($\phi = 0.93$ eV) is larger than that for Ni silicide SOI SB-FETs ($\phi = 0.64$ eV). The larger noise was attributed to injection of hot electrons for high ϕ. Noise amplitudes are difficult to compare with those of our device due to a larger device, and the spectra are shown in the saturation regime.

Noise in carbon nanotubes [32] and graphene transistors [33] seems to follow a similar behavior as our devices in the subthreshold region and was successfully explained by the charge noise model proposed for ballistic SB-FETs [25]. However, $N_{\rm ot}$ was not extracted because the fluctuation is considered to come from the SBs with a ballistic transport in the channel. V_d dependence of the noise has not been investigated so far.

VI. Conclusion

To conclude, we have studied the low-frequency noise in SOI-based SB junctions and SB-FETs which we consider as a test bed because of an excellent process control of the gate oxide interface and flexible engineering to control the SB height ϕ through dopant segregation. We have shown that, even for very small $\phi < 0.1$ eV, the contribution from the SB to the noise is not negligible even if the current is dominated by the channel resistance. In addition, there is an exponential decay of the normalized noise with V_d, which is an important point to consider for amplifier or sensor applications. Tuning ϕ by technological means such as dopant segregation tends to reduce the noise amplitude, although additional generation–recombination and trapping noise is noticed at small V_d for p-type devices. The proposed model could be considered for any diffusive SB-FET.

Appendix A

Derivation of (4)

We start from the Richardson equation [26] of electron transport through an SB

$$I = SR^*T^2 e^{\left(\frac{-q\phi}{kT}\right)}\left[e^{\left(\frac{qV_j}{kT}\right)} - 1\right] \tag{8}$$

where S is the diode section, R^* is the Richardson constant, T is the temperature, ϕ is the SB height, V_j is the voltage across the SB, and k is the Boltzmann constant. Supposing that ϕ barely varies with V_j (first-order approximation) and considering that noise originates from the voltage fluctuation across the SB as in the case of tunnel barriers [27], [34], we get

$$\frac{S_I}{(\partial I/\partial V_j)^2} = \frac{q^2 N_t}{C_{\rm SB}^2 S}\frac{1}{f} = \frac{A}{f} \tag{9}$$

where A (in square volts) is a parameter for noise amplitude comparison. It could be related either to a fluctuation of trapped

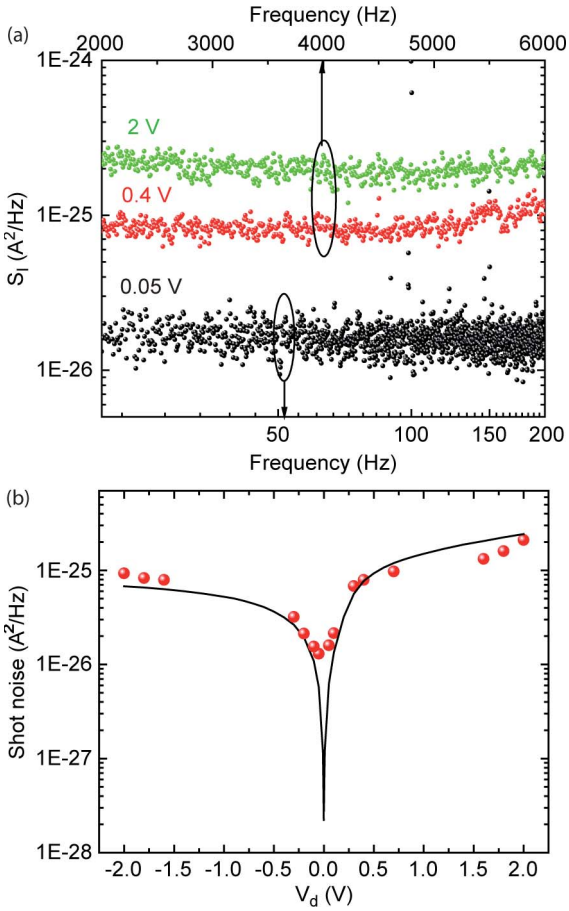

Fig. 6. (a) Power spectrum current noise around 100 Hz when $V_d = 0.05$ V and around 4 kHz when $V_d = 0.4$ and 2 V. White noise is observed. (b) Shot noise is plotted as a function of (red dots) V_d and compared with (black line) full shot noise.

charges at the SB interface (density N_t) (10) or to a fluctuation of dipoles in the SB [35] (11)

$$A = \frac{q^2 N_t}{C_{\rm SB}^2 S} \tag{10}$$

$$A = \frac{2kTtg\delta}{\pi C_{\rm SB} S} \tag{11}$$

where $C_{\rm SB}$ is the SB capacitance per surface unit and N_t is a density of defects that can trap charges. Due to the lack of knowledge for N_t and $C_{\rm SB}$, we consider A (in square volts) as a parameter for noise amplitude comparison

$$\frac{(\partial I/\partial V_j)}{I} = \frac{q}{kT}\left[\frac{1}{1 - e^{\left(\frac{-qV_j}{kT}\right)}}\right] \tag{12}$$

$$\frac{S_{\rm RSB}}{R_{\rm SB}^2} = \frac{S_I}{I^2} = A\left(\frac{q}{kT}\right)^2 \frac{1}{\left[1 - e^{\left(\frac{-qV_j}{kT}\right)}\right]^2}\frac{1}{f} \tag{13}$$

where $R_{\rm SB}$ is the SB resistance and $S_{\rm RSB}$ is the related power spectrum noise. When ϕ is small, the semiconductor channel serial resistance cannot be neglected

$$\frac{S_I}{I^2} = \frac{S_{\rm RSB} + S_{\rm RC}}{(R_C + R_{\rm SB})^2} = \eta^2\frac{S_{\rm RSB}}{R_{\rm SB}^2} + (1-\eta)^2\frac{S_{\rm RC}}{R_C^2} \tag{14}$$

where R_C is the channel resistance and S_{RC} is the related power spectrum noise. Using (13) for the first term and (1) for the second term leads to (4).

Shot Noise in n-Type SB Diodes

For n-type SB diodes, a white noise corresponding to full shot noise ($2qI$) is superimposed to the $1/f$ noise. At low bias (< 0.2 V), white noise can only be observed at very low frequency ($\sim$50 Hz) [Fig. 6(a)] and in the kilohertz range for higher bias (competition between cutoff frequency of a preamplifier and $1/f$ noise amplitude). Taking an average of S_I around 50 Hz and 4 kHz depending on the bias, S_I–V is plotted in Fig. 6(b). It shows a relatively good agreement with the full shot noise theoretical curve.

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