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Microwave performance of 100 nm-gate $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ high electron mobility transistors on plastic flexible substrate

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The transfer of 100 nm gate length high electron mobility transistors onto plastic flexible substrate is reported. The layers of transistors are grown epitaxially on indium phosphide bulk substrate. By means of adhesive bonding technique, the transfer of these transistors onto polyimide substrate has been achieved. High cut-off frequencies $f_T = 120$ GHz, $f_{max} = 280$ GHz are demonstrated. These microwave characteristics are comparable to those obtained on 100 nm gate high electron mobility transistors on rigid substrate, which makes the flexible substrate highly promising for large-area radio-frequency applications as well as high-speed processing ability in the near future. © 2011 American Institute of Physics. [doi:10.1063/1.3663533]

During the past decade, because of combined advantages of flexibility, portability, and reduction in assembly costs, flexible electronics have been widely used in various domains: solar cells, display applications, flexible antennas, blast sensors, smart textiles, and other systems.¹ So far, for these promising applications, a variety of technologies such as organic thin film transistors, amorphous silicon, and polycrystalline-silicon have already been reported.^{2–5} Nevertheless, because of many applications requiring more frequency bandwidth and, hence, the need to operate in higher frequency range (millimeter wave), the above technologies are limited because of their poor transport properties. Recently, high mobility III-V material on flexible substrate has been reported.⁶ In order to reach better electrical performance, the use of InAlAs/InGaAs high electron mobility transistor (HEMT) integrated into the polyimide substrate (Kapton) and embedded into thin-film micro-strip (TFMS) lines, is proposed in this letter. It is to be noted that only one paper dealing with the fabrication process of large 50 μm -gate InGaAs/InAlAs HEMT on flexible substrate (HEMT-FS)⁷ has been published. If the electrical static performance was reported, dynamic performance was missing, which is among the main objective of this letter.

Lattice-matched InAlAs-InGaAs epitaxial layers have been grown on an InP substrate using a solid source molecular beam epitaxy. The epitaxial structure is composed of three parts. From top to bottom, the first one corresponds to typical HEMT structure: an InGaAs cap layer (20 nm, $6 \times 10^{18} \text{ cm}^{-3}$), an InAlAs barrier (12 nm), a Silicon δ -doping ($5 \times 10^{12} \text{ cm}^{-2}$), an InAlAs spacer (5 nm), an InGaAs channel (15 nm), and an InAlAs buffer layer (200 nm). The second part corresponds to a passivation layer (InP, 20 nm) which prevents carrier depletion of the active layer induced by the Fermi level pinning at the surface.⁸ Indeed, during HEMT-FS fabrication, the epitaxial structure is upside down, as a result, InP passivation layer is exposed to the air at the end device technology fabrication. The last part of the

epitaxial structure is an etch-stop layer (InGaAs, 200 nm) which makes the transfer on flexible substrate easier. Figures 1(a)–1(d) describe the main four steps of HEMT-FS fabrication process. During the first main step, 100 nm-gate HEMTs are fabricated on rigid substrate (Fig. 1(a)). Ohmic contacts are realized using e-beam lithography and Ni/Ge/Au/Ni/Au evaporation with annealing at 295 °C during 20 s within a N_2H_2 ambient. Mesa isolation is achieved by wet etching using orthophosphoric acid based solution. This wet etching is stopped inside the InGaAs etch-stop layer. Then, the Ti/Au/Ti bonding pads are deposited. After gate electron lithography using bilayer resists, gate-recess process is carried out by wet chemical etching with a succinic acid based solution. Then, a Ti/Pt/Au/Ti gate is deposited by evaporation. Note that, at the end of these steps, devices are not isolated between them on the wafer because of the conductive InGaAs etch-stop layer. As a result, electrical characterization can not be performed at this time. During the second step, TFMS access lines are fabricated as illustrated in Fig. 1(b); Benzocyclobutene (BCB) polymer island is defined on the HEMT structures by a photolithography process. Then, a Ti/Au/Ti metallization is deposited to connect the two sides of the source bonding pads (TFMS ground plane). Next, during the third step, adhesive bonding process is performed using SU-8 photoresist as a bonding agent (Fig. 1(c)). SU-8 is spun onto the HEMT components and on the polyimide substrate (Kapton). Then, both are pressed together under vacuum environment and heated at 80 °C during 30 min. Owing to the ultraviolet transparency of polyimide film, SU-8 cross-linked is performed by UV exposure. Finally, during the last main step, the InP substrate is selectively removed using an hydrochloric acid based solution and the InGaAs etch-stop layer is selectively etched using a orthophosphoric acid based solution (Fig. 1(d)). This wet-etching process enables to accurately stop on the InP passivation layer. Fig. 1(e) features an optical image of our HEMT-FS, in which the mechanical bendability is clearly observed. In addition, for the sake of the benchmark of HEMT-FS structure, standard HEMTs on rigid substrate (HEMTs-RS) have been fabricated on another wafer. Note that HEMTs-RS do have the

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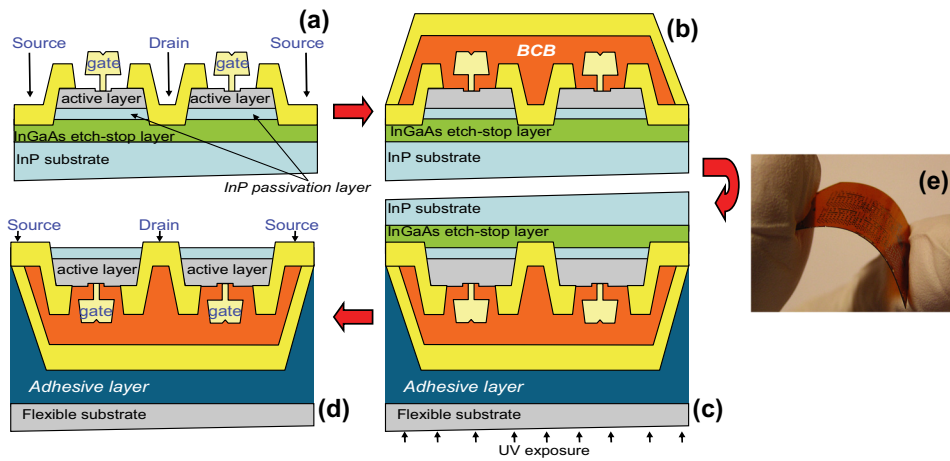


FIG. 1. (Color online) Process flow: (a) InAlAs/InGaAs HEMT fabrication. (b) TFMS access fabrication. (c) Transfer on flexible substrate. (d) Final schematic geometry of our HEMT on flexible substrate. (e) Optical image of HEMT on flexible substrate.

same epitaxial active layer as HEMT-FS and have identical device geometry with physical gate length of 100 nm and gate width of $2 \times 50 \mu\text{m}$.

Hall measurements have been performed at room temperature on both HEMT-FS and HEMT-RS active layers. HEMT-FS presents a hall mobility and a hall density of $7400 \text{ cm}^2/\text{V}^{-1} \text{ s}^{-1}$ and $5.4 \times 10^{12} \text{ cm}^{-2}$, respectively, while HEMT-RS features a hall mobility and a hall density of $6900 \text{ cm}^2/\text{V}^{-1} \text{ s}^{-1}$ and $6.8 \times 10^{12} \text{ cm}^{-2}$, respectively. It is to be noted that hall density of HEMT-FS is lower than HEMT-RS one. Since both structures have the same active layer, the difference can be attributed to a partial depletion of the HEMT-FS channel layer by the surface potential of the InP passivation layer. On wafer static and dynamic measurements have been carried out at room temperature on both HEMT-RS and HEMT-FS. Typical output characteristics are plotted Fig. 2. For HEMT-FS, the value of maximum drain current I_{dMAX} reaches 210 mA/mm for a gate-to-source voltage $V_{GS} = 0.2 \text{ V}$. But for HEMT-RS, this value exceeds 300 mA/mm for $V_{GS} = 0.1 \text{ V}$. According to transfer characteristics (not shown), maximum extrinsic transconductance g_m of HEMT-FS is 800 mS/mm for a drain-to-source voltage $V_{DS} = 1.2 \text{ V}$. By contrast, this value is about 1000 mS/mm at $V_{DS} = 0.8 \text{ V}$ on rigid substrate. Moreover, the threshold voltage V_{TH} is estimated to be -0.25 V on HEMT-FS, while it reaches -0.5 V on HEMT-RS. A qualitative explanation for these differences (positive shift of V_{TH} , decrease of g_m and I_{dMAX} for HEMT-FS) lies in the fact that the HEMT-FS is

upside down after transfer, as shown in Fig. 1(c). Indeed, the InP passivation layer, whose surface is exposed to air, does not fully prevent the depletion of the channel due to the Fermi level pinning at the surface. As a result, the depletion of the channel layer leads to the presence of a kink effect phenomenon when impact ionization occurs. Kink effect can be clearly observed when looking at the output characteristics of HEMT-FS (Fig. 2) at V_{DS} around 0.7 V. This phenomenon in HEMTs has been widely reported in the literature.^{9,10} The main reason of the kink effect is the combination of the holes accumulation generated by impact ionization on the high-field drain end of the gate area in the channel layer and the low electron channel concentration in the source side in recessed area.^{11,12} According to this mechanism, holes accumulation in the source side area lead to an opening of the channel which increases the drain current.

The S-parameters of the 100-nm-gate HEMT-FS and 100-nm-gate HEMT-RS have been measured on wafer using a vector network analyzer. Fig. 3 shows the Mason's unilateral power gain U_g and the extrinsic current gain $|H_{21}|^2$ (inset), respectively, as a function of frequency and for each device. Note that parasitic capacitances related to the probing pads have been carefully de-embedded from the measured S-parameters. Based on the usual 6 dB/octave extrapolation, the HEMT-FS exhibits a f_T of 120 GHz and a f_{MAX} of 280 GHz. For HEMT-RS, cut-off frequencies f_T and f_{MAX} are 203 GHz and 215 GHz, respectively. The lower f_T

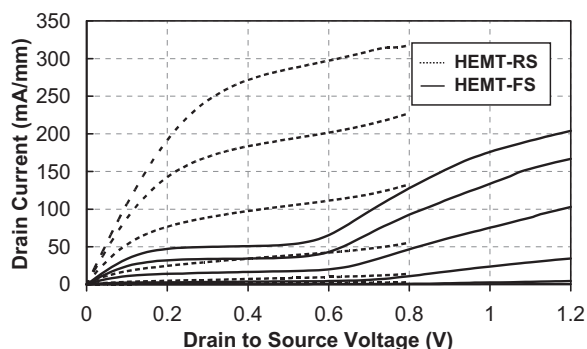


FIG. 2. Output characteristics of the HEMT-RS and HEMT-FS. The top gate bias for HEMT-FS is 0.2 V and for HEMT-RS is 0.1 V, both gate steps are -0.1 V .

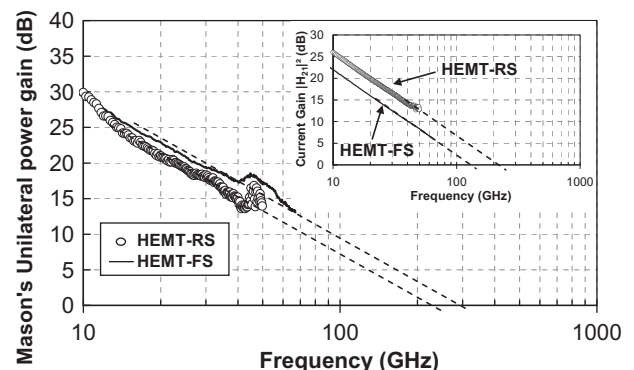


FIG. 3. The Mason's unilateral power gain U_g as a function of frequency measured at $V_{DS} = 0.8 \text{ V}$ (HEMT-RS), $V_{DS} = 1.2 \text{ V}$ (HEMT-FS). On the inset, current gain $|H_{21}|^2$ as a function of frequency measured with the same voltages.

obtained for HEMT-FS can be attributed to the decrease of gm and the use of BCB polymer which increases parasitic capacitances. The higher f_{MAX} for HEMT-FS can be related to the surface potential on InP layer; indeed, this surface potential counteracts the effect of carrier injection in the InAlAs buffer layer¹³ and increases the confinement of electrons in the InGaAs channel layer, which leads to lower output conductance gd . In turn, despite of differences of the cut-off frequencies mainly due to the kink effect, the RF performances obtained for both devices are similar and are not that much affected by adhesive bonding process on flexible substrate.

In summary, this letter introduces a feasible method for transferring conventional HEMTs onto the flexible substrate. Using this process, 100 nm-gate In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As HEMTs have been transferred onto polyimide film and electrically characterized in static and dynamic regime. Despite the presence of kink effect on these devices, which seems to be related to a partial channel depletion, high cut-off frequencies ($f_T = 120$ GHz and $f_{MAX} = 280$ GHz) have been achieved. These performances are in line with those obtained on 100 nm-gate HEMT on rigid substrate. These good characteristics open up the possibility to integrate high-frequency communication systems and other high-speed applications into the flexible devices. In our future work, an optimization of the technological fabrication process and/or epitaxial layer for lowering the Fermi level surface pinning effect of

HEMT-FS is scheduled, in order to suppress the kink effect and, thus, enhance the device electrical performance.

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