

A CMOS Low Loss / High Linearity Passive Mixer for 2.45 GHz Low Power Applications

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Abstract — A fully integrated passive mixer suitable for 2.45 GHz low consumption and low cost applications is proposed and demonstrated in a 90 nm CMOS technology. An original operating principle is adopted which is based on the use of a local oscillator square signal exhibiting a duty cycle less than 1/4. By using such a LO driving, the mixer operates as a sampler and can theoretically achieve a voltage conversion gain of 0 dB. This mixer has been integrated in a complete monolithic receiver. According to simulations, measurements demonstrate improvements of 5 dB on gain and 3 dB on noise figure without any linearity degradation and any additional cost, when compared to a common LO driving of 1/2 duty cycle.

Index Terms — Low-IF receiver, Zigbee receiver, passive mixer, switched mixer, sampling mixer.

I. INTRODUCTION

The growing demand for sensor networks motivates developments of very low cost and very low power radio frequency CMOS integrated receivers [1]. Some standards like ZigBee must maximize battery lifetime, which means a low current consumption under low voltage supply. Nevertheless, this operating mode must be achieved without any tradeoff on RF performances such as sensitivity and linearity. In this context, development of original solutions, able to fulfill these trends, appears as a major concern.

The mixer is a key part of the RF front-end receiver. Under low power issue, passive mixers are more attractive than active ones [2]. Furthermore, as linearity is often required whereas the mixer is low voltage biased, many current passive mixers have been developed [3-4]. But all of these mixers cannot fit very low power applications because of the current consumption and the need of gain stages for compensating high conversion losses.

In this paper, a voltage passive mixer is presented. It performs a direct transposition from the RF frequency band to the low-IF baseband. A reduced duty-cycle LO square signal makes it operate like a sampler. This principle demonstrates that very low frequency conversion losses and enhanced linearity can be reached.

The constraints that must be fulfilled by a very low cost and very low power receiver are summarized in section II. Then, this section deals with the proposed mixer optimization and the circuit implementation. In section III, experimental results are presented for a complete RF receiver. The

comparison with receiver performances reached when the mixer is driven by a standard LO square voltage clearly demonstrates the benefits of a mixer sampling operation.

II. CIRCUIT DESIGN

A. Constraints on a low cost / low power RF receiver

Many communication standards co-exist around 2.4 GHz, such as WLAN and Bluetooth. These signals act as interferers for a ZigBee receiver which linearity then constitutes an important issue. On the other hand, zero or low-IF receivers appear of main interest for low cost and low power applications. In these conditions, an image rejection is needed which leads to implement two channels, i.e. an in phase channel (I) and a quadrature channel (Q) (Fig.1). Moreover, since the number of blocks must be lowered, and the implementation of couplers must be avoided as well, both I and Q signals are generated at the mixer level, from two differential RF inputs and two differential LO inputs in quadrature. In this context, the passive mixer of each channel is simply composed by four small switches characterized by their “on” resistance (r_{on}). Since the mixer is expected to operate as a voltage conveyor, special care must be provided on the loading conditions. Hence, while high impedance loads are quite easy to reach at the low frequency IF mixer terminals, it is far more problematic for RF source to act as very low impedance equivalent Thévenin generator. The main reason is the low biasing current of all RF blocks which is set for low consumption operation.

The first issue with this kind of implementation is the interaction between I and Q channels when a LO signal duty cycle of 1/2 is used, and when the source impedance value at the RF terminal is not small enough (R_{IN} on Fig.1). For example, as illustrated on Fig.3a, the Q channel switches from “off” to “on” state at the middle of the “on” state of the I channel, which produces the Q channel output capacitance (C_{OUT}) discharge into R_{IN} . This “on” state overlapping of both I and Q mixers lowers and distorts V_{RF} voltage, leading to lowered V_{IFx} outputs voltages. Electrical simulations performed for a typical configuration (Fig.2) with $R_{IN} = 1 \text{ k}$, $r_{on} = 200$, $R_1 = 0$ and $R_{OUT} = 100 \text{ k}$ show 4 dB excess losses because this overlapping issue. Moreover, with a usual 1/2 LO duty-cycle (Fig. 4a), and considering RF and LO

signals exhibit the same frequency and are in phase, the mixer displays 4 dB losses, according to (1).

$$V_{IF} = V_{RF} \cdot \frac{2}{T} \cdot \int_0^{T/2} \sin\left(\frac{2\pi}{T} \cdot t\right) dt = \frac{2}{\pi} \cdot V_{RF} \quad (1)$$

As a summary, the conversion gain of a commonly LO driven passive mixer (1/2 duty cycle LO) is near -8 dB, which will affect the overall receiver performances.

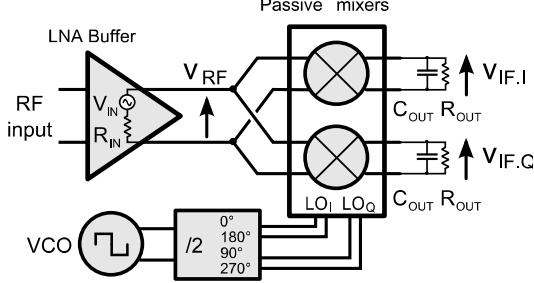


Fig. 1. Receiver configuration.

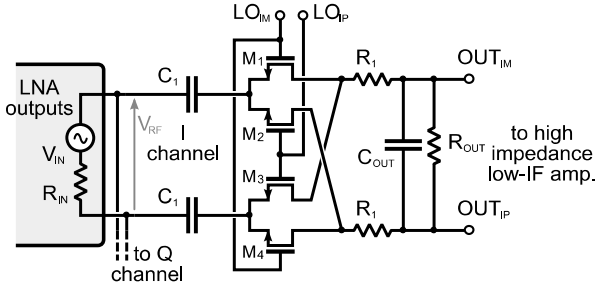


Fig. 2. mixer schematic of the I channel (the same as Q channel)

B. Passive mixer operating mode optimization

From previous statements, the passive mixer gain can be increased by limiting the “on” state overlapping of switches of I and Q channels. A first solution consists to increase the resistance of each channel by increasing the r_{ON} of the switches or by adding a series resistor R_1 (Fig.2). Nevertheless, the voltage gain improvement stays limited because the ratio of resistors R_{IN} , R_1 and R_{OUT} , and the mixer thermal noise is increased proportionately of R_1 . Adding $R_1 = 1\text{ k}$ to the previous example leads to a simulated improvement of only 2.5 dB.

A second solution appears to be more efficient and translates to a nearly lossless mixer [6]. It consists of reducing the LO duty cycle down to values less than 1/4 without any change on LO voltage amplitude. Applying this LO driving technique removes the overlapping of the “on” state of both channels (as depicted on Fig. 3b, the second channel cannot commute while the first one is in the “on” state), and reduces the averaging window of the RF voltage. Then, this small duty cycle LO driving drastically reduces losses. Taking the limit as the LO duty cycle is near zero, the mixer operates like a sampling mixer which IF amplitude can theoretically reach the RF one. In practice, this improvement is limited by rise and fall times of the LO driving, and this principle requires a capacitance C_{OUT} for the mixer output

load, to hold voltages when all switches are “off”. This capacitance C_{OUT} can be supplied by the post-mixer filter or, in many cases, by parasitic capacitors of the switches.

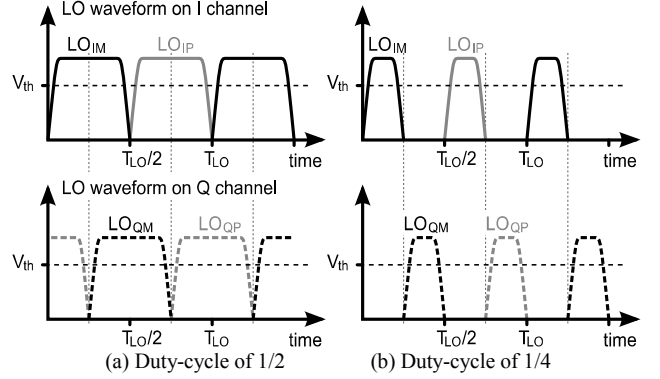


Fig. 3. LO waveforms versus duty-cycles

Fig. 4b illustrates the principle of operation for a LO duty cycle of 1/4. At low-IF ($T_{LO} \approx T_{RF}$) and considering a phase shift of $\pi/4$ between LO and RF signals, a gain of -1.9 dB is analytically obtained from (2). The second term in (2) models the average IF voltage value held by C_{OUT} when all switches are “off”.

$$V_{IF} = V_{RF} \cdot \frac{2}{T} \cdot \left[\int_0^{T/4} \sin\left(\frac{2\pi}{T} \cdot t + \frac{\pi}{4}\right) dt + \int_{T/4}^{T/2} \sin\left(\frac{2\pi}{T} \cdot \frac{T}{4} + \frac{\pi}{4}\right) dt \right]$$

$$\Rightarrow V_{IF} = V_{RF} \cdot \left(\frac{\sqrt{2}}{\pi} + \frac{\sqrt{2}}{4} \right) = 0.804 \cdot V_{RF} \quad (2)$$

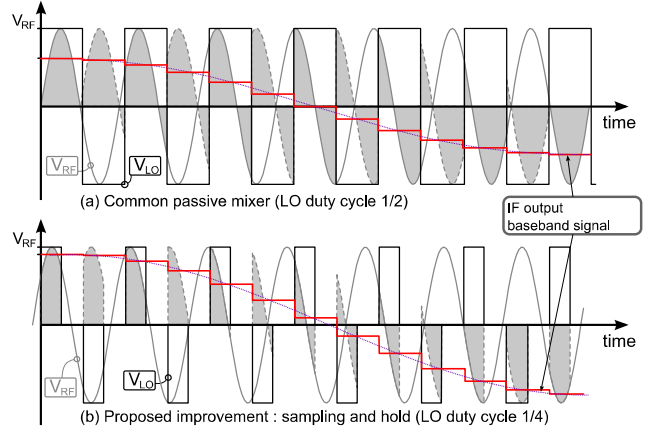


Fig. 4. Classic (a) and proposed (b) passive mixers waveforms

Fig.5 summarizes the simulated passive mixer gain versus LO duty-cycle, for $R_1 = 0$ and 1 k . The curves confirm the previous theoretical analysis and that a gain better than -2 dB is achievable when the mixer is driven with a 1/4 duty cycle LO. Moreover, the LO duty-cycle reduction maintains a high linearity level, which cannot be reached when rise and fall times are increased or when a sinusoidal LO is used [7].

C. Circuit description

The proposed mixer principle was implemented on a low power, low cost and low-IF receiver, including all functions from the input balun to the output first order channel filter.

Simulated gain of all blocks before the mixer is 17 dB, and the post-mixer channel filter exhibits a gain of 20 dB with an input noise of 12.3 nV/ $\sqrt{\text{Hz}}$.

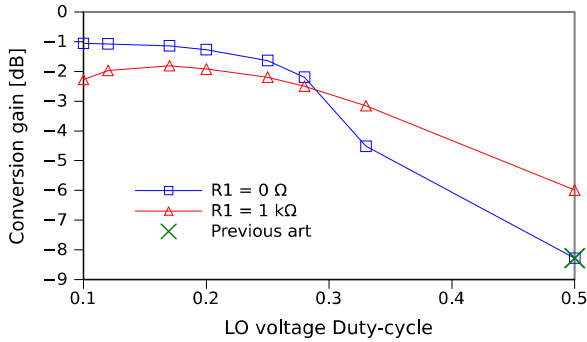


Fig. 5. simulated passive mixer gain versus LO duty-cycle

For comparison, two solutions were implemented. The first one uses a common 1/2 duty-cycle square LO voltage driving with $R_1 = 1 \text{ k}$ (label: Ref.), while the second one uses a LO duty-cycle of 1/4, realized by means of NOR gates, with $R_1 = 0$ (label: New mixer). Because of the rise/fall times and mixer threshold voltage, the actual LO duty cycle is about 1/5. The voltage amplitude is set around 1.2 V in both cases. Using a LO duty-cycle of 1/5 translates into a simulated conversion gain of -1.2 dB for the mixer. The NOR gates add a very small excess current consumption of 300 μA .

III. EXPERIMENTAL RESULTS

The overall receiver was fabricated using a 90 nm CMOS technology with seven metal layers [8]. The circuit operates under 1.35 V supply, for a total current consumption of 4.2 mA. Fig.6 gives the microphotograph of the fabricated receiver. Dimensions are $0.2 \times 0.4 \text{ mm}^2$.

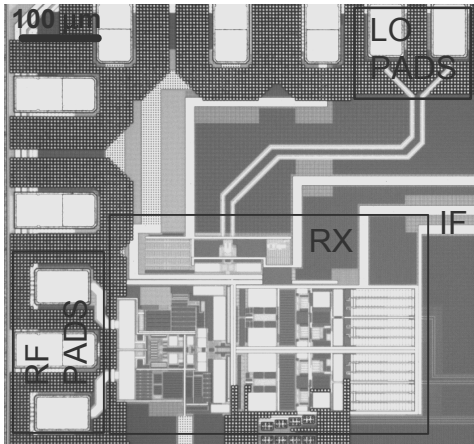


Fig. 6. microphotograph of the receiver

The Table I summarizes measurement results at 2.45 GHz for both receivers. As expected from simulations, reducing the LO duty-cycle down to 1/5 translates into important improvements on gain (5 dB) and on linearity. The noise figure of the receiver is then 3 dB better, which confirms that

in a low power CMOS receiver the mixer gain greatly impacts the overall sensitivity.

TABLE I
RX MEASURED PERFORMANCES (BALUN-LNA-MIXER-FILTER)

Receiver	Ref.	New mixer	Units
Gain	28.05	33.1	dB
Noise figure	11.1	8.1	dB
IIP3	-11	-9	dBm
OIP3	+6	+13	dBm
IP1dB	-21	-19	dB
DC power	5.4	5.7	mW

IV. CONCLUSION

This paper deals with a low power passive mixer implemented on a 90 nm CMOS technology. It demonstrates the huge interest of driving the mixer with a reduced duty-cycle square LO. A simple circuit is proposed for conditioning such a LO, which is based on NOR gates. Setting a LO duty-cycle lower than 1/4 leads to a passive mixer gain value near -1 dB, and enhances the mixer linearity as well. A sensitivity improvement of 3 dB is then reached for the overall receiver with almost no additional power requirement.

This principle has been successfully applied for a 2.45 GHz low power ZigBee receiver. Obviously, it remains full of interest and suitable for other standards and other frequency bands, as long as the technology is compliant with the required switching time for mixer control.

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