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# Chip on board 3-10GHz IR-UWB Transmitter with optimized die to antenna wire bond transition

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**Abstract**— In this paper, a low power and low cost Ultra WideBand Impulse Radio (IR-UWB) transmitter is presented. The transmitter includes a pulse generator integrated in a 0.13 $\mu\text{m}$  standard CMOS technology and an antenna printed on the chip carrier. The board is manufactured with Roger 4003 laminate substrate and has a total area of 50mm x 18mm. The transmitter provides 1.4V peak to peak FCC compliant pulses at antenna input for data rates up to 36Mb/s in an on-off keying (OOK) modulation scheme. The transmitter's power consumption is 12mW at 1.2GHz Pulse Repetition Frequency and the energy consumption is 10pJ per pulse. A 365mV peak voltage emitted pulse is measured in an anechoic room at 0.8m range with a receiver including a horn antenna (8.3 dBi), a LNA (32 dB), and a 12GHz real time oscilloscope.

**Index Terms**—antenna, CMOS impulse generator, circuit on board (CoB), transmitter, ultra wideband (UWB), wire bond interconnection.

## I. INTRODUCTION

The US Federal Communications Commission (FCC) authorizes transmission in the wide frequency bandwidth from 3.1 to 10.6 GHz since the signal bandwidth exceeds 500MHz, its mean Power Spectral Density (PSD) is lower than -41.3dBm/MHz and the peak PSD is lower than 0dBm/50MHz at the frequency where the power is maximum. Thus it is possible to transmit data by using short duration pulses and no carrier. Usually, this method of transmitting information is named Impulse Radio Ultra WideBand (IR-UWB) and enables the front end to be implemented by very simple architectures. Indeed the typical architecture of a non coherent energy detection receiver does not require a mixer and fully digital transmitters operating without any inductors have been reported. In addition the front-end only needs to be powered-on during the short pulse duration time. As a consequence the power consumption tends to be extremely low at low data rates. Thanks to its low cost and low power capacities, IR-UWB can address applications such as Radio Frequency Identification (RFID) [1], Wireless Body Area Network (WBAN) [2] or Sensor NetWork (SNW). In addition because of its very large bandwidth, IR-UWB can be used in high resolution sensing applications [3]. So, to be suitable for these applications, power consumption and physical implementation of IR-UWB systems have to be carefully

taken into consideration.

An efficient way to drastically reduce the power consumption is to transmit pulses with very short duration and to switch off the transmitter between each emitted pulse. The shortest pulses are obtained by using the full 3.1-10.6 GHz bandwidth. However, because of the limited performance of low cost CMOS technologies, most of published transmitters use only the lower part of the FCC bandwidth which is limited from 3 to 5 GHz. In [4], we demonstrated a CMOS pulse generator die compliant with the full 3.1-10.6 GHz FCC bandwidth having an energy consumption lower than 10pJ/pulse even with the emission of pulses with a peak to peak voltage greater than 1V. With such low energy consumption per pulse, very low power consumption levels can be reached for low data rate without reducing the communication range. In addition short pulse duration enables high pulse repetition frequency to achieve high data rate and low power communications simultaneously.

Other important points which need to be considered for mobile technologies systems are volume, shape factor and cost of the final product, including the antenna. A low cost implementation can be achieved by using a single chip made in a standard CMOS technology connected to an antenna with a low cost package. Nevertheless stringent requirements must be fulfilled in order to guarantee signal integrity with such low cost packages when very large bandwidth pulses are used. Ultra compact transmitters can be manufactured by integrating both the front end and the antenna into a single CMOS die [5]. The use of an on chip antenna avoids problems of signal integrity due to the interconnection between pulse generator die and a remote antenna. However, this technique reduces the antenna efficiency and consequently the communication range. Nevertheless, high efficiency antennas can be obtained by integrating them in Low Temperature Co-fired Ceramic (LTCC) packages using System on Package (SoP) approaches [6]. These packages can also be used to implement pulse shaping networks such as band pass filter [7]. In this way compact transceiver can be implemented using multi layer packages or multi layer Print Circuit Boards (PCB) but at a higher cost. A Chip on Board approach (CoB) can also be used with a planar antenna or a filter [8][9] on the board. For this type of structure, low cost PCB carriers can be used at the expense of a larger surface for the final product.

This paper presents a simple and compact UWB transmitter for low cost and low power applications. The transmitter includes a CMOS pulse generator die and a UWB antenna in a miniature CoB. By using the full 3.1-10.6 GHz FCC bandwidth, very low energy per pulse consumption is reached thanks to short pulse duration. The transmitter is made with low cost technologies: a single die fabricated in a standard CMOS process and a CoB package using conventional wire bonds and two metal layer interconnects. The transmitter provides 1.4V peak to peak FCC compliant pulses at antenna input for data rates up to 36Mb/s in an OOK modulation scheme. The transmitter power consumption is 12mW at 1.2GHz Pulse Repetition Frequency and the energy consumption is 10pJ per pulse. Emitted pulse measurements show 700mV peak to peak voltage pulse measured at 0.8m range with a 40.3dB gain receiver.

This paper is organized as follows. Section II describes the CMOS pulse generator die implemented in a 0.13 $\mu$ m standard CMOS technology. In section III the design of a compact planar UWB antenna is presented. Section IV describes the CoB assembly and presents the design of the wideband wire bond transition between the antenna and the output of the pulse generator. The transition is optimized to achieve the 3-10 GHz bandwidth. The measured results of the transmitter are presented in section V.

## II. PULSE GENERATOR

This section presents the transmitter die. The transmitter converts the incoming numeric data into a 3-10GHz IR-UWB pulse sequence with an OOK modulation scheme particularly well suited for low cost and low power consumption applications [4].

### A. Pulse Generator Sizing

The transmitter uses a CMOS integrated pulse generator [4] designed to achieve high magnitude pulses on 50 $\Omega$  load (coming from antenna impedance). As shown in Fig. 1, the generator is based on a filter impulse response technique which consists in applying a very short baseband pulse at the filter input in order to generate its Dirac response [10]. We consider that, instead of a Dirac, the filter is excited by a rectangular function  $\pi_\tau(t)$  which is formed by the product of a Heaviside step function ( $u(t)$ ) with its delayed and inverted replica ( $\bar{u}(t - \tau)$ ). The output ( $g(t)$ ) and its Fourier transform are given by :

$$g(t) = \frac{A}{\sqrt{l}} \pi_\tau(t) * h_e(t) \quad (1)$$

$$G(f) = \frac{A\tau \text{sinc}(\pi\tau f) \cdot H_e(f)}{\sqrt{l}}, \quad (2)$$

where  $A$  is the magnitude of the signal at the filter input,  $\tau$  the width of the rectangular function,  $l$  the power loss of the filter and  $H_e(f)$  the normalized transfer function of the filter. As the spectrum shape of the pulse ( $G(f)$ ) is mainly due to  $\tau$  and  $H_e(f)$ , these parameters must be chosen to comply to a particular standard mask.

This technique is well suited to the FCC standard since the minimum order of the filter needed is low ( $N=3$ ) due to the large width of the FCC frequency mask and enables the full integration of the filter with limited loss ( $l$ ). 3<sup>rd</sup> order Bessel filter (which has normalized low pass filter elements respectively equal to  $g_1=1.225$ ,  $g_2=0.5528$  and  $g_3=0.1922$ ) and 75ps width baseband pulse are used in this design to comply with the FCC mask.

Having  $H_e(f)$  and  $\tau$  it is possible to compute the Power Spectral Density ( $PSD_s(f)$ ) of a random signal ( $s(t)$ ) to evaluate the magnitude of the baseband pulse ( $A$ ) needed to fit the spectrum requirement :

$$PSD_s(f) = \frac{|G(f)|^2}{T_s} \left( \sigma_a^2 + \frac{\mu_a^2}{T_s} \sum_{i=-\infty}^{\infty} \delta\left(f - \frac{i}{T_s}\right) \right) \quad (3)$$

where  $\mu_a$  and  $\sigma_a^2$  are respectively the mean and the variance of the sequence data  $\{a_k\}$  and  $T_s$  the symbol time.

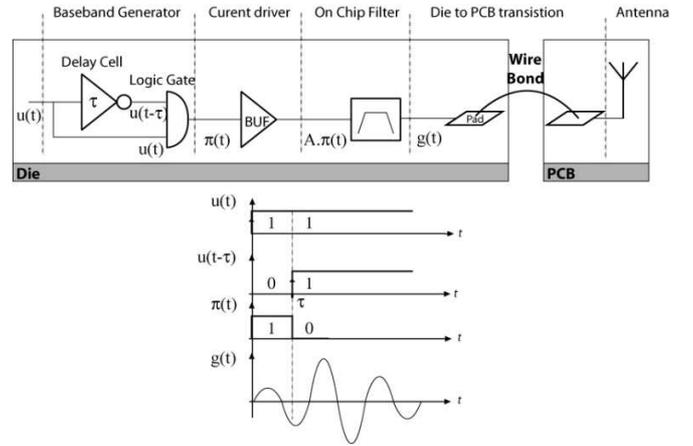


Fig. 1. Transmitter principle

To ensure low cost and low power architecture we use an OOK modulation scheme. Assuming data rates up to 36Mbs<sup>-1</sup> sufficient for most of the low cost applications we get a value of  $A=2.56V$  if 3dB power loss is considered.

### B. Pulse Generator Design

The pulse generator is designed using a standard 0.13 $\mu$ m CMOS technology to meet cost requirement. The use of such a technology implies constraints on design because passive components have low performances and standard CMOS digital cells based on logic inverter have a minimum propagation delay higher than several hundred picoseconds.

The design of the integrated filter is dominated by the choice of the filter structure, which needs components that perform well in the targeted technology. Indeed, the performances of the passive components and especially the inductor quality factor ( $Q$ ) vary with the value ( $L$ ) and the frequency range. For the technology used,  $L$  must be in a range of 400pH <  $L$  < 1.5nH to ensure a constant value and a  $Q > 10$  in a 10GHz bandwidth. The large relative bandwidth of the FCC mask is a great advantage because the constraints on the dispersion of the inductor values needed are not high and several filters can be realized with such relative bandwidth value. In our case, the chosen Bessel filter is implemented

using a modified ladder topology which leads to the values given in Fig. 2. It is pointed out here that, if the filter structure will not lead to required values, a different  $H_e(f)$  should be chosen during the sizing step which would modify  $A$  and  $\tau$ .

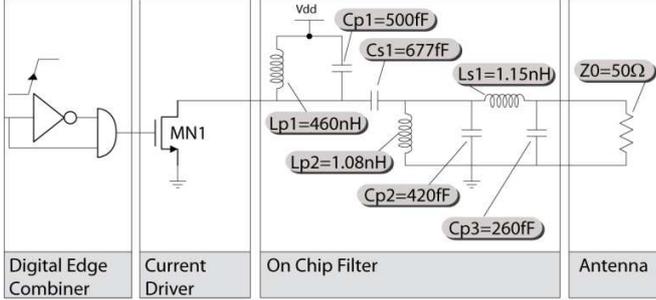


Fig. 2. Filter Topology

The baseband generator uses an edge combining technique (also called triangular pulse generation) [10], [11]. To achieve pulse width lower than few hundred picoseconds, modified MOS current mode gate logic (MCML) inverters are used [12]. In order to lower the propagation delay, this technique uses differential pair and reduced output swing as in emitter coupled logic (ECL) technology. Two consecutive edges produced by the MCML inverter are then combined using fast logic gate [10] to produce the baseband pulse. Due to the limited output voltage of the baseband stage ( $V_{dd}=1.2V$ ) and due to the low input impedance of the filter ( $50\Omega$ ), the baseband generator cannot drive the filter. A current driver is inserted between the baseband generator and the filter as presented in Fig. 1. The current driver consists of a transistor (MN1 in Fig. 2) operating in C class. MN1 is sized to supply a current value of  $I_0=A/50$  during the conduction time ( $\tau$ ). The large amount of current needed implies a large transistor width ( $W$ ). The output of the transistor must be matched to the filter. Using small signal hypothesis, the output impedance of MN1 ( $R_{ds}$  and  $C_{ds}$ ) can be approximated during the conduction time. The value of  $C_{ds}$  must be compensated by  $C_{p1}$  (if  $C_{ds} < C_{p1}$ ) to avoid pulse shape modification. Moreover  $R_{ds}$  should be equal to  $50\Omega$  to maximize power matching. Unfortunately,  $R_{ds}$  depends on  $W$  which is fixed to achieve  $I_0$ . It is not possible to realize power matching while supplying a given  $I_0$  and a trade-off must be made, resulting in lower power efficiency. In the presented design  $W=100\mu m$  which leads to  $R_{ds}=122\Omega$  and  $C_{ds}=240fF$ .

### C. Pulse Generator Results

The pulse generator has been made using a standard CMOS  $0.13\mu m$  technology from ST Microelectronics. The die photograph is shown in Fig. 3 and its area is  $0.54mm^2$ . The measurement of the generated pulse using on chip probing is given in Fig. 4. The maximum pulse magnitude is  $1.42V_{pp}$ . The measured spectrum of a  $36Mbs^{-1}$  OOK modulation demonstrates a good compliance with FCC spectrum. Fig. 4.c presents the output waveform when the input is driven by a  $1GHz$  “1 bit” sequence. The pulse generator can achieve data rates up to  $1.2Gbs^{-1}$ . In this case the measured DC power consumption of the pulse generator is  $12mW$  leading to a

measured energy per pulse consumption of  $10pJ$  including the DC power consumption. Table I summarizes the main performances of the pulse generator and presents a comparison with other published transmitters. The proposed transmitter die shows low energy per pulse consumption with high peak voltage and energy efficiency.

TABLE I  
TRANSMITTER PERFORMANCE COMPARISON

Ref	Technology ( $\mu m$ ) $V_{DD}$ (V)	BW (-10dB)	$V_{pp}$	Energy per pulse consump. <sup>a</sup>	Power Cons.	Silicon Area ( $mm^2$ )
[5]	CMOS 0.18 1.8V	6.5 to 9.5 GHz	30mV	12pJ	9mW @750MHz @PRR	0.045 (core)
[13]	CMOS 0.18 1.5V	3.75 to 4.25 GHz	0.18V @50Ω	18.2pJ	1.82mW @100MHz @PRR	0.39 (die)
[14]	CMOS 0.09 1V	3.78 to 4.33 GHz	0.65V @50Ω	47pJ	470μW @10Mbs <sup>-1</sup> @BPSK	0.08 (core)
[15]	CMOS 0.09	3.75 to 4.25 GHz	0.5V @50Ω	29.2pJ	146 μW @5MHz @PRR	1.3 (die)
This work	CMOS 0.13 1.2V	3.1 to 10.6 GHz	1.42V @50Ω	10pJ	12mW @1.2GHz @PRR	0.54 (die)

<sup>a</sup> Calculated from power consumption and data rate

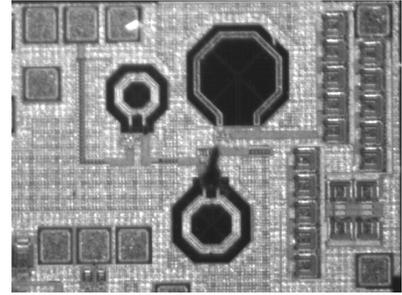
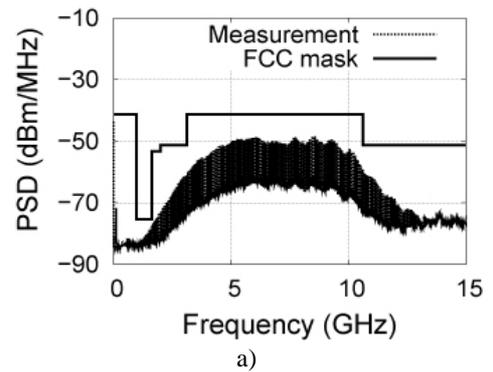


Fig. 3. Die photograph



a)

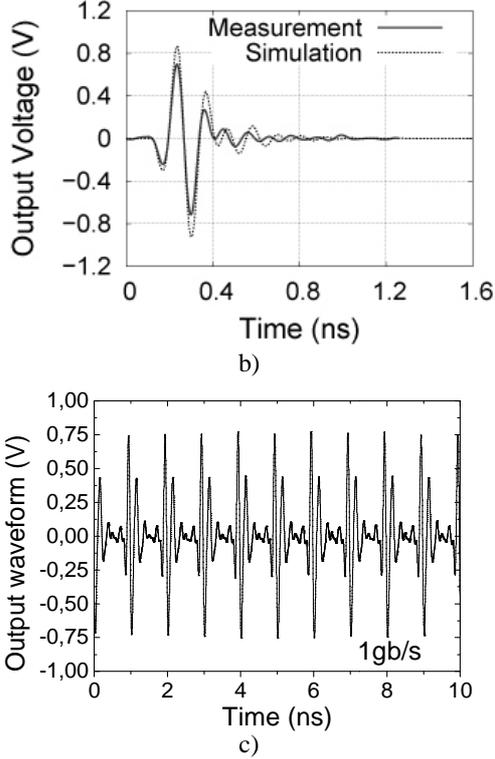


Fig. 4. Pulse generator probe measurement. (a) Frequency domain. (b) Time domain. (c) Output waveform for 1gb/s pulse repetition.

### III. ANTENNA

The antenna is printed on the top layer of the chip carrier. This top layer is made of Ro4003 material having a thickness of 200 $\mu$ m thickness. The generic layout of the antenna is shown in Fig. 5. The antenna is a rectangular patch composed of several rectangular steps. The antenna is fed by a 50 $\Omega$  grounded coplanar waveguide (GCPW) printed on the top substrate layer. Two rows of metallic plated holes are used to connect the upper side planes of the GCPW and the lower ground plane these two parts at the same electrical potential. In this way the parasitic modes of the transmission line are suppressed. The ground plane stops at the end of the GCPW leaving the patch antenna in free space and therefore maintaining its wideband characteristics.

#### A. Antenna design

The design of the transition between the line and the patch is crucial to obtaining UWB performances [16][17]. Therefore, a set of simulations were performed to properly tune the coupling between the rectangular patch and its feeding structure using various parameters. Notches were first cut in the two lateral planes at the end of the GCPW. Then another notch has been inserted in the ground plane in order to finalize the tuning. The proper dimensioning of these notches allows modifying the electromagnetic coupling between the line and the patch, and therefore obtaining the desired performances. The characteristics of the antenna can also be adjusted using the size of the ground plane. The final dimensions of steps and notches, corresponding to the selected antenna configuration, are given in Table 2.

#### B. Antenna measurement results

In order to validate the simulated performances of the antenna, a stand-alone antenna prototype (see Fig. 6.) has been made and measured. The comparison between simulated and measured return loss (RL) is presented in Fig. 7. The RL is greater than 6dB from 3 GHz to 10.6 GHz

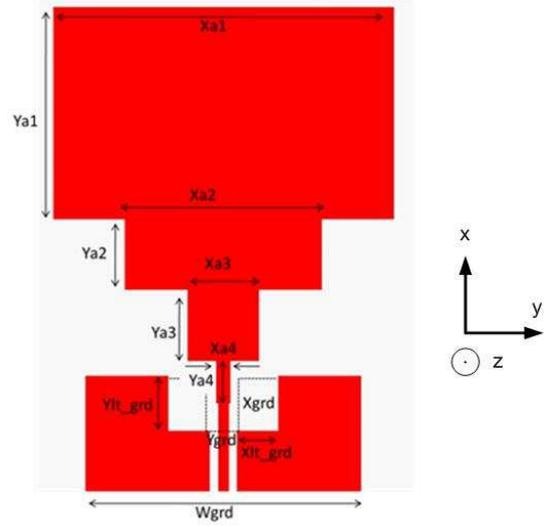


Fig. 5. Antenna geometrical parameters

TABLE 2  
FINAL ANTENNA PARAMETER VALUES

<b>Xa1</b>	12.35 mm
<b>Xa2</b>	7.15 mm
<b>Xa3</b>	2.6 mm
<b>Xa4</b>	1.52 mm
<b>Ya1</b>	7.8 mm
<b>Ya2</b>	2.6 mm
<b>Ya3</b>	2.6 mm
<b>Ya4</b>	0.56 mm
<b>Xlt_grd</b>	2 mm
<b>Ylt_grd</b>	1.5 mm
<b>Xgrd</b>	2 mm
<b>Ygrd</b>	0.8 mm
<b>Wgrd</b>	10 mm

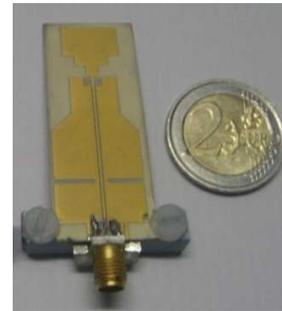


Fig. 6. Stand alone antenna prototype.

The radiation patterns at the lower and higher limits of the FCC band, respectively 3GHz and 10 GHz, are presented in Fig. 8. Radiation patterns similar to those of a monopole are obtained on the whole bandwidth.

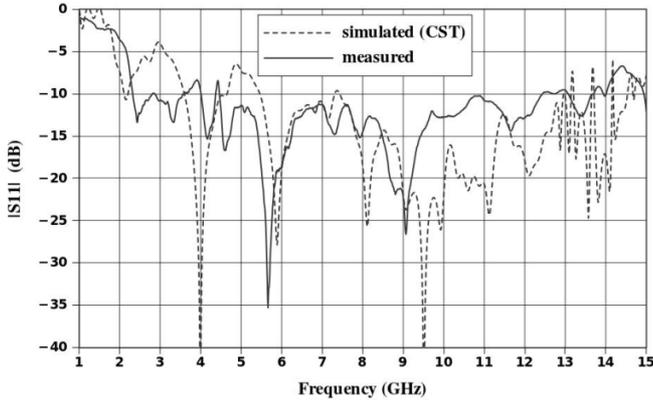


Fig. 7. Measured and simulated antenna return loss.

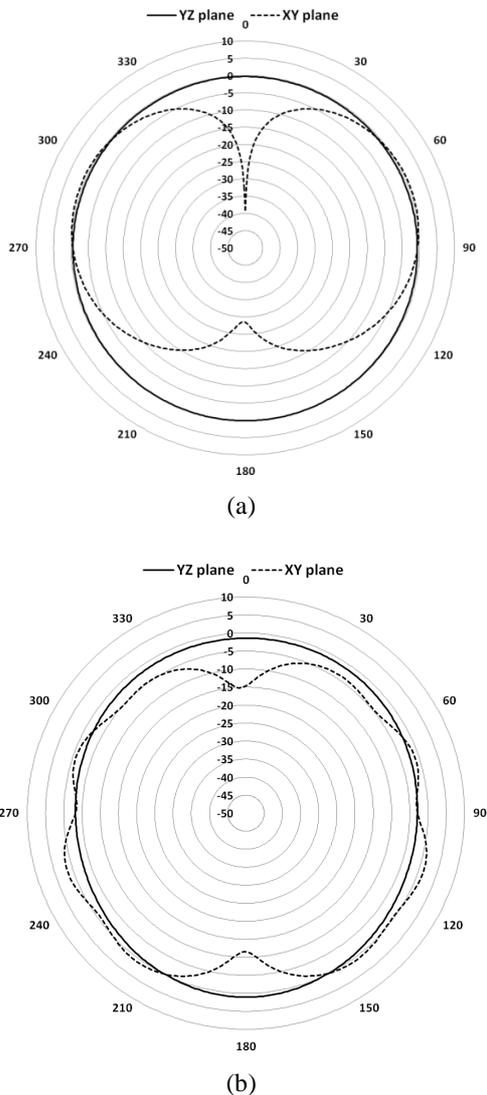


Fig. 8. Measured antenna radiation patterns in YZ plane and XY plane at 3 GHz (a) and 10 GHz (b).

#### IV. CHIP TO ANTENNA INTERCONNECTION

Large bandwidth systems require generally expensive packages. For low cost applications, wire bonds interconnections are frequently used. However such transitions

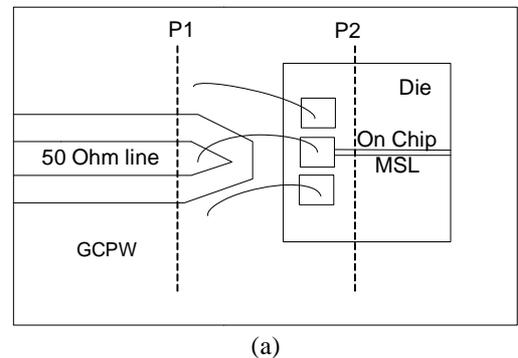
present a limited bandwidth due to the parasitic inductor introduced by the wire bonds length. In this section, a design methodology is presented in order to obtain a wire bond carrier to die transition with a return loss greater than 15dB in the entire 3-10 GHz UWB band.

##### A. Wire bond transition design and modelling

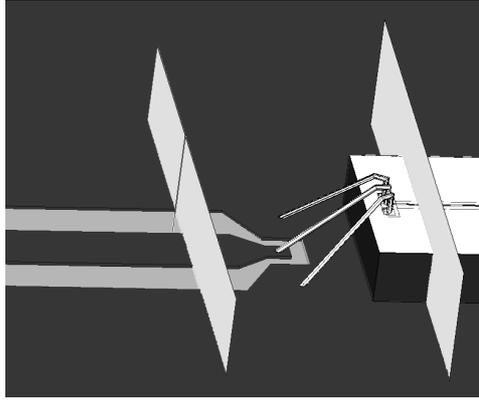
Schematic description of the wire bonds carrier to die transition is given in Fig. 9.a. The transition connects a 50Ω grounded coplanar line (GCPW) on the chip carrier to a microstrip line (MSL) on the chip. The chip carrier is made on the same top layer of Ro4003 material of 200μm thickness where the antenna has been printed. The major dimensions of the GCPW, which are its central strip width  $w$ , its gap  $g$  and its thickness  $t$  are respectively equal to (390/300/17) μm. The transition includes three 25μm diameter aluminium wire bonds. The CMOS silicon die height is 350μm. The design has been made to minimize the length of wire bonds while satisfying standard technological design rules for die and package, which leads to 0.8mm wire bond length.

To obtain an electrical model, the wire bond transition has been accurately simulated to provide the scattering parameters between the off die radio frequency (RF) reference plane (P1 in Fig. 9.a) and the on die RF reference plane (P2) referenced to the terminal impedance  $R_0$ . All the electromagnetic (EM) simulation results presented in this section have been obtained using a Finite Element Method EM simulator (HFSS). HFSS model of the wire bond transition between the GCPW and the die is shown in Fig. 9.b. During the simulation process, the RF reference planes are set as close as possible to the wire bond transition in order to minimize the maximum through phase shift and therefore to be closer to a lumped approximation of package transition.

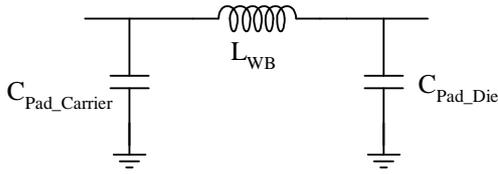
Under those conditions, the wire bond transition can be approximated by the equivalent  $\pi$  network shown in Fig. 9.c.  $L_{WB}$  is the extracted series inductance,  $C_{Pad\_Carrier}$  is the extracted shunt capacitance at the carrier RF reference plane P1 and  $C_{Pad\_Die}$  is the extracted shunt capacitance at the die RF reference plane P2. It should be pointed out that the wire bond transition model includes the effects of both the signal wire bond and the two wire bonds connecting the carrier ground to the die ground.



(a)



(b)

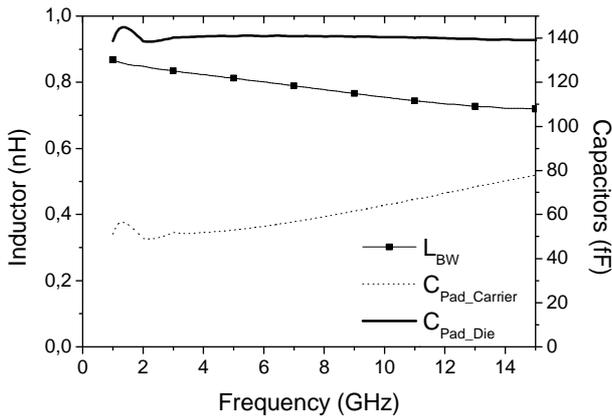


(c)

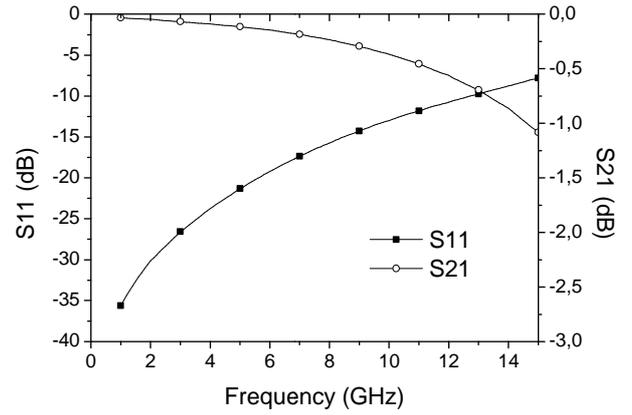
Fig. 9. Wire bond transition. (a) Schematic description. (b) HFSS model (c) Lumped equivalent  $\pi$  network.

Fig. 10.a plots the extracted values of the series inductance and shunt capacitances of the wire bond transition  $\pi$  electrical model. The extracted values of the series inductance and shunt capacitances are nearly constant up to 10GHz. The capacitance and inductance differences are respectively less than 20fF and 0.1nH from DC to 10GHz.

The wire bond transition scattering parameters obtained by EM simulation are given in Fig. 10.b. Transition has a return loss greater than 15dB from DC to 8.5GHz. This bandwidth is not sufficient in our case where the full 3.1-10.6 GHz UWB band is targeted.



(a)



(b)

Fig. 10. (a) Extracted series inductance and shunt capacitance of the  $\pi$  model of the wire bond transition. (b) Scattering parameters of the wire bond transition obtained by 3d EM simulation.

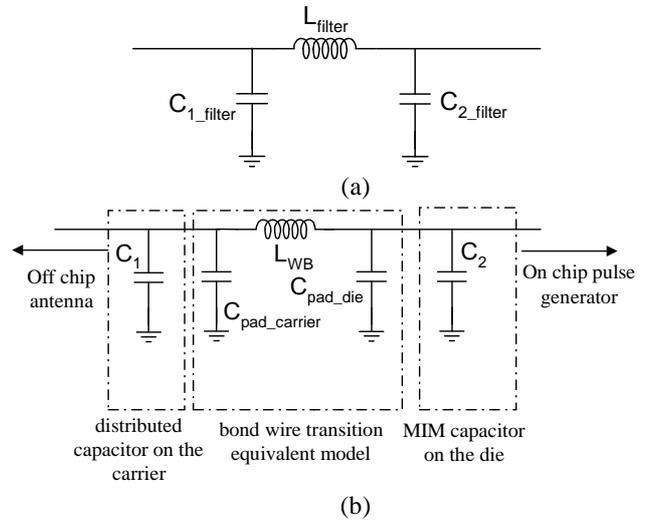
### B. Wire bond transition bandwidth enhancement.

Transition bandwidth can be extended by designing a third order low pass filter embedding parasitic elements of wire bond transition [18]. As shown in Fig. 11, a third order low pass filter (Fig. 11.a) can be synthesized with the transition by adding two capacitors  $C_1$  and  $C_2$  respectively on the carrier and on the die (Fig. 11.b). Inductance  $L_{filter}$  of the low pass filter is obtained by equaling it to the inductance  $L_{WB}$  coming from the  $\pi$  network modeling the wire bond transition.

In standard filter design, for ideal inductors and capacitors, the minimum return loss in the filter bandwidth  $f_{cutoff}$  is directly linked to the  $S_{21}$  ripple  $\epsilon_{dB}$  by

$$RL = -20 * \log\left(\sqrt{1 - 10^{-\frac{\epsilon_{dB}}{10}}}\right) \quad (4)$$

Embedding parasitic elements of the transition in a 0.14dB ripple low pass filter enables a transition to be obtained with a RL greater than 15dB in the whole targeted bandwidth.



(b)

Fig. 11. (a) Standard low pass filter. (b) Low pass filter embedding the wire bond transition.

In order to synthesize the normalized low pass filter we must satisfy:

$$L_{\text{filter}} = \frac{g_2 R_0}{2\pi f_{\text{cutoff}}} = L_{\text{pkg}} \quad (5)$$

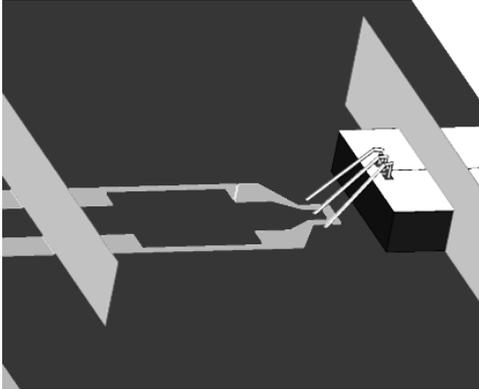
$$C_{1\_filter} = \frac{g_1}{2\pi R_0 f_{\text{cutoff}}} = C_1 + C_{\text{Pad\_Carrier}} \quad (6)$$

$$C_{2\_filter} = \frac{g_3}{2\pi R_0 f_{\text{cutoff}}} = C_{\text{Pad\_Die}} + C_2 \quad (7)$$

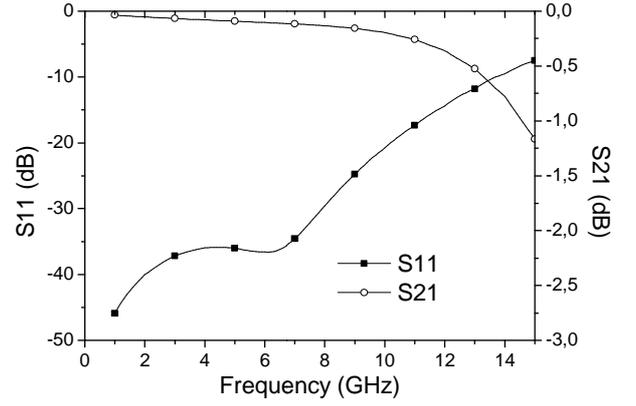
Where  $g_i$  are the low pass filter coefficients allowing a given filter type synthesis (order, ripple, and response) and  $R_0$  the filter characteristic impedance ( $50\Omega$  here).

In this design  $L_{\text{WB}}$  is set by the physical geometry of the wire bond transition. With a 0.14dB ripple Butterworth response ( $g_1=0.57$ ,  $g_2=1.13$ ,  $g_3=0.57$ ) [19] we obtain from (5) a bandwidth ( $f_{\text{cutoff}}$ ) of 12 GHz and from (6) and (7)  $C_{1\_filter}=C_{2\_filter}=151\text{fF}$ .  $C_{1\_filter}$  and  $C_{2\_filter}$  are obtained by adding respectively an 80fF distributed capacitor  $C_1$  to  $C_{\text{pad\_carrier}}$  on the carrier and an 11fF metal insulator metal (MIM) capacitor  $C_2$  to  $C_{\text{pad\_die}}$  in the die.

The modified wire bond transition HFSS model is shown in Fig. 12.a and Fig 12.b. shows the scattering parameters of the modified wire bond transition obtained by 3d EM simulation. Modified transition suits UWB applications since it has a return loss greater than 15dB from DC to 11.8 GHz.



(a)



(b)

Fig. 12. Modified wire bond transition. (a) HFSS model. (b) Simulated scattering parameters.

## V. UWB TRANSMITTER MEASUREMENTS AND RESULTS

### A. Transmitter board.

The transmitter board microphotograph is shown in Fig. 13. The board is fabricated using only two metal layers on a Roger 4003 substrate of  $200\mu\text{m}$  high. The transmitter includes the pulse generator CMOS die presented in section II and the printed monopole antenna presented in section III fed by a  $50\Omega$  ground coplanar line. The transmitter board is plugged into a mother board with an SFP connector which provides the DC biasing and the incoming data. The transmitter emits one pulse when a rising edge is driving the data input (data rates up to 1.2Gb/s can be achieved). The microphotograph of the carrier to die transition optimized as explained in section IV is shown in fig. 13.d. This transition provides a full band UWB access between the RF output of the pulse generator and the  $50\Omega$  ground coplanar line that feeds the antenna.

TABLE III: 3.1-10.6 GHz published transmitters comparison

	Chip technology	Transmitter area	Power consumption	Energy per pulse consumption	Data rate	Peak to peak measured voltage	Calculated emitted peak power at 1m
This Work	CMOS 0.13 $\mu$ m VDD=1.2V	50mmx18mm	12mW@1.2Gb/s	10 pJ <sup>1</sup>	up to 1.2 Gbs <sup>-1</sup>	700 mV @80cm @40,3dB/50 $\Omega$ receiver	-41.3 dBm <sup>2</sup>
[9]	CMOS 0.35 $\mu$ m VDD=3.3V	39mmx40mm	N/A	N/A	100Mbs <sup>-1</sup>	16 mV @ 1m @ 10dB/50 $\Omega$ receiver	-41.9 dBm <sup>2</sup>
[3]	SiGe 0.8 $\mu$ m	60mmx90mm	38mW@200Mb/s	190pJ <sup>1</sup>	200Mbs <sup>-1</sup>	34 mV @ 15cm @ 6.8dB/50 $\Omega$ receiver	-48.7 dBm <sup>2</sup>
[8]	CMOS 0.35 $\mu$ m	30mmx35mm	N/A	N/A	10Mbs <sup>-1</sup>	13 mV @ 90cm Receiver gain : N/A	

<sup>1</sup> Calculated from the power consumption and the pulse repetition rate.

<sup>2</sup> Calculated from the measured peak to peak voltage and the receiver gain.

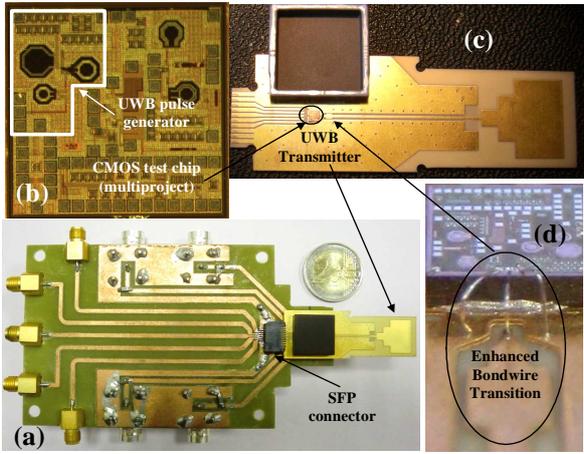


Fig. 13. (a) Transmitter board plugged into the mother board. (b) CMOS multi-project test chip including the UWB pulse generator. (c) UWB transmitter. (d) Enhanced carrier to die wire bond interconnection.

### B. Transmitter measurement results.

The transmitter measurement setup is described in Fig. 14. The transmitter board is driven by a pulse pattern generator (Agilent 81134A). The measurement receiver includes an 8.3dBi horn antenna, a 32dB LNA and a 12GHz real time oscilloscope (Agilent DSO81204B). All the measurements are performed in an anechoic chamber. Fig. 15 shows a pulse received at 80cm range where 700mV peak to peak voltage has been measured. Taking into account the receiver gain, including the antenna, the LNA gain and the cable loss, we can compute the emitted pulse at 1m range. The calculated peak to peak voltage is 4.3mV which corresponds to an emitted peak power of -41.3dBm at 1m range. Fig. 16 shows the normalized spectrum of the received pulse. Considering that our on chip generator is capable of emitting 1.42Vpp pulses, maximum emitted peak power at 1m range that can be delivered by the on chip generator with an ideal package and an ideal antenna can be estimated thanks to Friis free space equation and considering a frequency of propagation of 5.8GHz ( $(3.1 \cdot 10.6)^{0.5}$ ). Calculations indicate a maximum emitted peak power of -40.5dBm at 1m range. This calculated value is closed to -41.3dBm the value obtained in measurement. This demonstrates that the pulses emitted by the chip are not degraded by the antenna and the packaging.

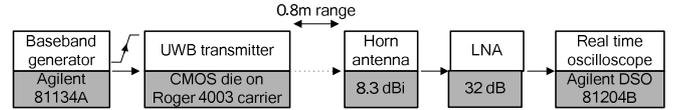


Fig. 14. Measurement setup

Table III compares the proposed transmitter with other 3.1-10.6 GHz published transmitters. The proposed transmitter shows low energy per pulse consumption with high data rate capabilities and high emitted peak power.

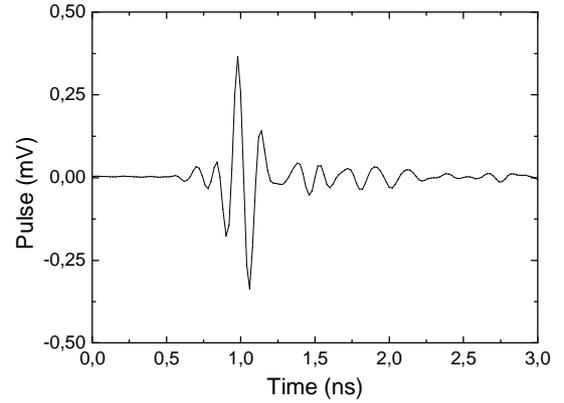


Fig. 15. Received pulse at 0.8 meter range.

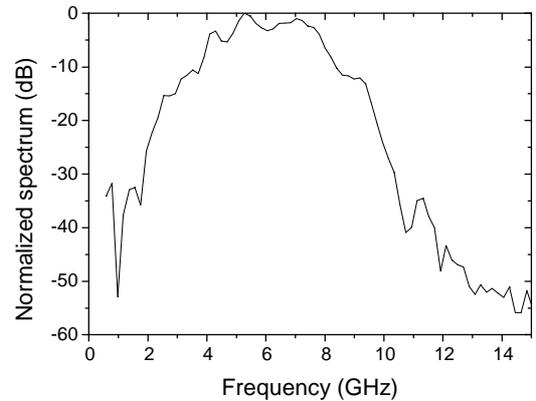


Fig. 16. Normalized spectrum of the received pulse.

## VI. CONCLUSION

A compact UWB transmitter module has been presented. The transmitter uses low cost technologies: a single standard CMOS die, a two metal layer carrier, standard bonding wires and a printed monopole antenna. The transmitter demonstrates a very low energy per pulse consumption (10pJ), a pulse peak power of -41.3dBm@1m and can achieve high data rates (1.2Gb/s). These performances could be useful for applications such as low cost and low power accurate positioning or high data rate short range communications.

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