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Digital Block Design of MIMO Hardware Simulator for LTE Applications

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***Abstract*—This paper presents new frequency domain and time domain architectures for the digital block of a hardware simulator of MIMO propagation channels, with 3GPP TR 36.803 channel models test, for LTE applications. The hardware simulator facilitates the test and validation cycles by replicating channel artifacts in a controllable and repeatable laboratory environment, thus making it possible to ensure the same test conditions in order to compare the performance of various equipments. After the description of the general characteristics of the hardware simulator, the new architectures of the digital block are presented and designed on a Xilinx Virtex-IV FPGA. Their accuracy and latency are analyzed. 3GPP TR 36.803 channel models test are given in details.**

Keywords-Hardware simulator; radio channel; MIMO; FPGA; 3GPP TR 36.803v0.3.0 channel model

I. INTRODUCTION

Multiple-Input Multiple-Output (MIMO) systems make use of antenna arrays simultaneously at both transmitter and receiver to improve the channel capacity and the system performance. Because the transmitted electromagnetic waves interact with the propagation environment (indoor/outdoor), it is necessary to take into account the main propagation parameters for the design of the future communication systems.

Hardware simulators of mobile radio channel are very useful for the test and verification of wireless communication systems. These simulators are standalone units that provide the fading signal in the form of analog or digital samples [1], [2].

The current communication standards indicate a clear trend in industry toward supporting MIMO functionality. A support for higher order of antenna arrays will be required to enable higher channel capacity and system performance. In fact, several studies published recently present systems that reach a MIMO order of 8×8 and higher [3]. This is made possible by advances at all levels of the communication platform as, for example, the monolithic integration of antennas [4] and the design of the simulator platforms.

With the continuous increase of field programmable gate array (FPGA) capacity, entire baseband systems can be efficiently mapped onto faster FPGAs for more efficient prototyping, testing and verification. As shown in [5], the FPGAs provide the greatest flexibility in algorithm design and visibility of resource utilization. Also, they are ideal for rapid prototyping and research use such as testbed [6].

The simulator is reconfigurable with standard bandwidths not exceeding 100 MHz, which is the maximum for FPGA Virtex IV. However, in order to exceed 100 MHz bandwidth, more performing FPGA as Virtex VI can be used [7]. The simulator is configured with the Long Term Evolution System (LTE) and Wireless Local Area Networks (WLAN) 802.11ac standards. The channel models used by the simulator can be obtained from standard channel models, as the TGn 802.11n [8], 3GPP TR 36.803 [9], or from real measurements conducted with the MIMO channel sounder designed and realized at IETR [10]. Different architectures of antenna arrays can be used for outdoor and indoor measurements [11].

At IETR, several architectures of the digital block of a hardware simulator have been studied, in both time and frequency domains [12], [13]. Moreover, [14] presents a new method based on determining the parameters of a channel simulator by fitting the space time-frequency cross-correlation matrix of the simulation model to the estimated matrix of a real-world channel. This solution can be considered only as heuristic method because it shows that the obtained error can be important. Typically, wireless channels are commonly simulated using finite impulse response (FIR) filters, as in [13], [15] and [16]. Nowadays, different approaches have been widely used in filtering, such as distributed arithmetic (DA) and canonical signed digits (CSDs). However, for a hardware implementation, it is easier to use the FFT (Fast Fourier Transform) module to obtain an algebraic product. Thus, frequency architectures are presented, as in [13] and [15].

The previous considered frequency architecture in [13] operates correctly only for signals with a number of samples not exceeding the size of the FFT. However, in this paper, a new frequency domain architecture avoiding this limitation, and a new time domain architecture are both tested with 3GPP TR 36.803 channel models.

The rest of this paper is organized as follows. Section II presents the new frequency and time domain architectures of the digital block. Section III shows the hardware implementation of the digital block for each architecture. Moreover, the accuracy of these two architectures is analyzed. Lastly, Section IV presents some concluding remarks.

* CPER PALMYRE - II Project supported by "Région Bretagne".

II. HARDWARE SIMULATOR: PRINCIPLE, ARCHITECTURE AND OPERATION

The simulator must reproduce the behavior of a MIMO propagation channel. It is able to accept input signals between -50 and 33 dBm. The considered bandwidth is 20 MHz for LTE.

The design of the RF blocks for UMTS (Universal Mobile Telecommunications System) was completed during a previous project [13]. The objectives of PALMYRE II* project concern the channel models and their hardware implementation into the MIMO simulator.

A. Channel Model

3GPP TR 36.803 channel model is used for mobile wireless applications. A set of 3 channel models are implemented to simulate the multipath fading propagation conditions. A detailed description is presented in [9]. The definitions of the 3 specific channel models are shown in the following Table I, and their relative powers are calculated by taking the LOS (Line-Of-Sight) impulse response as reference. The sampling frequency and the period are f_s = 180 MHz and $t_s = 1/f_s$ respectively.

TABLE I. PATH LOSS FOR 3GPP TR 36.803 CHANNEL MODELS

Tap index	Pedestrian A model (EPA)		Vehicular A model (EVA)		Typical Urban model (ETU)	
	Excess delay [s]	RP [dB]	Excess delay [s]	RP [dB]	Excess delay [s]	RP [dB]
1(Ref)	0 x t_s	0.0	0 x t_s	-0.0	0 x t_s	-1.0
2	1 x t_s	-1.0	1 x t_s	-1.5	2 x t_s	-1.0
3	3 x t_s	-2.0	7 x t_s	-1.4	6 x t_s	-1.0
4	4 x t_s	-3.0	15 x t_s	-3.6	10 x t_s	-0.0
5	5 x t_s	-8.0	18 x t_s	-0.6	11 x t_s	-0.0
6	9 x t_s	-17.2	35 x t_s	-9.1	25 x t_s	-0.0
7	21 x t_s	-20.8	54 x t_s	-7.0	80 x t_s	-3.0
8	-	-	86 x t_s	-12.0	115 x t_s	-5.0
9	-	-	125 x t_s	-16.9	250 x t_s	-7.0

Fig. 1, Fig. 2 and Fig.3 presents the impulse responses of EPA, EVA and ETU models respectively.

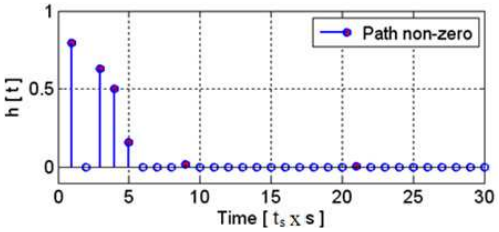


Figure 1. EPA channel model.

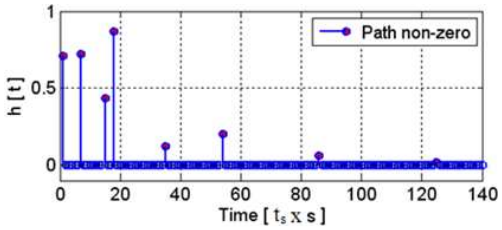


Figure 2. EVA channel model.

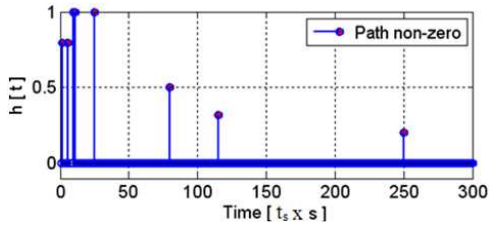


Figure 3. ETU channel model.

However, the channel models can also be obtained from measurements by using a time domain MIMO channel sounder designed and realized at the IETR [10], as shown in Fig. 4.



Figure 4. MIMO channel sounder: receiver and transmitter.

B. Digital Block

According to the considered propagation environments, Table II summarizes some useful parameters for LTE standard. The number of samples is:

$$N = W_t \times f_s \quad (1)$$

where W_t represents the width of the time window of the impulse response of the propagation channel.

TABLE II. SIMULATOR PARAMETERS

	Type	Cell Size	$W_{t\,eff}(\mu s)$	N	$W_t(\mu s)$
LTE	Rural	2-20 km	20	512	10.24
(B = 20 MHz)	Urban	0.4-2 km	3.7	128	2.56
(f_s = 50 MHz)	Indoor	20-400 m	0.7	64	1.28

In order to have a suitable trade-off between complexity and latency, two solutions are considered: a time domain approach and a frequency domain approach. For indoor environments, W_t is smaller than 1 µs. Therefore, the time domain approach is more suitable to use, because a FIR filter has, in spite of its relative complexity, much lower latency (less than 1 µs). N is the closest 2^n value which is imposed by the FFT. Therefore, both approaches can be used according to the considered propagation environment.

A description of the simple architectures of the digital block for frequency and time domains is given in [13]. In this section, we present a new improved frequency domain and a time domain architectures based on a FIR filter.

1) *New Frequency Domain Architecture*

The new frequency architecture has been verified with Gaussian impulse response and a complete detailed description

is presented in [17]. It operates correctly for signals with a number of samples exceeding the size of the FFT module.

For 3GPP TR 36.803 channel model, N_{eff} = 21 samples (N = 32 samples) for EPA model, 125 samples (N = 128 samples) for EVA model and 250 samples (N = 256 samples) for ETU model. However, to test the new architecture, it is mandatory to extend each partial input signal with a "tail" of N zeros as presented in [17]. Therefore, the FFT module used has 64 samples with EPA model, 256 with EVA model and 512 with ETU model. The new frequency architecture with ETU model is presented in Fig. 5.

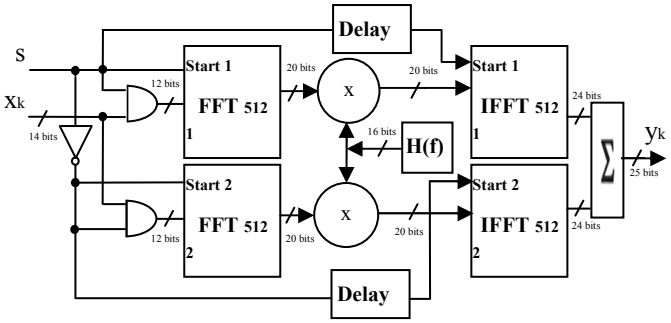


Figure 5. Frequency architecture of a SISO channel.

The truncation block, used in [12] and [13], is located at the output of the digital adder. It is necessary to reduce the number of bits after the sum of the IFFT blocks to 14 bits so that these samples can be accepted by the DAC (Digital-to-analog converter), while maintaining the highest accuracy. The immediate solution is to keep the 14 most significant bits. It is a "brutal" truncation. However, for low values of the output of the digital adder, the brutal truncation generates zero values to the input of the DAC. Therefore, a better solution is the sliding window truncation presented in fig. 6 which uses the 14 most effective significant bits [12].

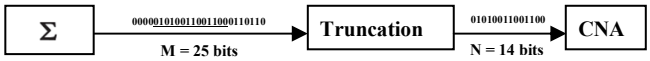


Figure 6. Sliding window truncation, from 31 to 14 bits.

2) *Time Domain Architecture*

Studies of the FIR filter with 64 points are presented in [12]. However, for ETU model, N = 250 samples. This model imposes the use of 9 multipliers. The general formula for a FIR 250 with 9 multipliers is:

$$y_q(i) = \Delta t \sum_{k=1}^{9} h_q(i_k).x_q(i - i_k) \quad (2)$$

Fig. 7 presents the internal architecture of a filter FIR 250 with 9 non-zero positions. Also, it present packs of impulse responses with a refresh frequency f_{ref} depending on the channel, which will allow the test of a time variant impulse response. Therefore, we have developed our own FIR filter instead of using Xilinx MAC FIR filter to make it possible to reload the FIR filter coefficients. f_{ref} must be at least twice the maximum Doppler frequency. Thus, t_{ref}= p/f_{ref} where p is the number of subchannels of the MIMO channel.

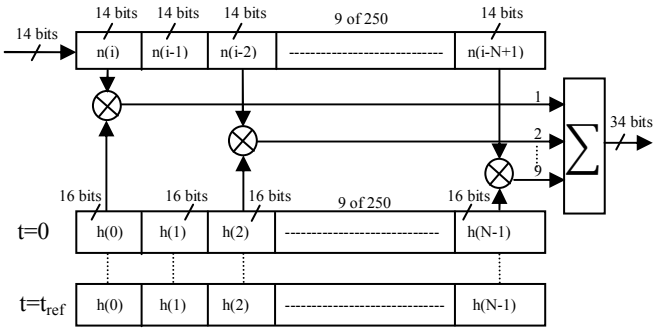


Figure 7. FIR 250 with 9 multipliers.

III. IMPLEMENTATION

In order to implement the hardware simulator, the adopted solution uses a prototyping platform (XtremeDSP Development Kit-IV for Virtex-4) from Xilinx [7], which is presented in Fig. 9 and described in [17].



Figure 9. XtremeDSP Development board Kit-IV for Virtex-4.

The simulations and synthesis are made with Xilinx ISE [7] and ModelSim software [18].

A. Implementation and Results of Frequency Architecture

The V4-SX35 utilization summary after synthesis, mapping and route, for the frequency architecture with FFT 512 and IFFT 512 blocks, is given in Table III.

TABLE III. VIRTEX-4 SX35 UTILIZATION FOR 2 FFTS AND 2 IFFTS IN PING-PONG FREQUENCY ARCHITECTURE

Number of slices	4,599 out of 15,360	30%
Number of bloc RAM	36 out of 192	19%
Number of DSP48s	46 out of 192	24%

In order to determine the accuracy of the digital block, a comparison is made between the theoretic and the Xilinx output signals. With Gaussian input signal, the theoretic output signal can be obtained. Therefore, an input Gaussian signal x(t) is considered and long enough to be used in streaming mode (a length of $3W_t$ is sufficient):

$$x(t) = x_m e^{-\frac{(t-m_x)^2}{2\sigma_x^2}} = N(x_m, m_x, \sigma_x^2), 0 \le t \le 3W_t \quad (3)$$

where N = 512, $W_t = N/f_s$, $m_x = 3W_t/2$ and $\sigma_x = m_x/4$.

The impulse response corresponds to ETU channel model has 9 paths. [$-V_m$,V_m] is the full scale of the converters, with V_m = 1 V and $x_m = V_m/2$. The theoretic output signal is the sum of the 9 Gaussian signals corresponds to the 9 paths of the impulse response, and it's presented by:

$$y(t) = \sum_{k=1}^{9} N(y_{mk}, m_{yk}, \sigma_y^2) = \sum_{k=1}^{9} h_k.x(t - i_k t_s) \quad (4)$$

The relative error is determined for each output sample by:

$$\varepsilon = \frac{Yxilinx - Ytheoretical}{Ytheoretical} . 100\ [\%] \qquad (5)$$

Therefore, the Signal-to-Noise Ratio (SNR) is given by:

$$SNR = 20.\log_{10} \left| \frac{Ytheoretical}{Yxilinx - Ytheoretical} \right| [dB] \qquad (6)$$

Fig. 10, Fig. 11 and Fig. 12 show the theoretical and the Xilinx signals at the output with their relative error for the new frequency architecture using 3GPP TR 36.803 EPA, EVA and ETU models respectively, with LTE signals (f_s = 50 MHz).

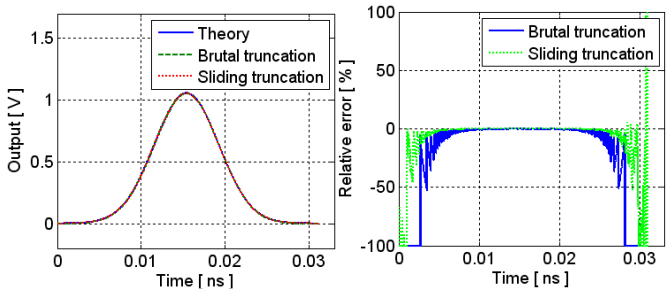


Figure 10. The theoretic and Xilinx output signals for the frequency architecture and the relative error with 3GPP TR 36.803 EPA channel model.

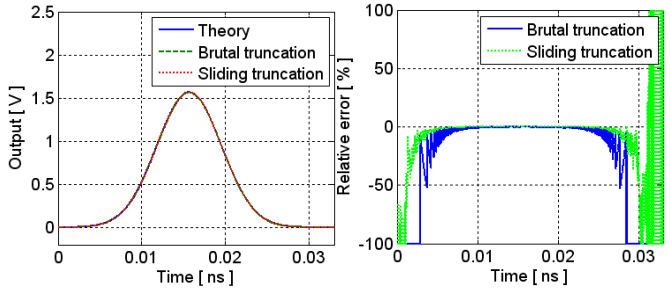


Figure 11. The theoretic and Xilinx output signals for the frequency architecture and the relative error with 3GPP TR 36.803 EVA channel model.

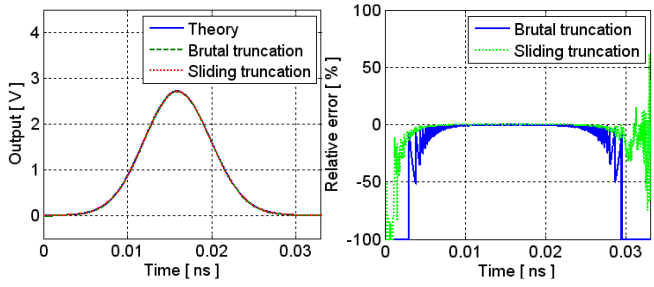


Figure 12. The theoretic and Xilinx output signals for the frequency architecture and the relative error with 3GPP TR 36.803 ETU channel model.

After the DAC block, the signal is limited between [-V_m,V_m] with V_m = 1. Therefore, a reconfigurable amplifier block after the DAC is mandatory placed to multiply the signal with 2^{-k_0} where k_0 is an integer and 0.5 V < $2^{k_0} \times y_{max}$ < 1 V.

The relative error is high only for small values of the output signal because the Gaussian signal is close to 0.

B. *Implementation and Results of Temporal Architecture*

Table IV shows the device utilization for a single FIR filter 250 with 9 taps (9 multipliers).

TABLE IV. FIR SIMULATED ARCITECTURE

Number of slices	1,847 out of 15,360	12 %
Number of bloc RAM	9 out of 192	4.6 %
Number of multipliers	9 out of 192	4.6 %

Before each operation, the 9 coefficients of the FIR filter are stored first in 1 shift register of length 9 via the USB port of the development board, then in the FPGA dual-port RAM.

Fig. 13, Fig. 14 and Fig. 15 show the theoretical and the Xilinx signals at the output with their relative error for the time domain architecture using 3GPP TR 36.803 EPA, EVA and ETU models respectively, with LTE signals (f_s = 50 MHz).

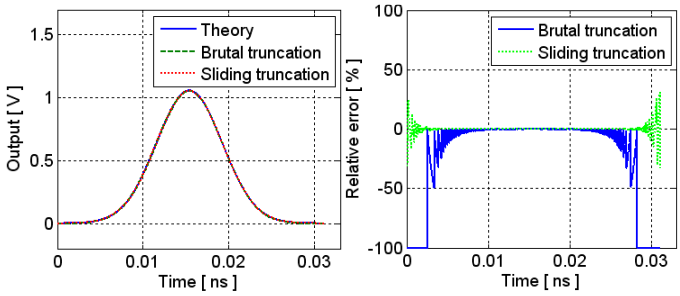


Figure 13. The theoretic and Xilinx output signals for the time domain architecture and the relative error with 3GPP TR 36.803 EPA channel model.

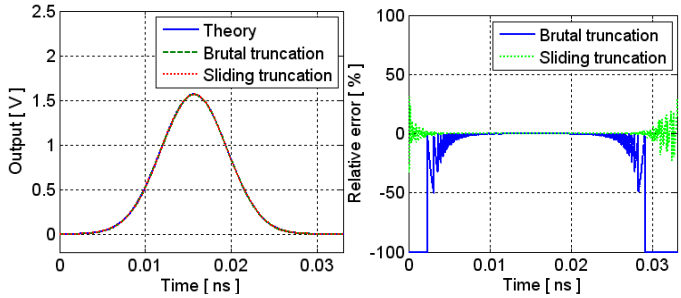


Figure 14. The theoretic and Xilinx output signals for the time domain architecture and the relative error with 3GPP TR 36.803 EVA channel model.

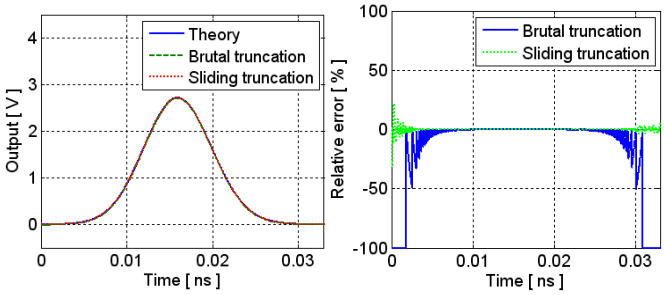


Figure 15. The theoretic and Xilinx output signals for the time domain architecture and the relative error with 3GPP TR 36.803 ETU channel model.

The relative error is high only for small values of the output signal because the Gaussian signal is close to 0.

C. *Accuracy and occupation of slices with all 3GPP models*

The global values of the relative error and SNR of the output signal before and after the final truncation are:

$$\varepsilon = \frac{\|e\|}{\|y\|} \times 100\ [\%] \qquad (7)$$

$$SNR = 20 \times \log_{10} \frac{\|y\|}{\|e\|} [dB] \qquad (8)$$

where y is the theoretic output signal, yc is the computed signal (with or without truncation) and e = yc - y. For a given digital signal $x = [x_1, x_2, \ldots, x_N]$, $\|x\|$ is:

$$\|x\| = \sqrt{\frac{1}{N}\sum_{k=1}^{N} x_k^2} \quad (9)$$

Table V shows the global values of the relative error and the global SNR with sliding window truncation, and the occupation on the FPGA, for the frequency domain (with the size of FFTs used) and time domain (with the size of the FIR used) architectures, for all 3GPP TR 36.803 channel models.

TABLE V. COMPARISON BETWEEN THE PROPOSED ARCHITECTURES FOR DIFFERENT MODELS

EPA model	**Frequency Architecture**		**Time Architecture**	
Relative Error	Error (%)	SNR (dB)	Error (%)	SNR (dB)
	0.1115	59.05	0.0137	77.26
Slices (%)	20 (with FFTs 64)		11(with FIR 21)	
EVA model				
Relative Error	Error (%)	SNR (dB)	Error (%)	SNR (dB)
	0.1066	59.44	0.0125	78.09
Slices (%)	26 (with FFTs 256)		12(with FIR 125)	
ETU model				
Relative Error	Error (%)	SNR (dB)	Error (%)	SNR (dB)
	0.1051	59.56	0.0122	78.26
Slices (%)	30 (with FFTs 512)		12(with FIR 250)	

D. Discussion

We compare the time domain architecture with the new frequency domain architecture. According to Table V, three points resume the comparison: the precision, the occupation on the FPGA and the latency.

With sliding truncation, the relative error does not exceed 0.12 % (for the worst case, with EPA model), which is sufficient for applications of the hardware simulator.

However, in term of occupation of slices on the FPGA Virtex IV, the time domain architecture has a maximum of 12 % in contrast with the occupation of the frequency domain architecture which is 30 %. Thus, the time domain architecture presents one advantage which allows the implementation of 8 SISO channels with EPA model (and 6 for EVA and ETU models). Thus, for a 4x2 MIMO channel, this architecture uses 7x8 = 56 multipliers and produces an occupation of 88 % of slices on the FPGA.

The time domain architecture has a latency of 115 ns with ETU model. However, the frequency domain architecture has much higher latency of 9 µs.

Therefore, the time domain architecture is more efficient to use. However, to obtain an algebraic product, the new frequency domain architecture is considered. In this case, the use of more performing FPGAs as Virtex VII [7] is mandatory to solve the occupation problem, and which will provide the use of many SISO channels and be able to test up to 10x10 MIMO systems.

IV. CONCLUSION

After a comparative study, in order to reduce occupation on the FPGA, the error and the latency of the digital block, the time domain architecture present the best solution for outdoor environments, which has been tested in this paper with 3GPP TR 36.803 channel models.

Nowadays, we work with a configuration which requires 3 XtremeDSP Development Kit-IV. More measurement campaigns will be carried out with the MIMO channel sounder realized by IETR, for various types of environments (indoor, outdoor). The final objective of these measurements is to obtain realistic and reliable impulse responses of the MIMO channel in order to supply the digital block of the hardware simulator. Tests will be done by using time-varying channels, thus, the architectures will be completed to obtain a "dynamic" system. A Graphical User Interface will be designed to allow the user to reconfigure the channel parameters.

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