Broadband digitization for cable tuners front-end

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***Abstract* —The RF front-end for forthcoming broadband receivers of cable modems is investigated. The aim is the digitization of the whole RF cable input spectrum, which spreads from 50MHz to 1GHz. In this paper, several architectures are proposed and evaluated. We introduce a general cost function in order to compare these proposals. We verify that the complete digitization of the cable input spectrum is a challenging problem, and show that a solution based on analytic signals and downconversion is promising.**

I. INTRODUCTION

Multi-stream reception is a key point for future products in cable modem, terrestrial and satellite TV. This implies simultaneous reception of several channels located anywhere on the whole band or partial RF band. This is a required feature for watch-and-record, picture-in-picture, or bonded channel applications. The simultaneous reception supposes either the digitization of the whole band or the use of as many tuners as wanted channels. The spectrum of interest spreads from 50MHz to 1GHz, and one might want to simultaneously receive up to 16 channels of 6MHz. Of course, using for instance 16 tuners Integrated Circuits for receiving 16 channels will be severely over-killing in terms of cost and power. Therefore it is of particular importance to investigate solutions for the complete digitization of the 1GHz input spectrum. Broadband digitization is indeed a studied matter, for example in [1]. Furthermore, this is a foreseen direction in RF sampling architecture: the whole RF band is sampled very early in the signal path. This reduces RF hardware, allows most of the processing to be done in digital domain, thus facilitates reconfigurability by software (Software Radio).

The well-known Analog-to-Digital Converters (ADC) architectures are not adapted to such an application. Flash ADCs, pipeline ADCs, Successive Approximation Register (SAR) ADCs and ΣΔ ADCs are either high speed or high resolution. In the targeted application, we need both high-speed and high-resolution. As an objective, we consider the following specifications, which are in accordance with the normalization [2] with an additional security margin. The maximum input frequency being 1GHz, we select a sampling frequency of 2.2GHz. We also want a minimum Signal-to-Noise Ratio (SNR) of 50dB. This value leads to 10 bits of resolution. Of course, low consumption and low cost are highly relevant objectives in such mass devices.

According to the literature, it seems that parallel structures for ADCs are a key for high-speed, high-resolution data converters. Time-interleaving (TI) [3], Parallel Delta-Sigma (πΔΣ) ADC [4], Hybrid Filter Banks (HFB) [5] are potential architectures. However, given the very high sampling frequency of our application, the direct use of such solutions seems still difficult. Another possible way to cope with this problem is to divide the issues by splitting the spectrum into subbands. Each reception chain begins with a LNA. It is an important block but as it is common to all the following components and architectures, it is out of the scope of the present analysis which focuses on the ADC structures and performances.

In section II, we review the literature and propose several potential architectures. In section III, we introduce a general cost function in order to compare the different solutions. The results are presented and discussed in section IV.

II. POSSIBLE ARCHITECTURES

This section first gives a brief review of the literature and of the current state-of-the-art. For comparison purposes, we select a particular high performance ADC [6], adapt it so that it meets our requirements and give an ideal extrapolation of a possible ADC for years 2012-2013. Both the existing ADC and the extrapolated model will be used as guideline for the evaluation of our proposals. These proposals and architectures are discussed in paragraphs II-C to II-E.

A. Literature review

ADCs are often characterized by the sampling rate and the resolution. This latter is defined by the SNR and the Effective Number of Bits (ENOB). Surface and power consumption are key elements when addressing a market. The following figure-of-merit (FoM) used in [7], [8], links three of the parameters:

$$\mathrm{FoM} = \frac{\mathrm{P}}{2^{\mathrm{ENOB}} \times \mathrm{Fs}}$$

The ADC AT84AS008 [9] almost reaches the targets but it has a high FoM=9.2pJ/conversion-step. Thus, we select another ADC [6], which is quite close to these specifications. This Time-Interleaved pipeline ADC has a sampling rate of 1.8Gsps and 10-bit resolution. It is implemented with a 0.35-µm BiCMOS, achieves an ENOB of 7.19 bits with a 764-MHz input while consuming 3.5W. The chip's size is around 40mm².

We estimate the power consumption and the area of the same ADC working at 2.2Gsps thanks to an extrapolation. Increasing the sampling rate implies a rise in the number of time-interleaved ADCs. Indeed, 29 time-interleaved ADCs working at 77.75Msps are required. The analog surface is proportional to the number of channel ADCs, and so is the power consumption. From the chip micrograph of [6], we assess the digital surface to be a quarter of the whole chip in 0.35-µm BiCMOS. Scaling it down to a newer technology, a better FoM could be obtained. For instance, in 65nm, a FoM of 7.6pJ/conversion-step instead of 13.2pJ/conversion-step could be reached. This is also better than 9.2pJ/conversion-step of [8].

The performances of the reference [6] (first line), the extrapolated ADC (second line) and the commercial ADC [9] are recapitulated in the following table Table 1.

TABLE I. COMPARISON OF THE ADCS

	Fs (MHz)	SNR (dB)	ENOB (bits)	S (mm²)	P (W)	FoM (pJ/conv.step)	Techno (nm)
[6]	1800	45	7.2	40	3.5	13.2	350
e	2200	50	8	38.6	4.3	7.6	65
[9]	2200	48.1	7.7	u	4.2	9.2	u

e: [6] extrapolated, u: unavailable

B. Ideal reference architecture

An ideal extrapolated reference for conversion is proposed as a guideline. Based on the current state-of-the-art, we model a targeted ADC for years 2012-2013. This one is a Time-Interleaved ADC with 10-bit resolution, with a 2.2GHz sampling frequency. It reaches 50dB SNR and a FoM of 3.5pJ/conversion step. The surface is no more than 30mm² and it consumes 2W. Reaching these performances is currently really challenging.

This virtual ADC is used here as a guideline for the design, and is a basis for the comparison. As depicted in Fig. 1, the unique ADC digitizes the whole band, after the LNA.

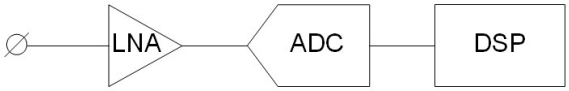

Figure 1. Unique ADC

The main difficulty with this solution is the incredible required rate, which in turn imposes severe constraints on all individual components. In order to relax these constraints, by decreasing the sampling frequency, a simple idea is to split the spectrum of interest into several subbands.

C. Subband splitting with real signals

In this case, a bank of analog filters divides the input spectrum into *M* subbands, with for instance

$$B = \frac{F_{max} - F_{min}}{M}$$

(case of equal bandwidths), where F_{min}=50MHz and F_{max}=1GHz denote the edges of the total bandwidth of the input spectrum. Automatic Gain Control (AGC) components are implemented in order to compensate filters losses and drive the ADCs with a full-scale signal, as depicted in Fig. 2.

The surface of the final integrated circuit is an important parameter. With this in mind, we can already note that the number of subbands M has to be limited. The studied cases correspond to a division into two, four and eight subbands. As far as the filters are concerned, they are specified by their order, type and cutoff frequencies, whereas the sampling frequency and the SNR are of interest for the ADCs.

The most stringent objective is aliasing rejection, which should be around 60dB. On the one hand, the filters must attenuate the replicas by 60dB. On the other hand, the sampling rate determines the location of the replicas. Hence we have a necessary trade-off between the steepness of the filter, thus the order and type, and the sampling rate of the ADC. Furthermore, the required SNR depends on the sampling rate, but also on the power rejected by the filters, which is related to the number of subbands. Indeed, power rejection is defined by:

$$\text{Power\_rejection} = \frac{P_{\text{wanted/total,out}}}{P_{\text{wanted/total,in}}}$$

$$P_{\text{wanted/total,out}} = \frac{P_{\text{wanted/total,in}}}{M}$$

$$\text{Power\_rejection}_{|\text{dB}} = -10\log(M)$$

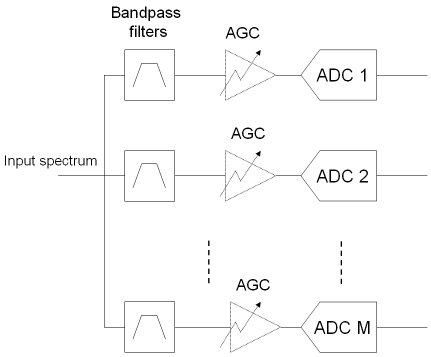

Figure 2. Subband splitting with real signals

The sampling rate is chosen such that the replicas of the considered spectrum fall out of the band, or at least can be easily filtered. In the first case, the role of the filters is only to reject power, not to limit the aliasing; therefore their order is lower than in the second case. The method of bandpass sampling [10] can be used to reduce the sampling frequency, but this often implies a high-order filter. As a matter of fact, a unique sampling rate for the *M* ADCs is only possible if it is higher than 2 GHz, which is nothing but Shannon-Nyquist condition for the whole band. It is easy to check that in order to lower the sampling rate below 2 GHz, we should have at least two different sampling frequencies.

Since all the parameters are linked together, there is a high number of possibilities. These were exhaustively studied, and the main conclusions are as follows:

- We need two sampling frequencies at least.
- Bandpass sampling is not well-adapted for large band subsampling.
- Increasing the number of subbands raises the surface and the power consumption of the architecture.
- The filters that have to reject aliasing that falls in the whole band have to have high orders and thus are difficult to realize.

The main difficulty in this scheme is that it requires several sampling frequencies. Should we be able to suppress negative frequencies components, then it would be possible to avoid aliasing and exhibit a much lower sampling frequency as [1] and [11]. The use of a Hilbert transform to generate analytic signals seems a must.

D. Subband splitting with analytic signals

After the bank of analog filters and AGCs, a bank of Passive Polyphase Filters (PPF) is added for the generation of

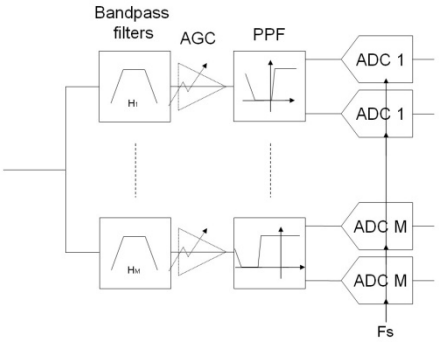

Figure 3. Subband splitting with analytic signals

the analytic signals. Obviously, the number of ADCs doubles, as shown in Fig. 3.

The constraints on the PPF concern the image rejection ratio (IRR) and the bandwidth to suppress. As in the case of the filters for aliasing rejection, the PPF requires a 60dB IRR over the bandwidth of interest, to get rid of the negative frequencies, which is challenging regarding the state-of-the-art. Yet, the main advantage is that the sampling rate can be unique and that it only has to respect $Fs>B$, instead of Shannon's condition. However, there still exists a trade-off between the sampling rate and the complexity of the filters.

E. Subband splitting with analytic signals and downconversion

An improvement of the previous structure is described now. Since the actual frequencies at the input of the ADCs can still be very high, the idea is to relax the design of the ADC, namely the sample-and-hold part, by adding a down-conversion stage. This approach is close to zero-IF/ Near-zero-IF RF architecture: the signal is down-converted to a center intermediate frequency (IF) which is close to DC.

Nevertheless, as opposite to classical ZIF approach, the broadband downconverted signal can put high constraints on the image-reject mixer (PPF+Mixer), and on the ADC matching. Two types of downconverters are studied: the double-balanced mixer and the quadrature mixer.

1) Double-balanced mixer (DBM)

RF, LO and IF are real signals. In our case, the RF signals are the output of polyphase filters, so we will need a DBM for each branch. If we consider that the polyphase filters reject the negative frequencies by 60 dB, there is no image issue.

2) Quadrature mixer (QM)

LO and IF are quadrature signals. The requirement on Image Rejection is still 60 dB. The constraints can be divided into the PPF and the QM: 30dB each seems to be a correct compromise.

$$\mathrm{IRR} \approx \mathrm{Quad}_{\mathrm{LOdB}} + \mathrm{Quad}_{\mathrm{RFdB}} \approx 60\mathrm{dB}$$

Hence, using this simple approach, we see that the PPFs become much more feasible [12].

Finally, there are two strategies for the choice of the LO.

a) Homodyne architecture: in such architecture, the centering of each subband on zero requires as many LO frequencies as subbands, i.e. M. The maximum input frequency is $B/2$, but the solution is clearly expensive in terms of clock generation.

b) Heterodyne architecture: in this solution, the middle frequency of the whole band is 525MHz and is a possible LO frequency. Consequently, the clock generation is quite easy.

III. A COST FUNCTION AND COMPARISONS

For decision purposes, as well as the selection of the best working directions, we need an objective measure of the performances of the different solutions. With this in mind, we introduce a simple, but general cost function. Since the two key parameters are surface and power consumption, we simply choose to define the cost function as the function that associates the two indicators {Surface, Power} to any set of parameters describing the solution. This leads us to the comparison Fig. 5. The main steps of the computation are described below.

A. Surface estimation

1) Filters

The filters split the input spectrum into M subbands. The first one is a lowpass filter, followed by M-2 bandpass filters and a final highpass filter. They are passive and their orders depend on the sampling frequency. Thus, the filters' complexity should be taken into account. Given the order, the bandwidth and the cutoff frequency(ies), we find the components' values and estimate their surface.

2) ADCs

The ideal reference ADC imagined in II-B is a Time-Interleaved ADC. The number of interleaved elementary ADCs depends on the sampling frequency Fclk of the ADC. The surface Sref of the whole ADC is therefore nearly proportional to the number of unit ADCs. Thus, if we reduce

the sampling rate Fs, the number of unit ADCs will be reduced proportionally, and so the surface S. Indeed, we have:

$$\frac{Fclk}{Fs} = \frac{Sref}{S}$$

3) Others

The surface of the other elements, namely AGCs, mixers and PPFs are estimated from the state-of-the-art.

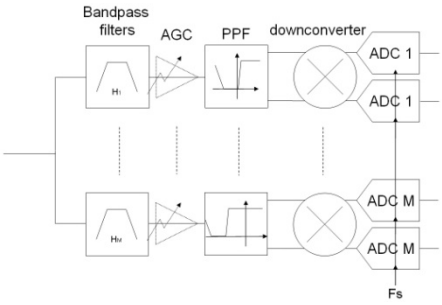

Figure 4. Subband splitting with analytic signals and downconversion

B. Power consumption estimation

1) ADCs

In order to obtain a first estimate of the power consumption, we suppose to work with ADCs with a known, constant, figure of merit FoM (1). For instance, if the ADCs are in the same family as the ADC presented in II-A, we have FoM=7.6pJ/conversion-step, and if they are derived from the ideal ADCs of II-B, we assume that FoM=3.5pJ/conversion-step.

Then, from the $SNR_{Nyquist}$, we deduce the ENOB, and with a given sampling frequency, we are able to estimate the power consumption of each ADC as

$$P \approx FoM \times 2^{ENOB} \times Fs$$

2) Others

We do not take the subband filters' and the polyphase filters' power consumption into account since they are passive. The power consumption of the AGCs and the mixers are estimated from the state-of-the-art.

C. Comparisons

We compare three situations: (1) refers to the reference model, either (a) with the figures extrapolated from the ADC of [6], or (b) with an ideal model. Architectures (2a) and (2b) correspond to an example of subband splitting with real signals for *M*=4 and the architectures (3a) and (3b) to subband splitting with analytic signals and downconversion for *M*=2. The case of subband splitting with analytic signals without downconversion is not presented because the PPF is not feasible a priori: Fig. 5 presents the comparison as a graph of power consumption versus the surface for each studied architecture. We verify that the ones studied in II.E is equivalent to the reference ones according to these parameters but are the easiest to realize because of the reduction of the sampling rate and the low-order filters. Furthermore, we can notice that power consumption is half of [9].

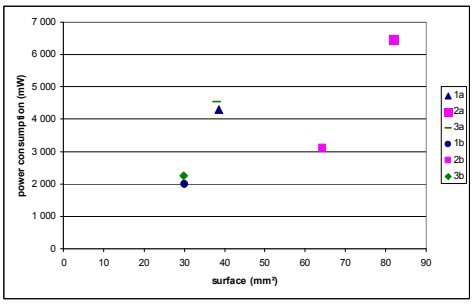

Figure 5. Power consumption versus surface for each studied architecture

IV. CONCLUSION

Our results show the interest of subband splitting with analytic signals and downconversion. It is almost equivalent to the ideal reference. In terms of feasibility, this solution is easier because the filters have low orders, the LO frequency and the sampling frequency are related together, the PPF and the mixer need 30 dB image rejection each, which can be found in the literature. Furthermore, the design of the ADC is easier when the sampling rate is small.

Of course, we are aware that there are many possibilities and the figures could be different. Some improvements are planned, e.g. working on choice of the family of ADC for this type of digitization. One can also imagine to switch-off unused subbands, in order to save power consumption. For example, if there are 5 channels to receive and 4 subbands, we could statistically switch-off one subband out of 4. Finally, noise has not been evaluated in the architectures yet.

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