Design, optimization and realization of an HFB-based ADC

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Abstract— **This paper presents a two-channel Hybrid Filter Bank (HFB) Analog-to-Digital Converter (ADC) that targets broadband digitization, for Cognitive Radio (CR) applications. The proposed architecture partitioning uses low-cost third order Butterworth analog filters and fourth order digital IIR filters. The optimization algorithm combines direct simplex search, minimax methods and a perturbation strategy to avoid local minima. A sensitivity study of the analog filters quantifies the impact of poles and zeros spread on system performance. Finally, the experimental results obtained from our concrete realization are reported. The measurements show the aliasing rejection provided by HFB structure and confirms the parallel architecture sensitivity to analog mismatches.**

I. INTRODUCTION

In the context of Cognitive Radio (CR), processing of signals with bandwidth of 1GHz is required. Several mixer-based receivers can be used in parallel in order to capture the required bandwidth, at the price of cost, power and analog complexity. An attractive way to address this reception problem is to design an RF sampling architecture. This approach offers more flexibility, as most of the processing is now moved to the digital domain. However, this puts tough requirements on the Analog-to-Digital Converter (ADC): the wide signal bandwidth requires a high sampling rate (>2Gsps), while the lack of RF selectivity and the non-uniform input power spectral density (PSD) leads to high dynamic range requirement (>10bits).

The current Analog-to-Digital Converters architectures are not adapted to such an application. Flash ADCs, pipeline ADCs, Successive Approximation Register (SAR) ADCs and $\Sigma\Delta$ ADCs are either high speed or high resolution. According to the literature, parallel structures for ADCs are a key for the design of high-speed, high-resolution data converters. Time-interleaving (TI) [1], Parallel Delta-Sigma ($\pi\Delta\Sigma$) ADC [2], Hybrid Filter Banks (HFB) [3] are potential architectures.

An analysis of an HFB-based ADC solution is proposed in this paper, together with original contributions, namely concerning (a) the design of the digital synthesis bank, and (b) the realization of the architecture. These are valid independently of the ADC architecture. The principle of the HFB and main relations are recalled in section II. In the next section, we explain the main implementation choices, present

an algorithm for the optimization of synthesis filters. Section IV describes the realization of the HFB and presents some results.

II. PRINCIPLE OF HFB

Hybrid filter banks (HFB) employ both a bank of analog filters H_i, called analysis bank, and a bank of digital filters F_i, the synthesis bank.

The analog filters split the input into sub-bands. Each ADC then digitizes each sub-band at the sampling rate of $Fs=Fe/M$, where M is the number of channels and Fe is the sampling rate of the global ADC. The analysis structure is then followed by up-samplers-by-M and digital synthesis filters. Finally, the M channels are recombined at the output. So doing, the output of the HFB is the digital equivalent of the analog input, up to reconstruction errors that must be minimized.

Actually, the HFB shall be designed so as to fulfill, as far as possible, the so-called Quasi-Perfect Reconstruction (QPR) condition. This leads to the main advantage of the architecture which is that aliasing is tolerated in each sub-band, but is attenuated, ideally suppressed, by the recombination of the outputs of the synthesis filters.

We have selected a two-channel HFB architecture in order to minimize implementation cost of the analog filters as shown in Fig.1.
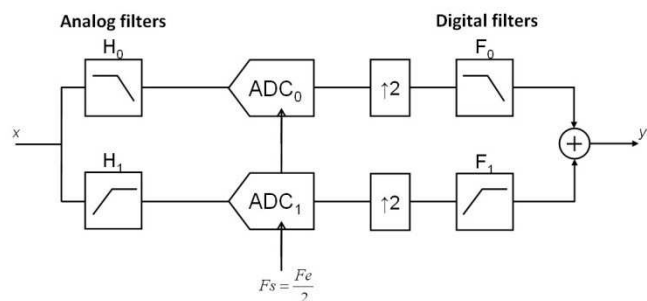

Figure 1.   HFB architecture

The following equations stand for this particular case, as studied in [4].

Let $X(j\omega)$ and $Y(e^{j\omega Te})$ be the Fourier transforms of the input x(t) and the output y(n) of the system. Then, we have:

$$Y(e^{j\omega Te}) = G_{TF}(j\omega).X(j\omega) + G_{AF}(j\omega).X\left(j\omega - j\frac{\pi}{Te}\right)$$

with $G_{TF}(j\omega) = H_0(j\omega).F_0(e^{j\omega Te}) + H_1(j\omega).F_1(e^{j\omega Te})$ (1)

and

$$G_{AF}(j\omega) = H_0\left(j\omega - j\frac{\pi}{Te}\right).F_0(e^{j\omega Te}) + H_1\left(j\omega - j\frac{\pi}{Te}\right).F_1(e^{j\omega Te}) \quad (2)$$

In these relations, G_{TF}, as given by (1), is the distortion (or transfer) function while G_{AL} in (2) is the aliasing function. The overall goal of the design of the HFB is to approach a perfect reconstruction (PR), i.e. G_{TF} should be a pure delay and G_{AF} should be null. These conditions can be satisfied with a digital filter bank but can only be approached with Hybrid Filter Banks. Thus, we have specified a maximum distortion of the transfer function (1) and a maximum of aliasing rejection (2), so that the digitized output is considered sufficiently accurate for being further processed. In the present work the following targets have been set: $\max(G_{TF})<0.5$dB and $\max(G_{AL})<-70$dB.

So as to improve the performances, we introduce a guard band on each part of the band of interest, as shown in [5]. In this case, G_{TF} and G_{AF} are defined on the band of interest.

There are many ways to implement an HFB-based ADC. These are discussed below, with highlights on our particular choices.

III. IMPLEMENTATION

A. Choice of the filters

The performance of HFB architecture relies on the design of the filter banks. Several solutions have been proposed to construct an HFB-based ADC. As PR is reachable with digital filter banks, a possible approach consists in using a Z-to-S transform to design the continuous-time analog filters [6]. However, this method results in high-order filter bank [7]. Specifically, the order of each analog filter equals the order of the prototype multiplied by the degree of the transform. A second approach consists in adjusting the poles and zeros of the analog filters so as to minimize the reconstruction errors. Another solution is to first optimize the analog filters and then, with the analog filters fixed, design the digital synthesis filters [8]. In [9], it is proposed to use power complementary filters for a two-channel HFB-based ADC, which are characterized by special relations between the numerators and denominators of the transfer functions of the analog filters. The previous approaches suffer either from the difficulty to design the required analog filters at 1GHz, or from the too high FIR number of taps.

With implementation cost in mind, we have decided to use standard and fixed analog filters with low-complexity. The complexity associated to the research of the QPR is thus reported on the optimization of the digital synthesis filters. In this part, we can better afford high-order synthesis filters to ensure QPR. However, we still use IIR structures for the synthesis filters so as to lower the filter order, compared to FIR filters. Stability issues of IIR filters have been taken into account in the optimization described in the following part.

B. Optimization

The aim of the optimization is to adjust the synthesis filters so as to approach QPR, as specified by a maximum distortion, and a maximum of aliasing rejection. Thus we are looking for a way to obtain a transfer function G_{TF} close to 1 and to minimize the aliasing function G_{AF}. These two objectives are integrated into the single criterion

$$J(F_0, F_1) = (|G_{TF}(j\omega)| - 1)^2 + \beta|G_{AL}(j\omega)|^2$$

where β is a parameter that tunes the relative weight of the two terms. The most stringent requirement being aliasing rejection as illustrated in Table II, the largest weight is given to this term. In the case of guard band, the criterion is only applied on the band of interest.

It has yet been reported [10] that the mixed criterion above suffers of local minima, which turns the filter synthesis into a difficult, but key, task.

In order to find possible (optimum) synthesis, we have developed a heuristic approach that rests on the application of two minimizations strategies: a direct simplex search method that minimizes the average energy of the criterion with fast convergence, complemented by a minimax procedure whose particular goal is to lower the local maxima of the criterion especially on the edges of the band [10]. The algorithm also includes a perturbation strategy to avoid local minima. The overall algorithm is depicted in Fig. 2 and described below.

The algorithm focuses on the specification of maximum of aliasing rejection. It ends when the target is reached. It optimizes the coefficients of the numerators and denominators of the IIR digital filters.

Optimization functions — Specifically, the algorithm is implemented under Matlab, and uses the functions *fminsearch* and *fminimax*. *fminsearch* is a direct search method which is based on the Nelder-Mead method. The corresponding algorithm will find the minimum of a function of N variables. The function *fminimax* minimizes the worst-case (largest) value of a set of multivariable functions. This is generally referred to as the minimax problem. Both functions start at an initial estimate and may only give local solutions.

Initialization — Initial conditions for the synthesis filters are selected as follows. To fasten the process of optimization, we choose the synthesis filters optimized for a particular case of digital filter bank. Actually, we identify and use the discrete-time analog filters that correspond to the actual analog H_0 and H_1, the continuous-time filters. As we consider IIR filters, we have to stabilize the solutions given by the functions.

Perturbation strategy — As the functions may only give local solutions, a potential issue is to stall in a local minimum, before having reached the target. We first have to detect a possible local minimum. If two successive results of aliasing rejections have approximately the same value, we propose two ways to resolve it. On the one hand, we add a small deviation that should be carefully chosen, to get out of the local minimum. On the other hand, we increase the order of the IIR filters, and we compare the two solutions.

The algorithm is stopped when the targeted performance is reached. We could go further but prefer keeping the solution which provides an IIR with the smallest order.
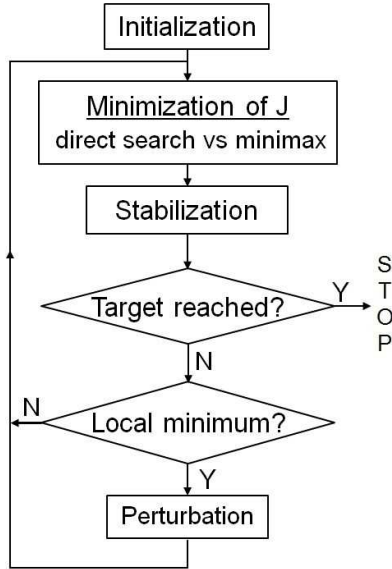

Figure 2.   Optimization algorithm

All our tests show that the procedure reaches the targeted performances and gives very interesting results in the case of perfectly known analog filters.

The following table gives an example of performances predicted by simulation in the case of two analysis filters chosen as analog 3rd-order Butterworth filters. As shown in table I, the IIR filters created are only 12th-order filters.

TABLE I.   PERFORMANCES WITH THEORETICAL ANALOG FILTERS

Max(G_{TF}) [dB]	Max(G_{AF}) [dB]	IIR order
0.03	-72.22	12

C. Realization and analog errors

Because of manufacturing spreads, the poles and zeros of realized analog filters differ from the theoretical ones. In addition, measurement errors can occur during the characterization of the analog filters. Since we do not have access to their exact transfer functions, the synthesis filters that correspond to the theoretical case do not exactly match and the performances are degraded. In order to quantify this effect, we introduce random errors on the coefficients of the ideal transfer functions and look at the performances. The percentages are relative to the ideal values of the coefficients. We choose the example from Table 1 as reference.

TABLE II.   PERFORMANCES WITH ACTUAL ANALOG FILTERS

Analog errors (%)	Max(G_{TF}) [dB]	Max(G_{AL}) [dB]
10	0.99	-15.86
1	0.09	-40.39
0.1	0.03	-56.79
0.01	0.03	-71.63

These results clearly highlight that this architecture is very sensitive to realization and analog errors. This is a known limitation which has already been reported in [11].

However, few practical HFB realizations have been reported in the literature. The next section details the measurements operated on a 2-channel HFB.

IV.   REALIZATION AND RESULTS

A system integrating two passive analog filters (3rd order Butterworth), two 150Msps 14-bit ADCs (AD9254) and an FPGA have been designed for an input spectrum in the band 30MHz-40MHz. The goal is to design a device with prescribed performances and then measure the actual performances of the realization.

A. Analog filters measurements

In order to obtain a good reconstruction, we need to determine as accurately as possible the transfer functions of the analog filters. They were measured through the ADCs in order to take into account every possible parasitic due to the acquisition card.
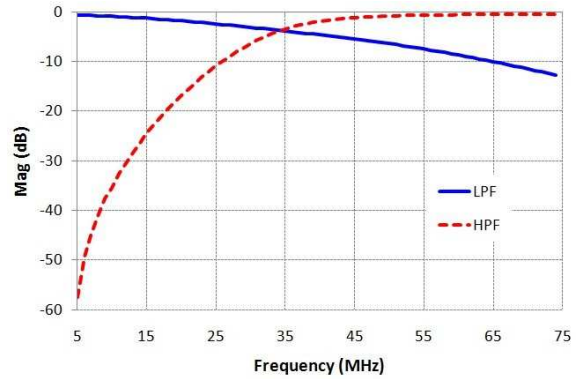

Figure 3.   Measurements of analog filters

Furthermore, in order to avoid aliasing, analog filters outputs were digitized at the maximum sampling rate of 150Msps. Measurements use both ADCs: on one path, the input signal was digitized, while on the 2nd path the output of one filter was digitized. This operation was repeated with the opposite configuration. As a result, transfer functions of the filters have been determined from 5MHz to 75MHz. The results are reported on Fig. 3.

B. Reconstruction

The input spectrum ranges from 30MHz to 40MHz. Thus, to get a satisfactory reconstruction on this bandwidth, we need the aliasing which falls in it to be attenuated by more than 70dB and the distortion between the digitized and analog input to be less than 0.5dB. The algorithm described in section III.B is applied. It performs an optimization of the coefficients of the digital synthesis filters associated to the measured transfer functions of the analog filters. After optimization, we get two stable 4th-order IIR filters.
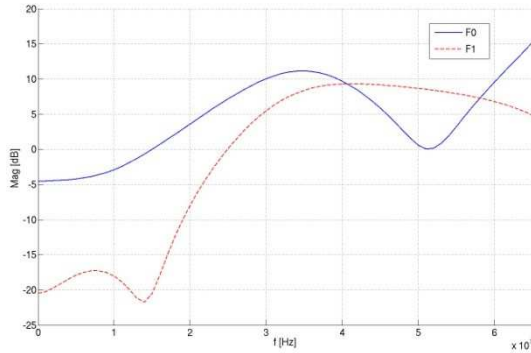
Figure 4. 4th-order IIR filters obtained after optimization

The following table gives the performances predicted after the optimization step, over the whole bandwidth:

TABLE III.   PERFORMANCES WITH MEASURED ANALOG FILTERS

Max(G_{TF}) [dB]	Max(G_{AF}) [dB]	IIR order
0.06	-72.83	4

C. Results

To illustrate with concrete figures the previous description of the measurements, we fed the analog filters with a sinus at 36MHz. Sampling at 75MHz, the aliasing occurs at 39MHz. As shown in Fig. 4, this aliasing is attenuated by 75.2dB.
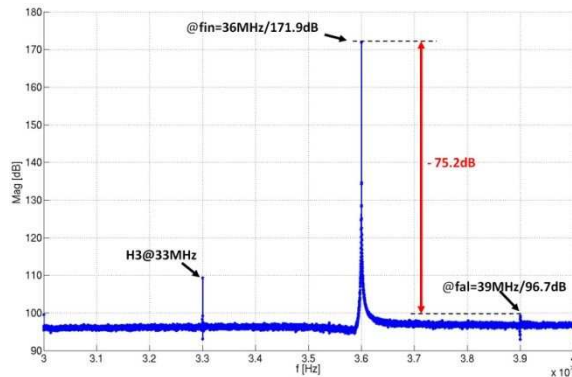

Figure 5. Module of FFT (dB) after reconstruction

The measurements have been done for several frequencies and the results are synthesized on Fig. 5, which compares the values predicted by simulation to the actual results on the device.
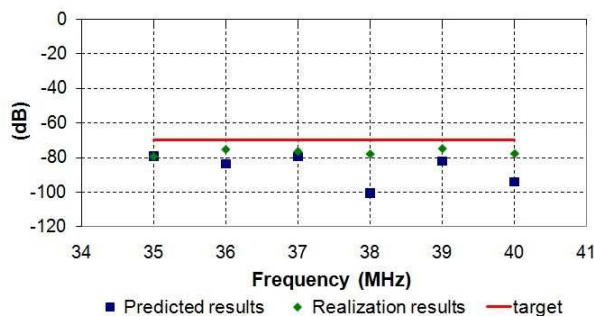

Figure 6. Synthesis of aliasing rejection results

The results are very interesting. However, if we repeat the measurements with the same configuration, we notice that the performances are degraded to between -45dB and -60dB. Hence, we observe that the target of -70dB is not fully reached; but still approached. The differences between the measured and predicted performances are due to measurements imprecision of the analog filters, their drift in temperature and the high sensitivity of the architecture to mismatches. On the other hand, we shall also mention that the level of performances is also dependent on the order of the analog analysis filters: the higher their order, the more aliasing rejection is obtained. There is also a trade-off between performances and complexity to tune at this point.

V.   CONCLUSION

In this paper we have presented an approach to build up an HFB-ADC based on low-order analog filters such as Butterworth or Elliptic filters for the analog analysis bank and on low-complexity digital IIR filters for the synthesis bank. We have designed the IIR filters of the synthesis bank using an optimization algorithm based upon both direct search and minimax. The results highlight that the proposed methods give interesting results for the optimization of the synthesis bank but confirm that the structure is very sensitive to measurement errors and that a security margin is necessary. Yet, the concept has been proven not only with simulations but also through a concrete hardware realization. We assume that reconstruction is scalable and could thus be applied to broader bandwidth for Cognitive Radio applications.

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