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Design of Complementary LDMOS in 0.35 μ m BiCMOS technology for Smart Integration

Mohamed Abouelatta-Ebrahim^{1,2}, Christian Gontrand¹ and Abdelhalim Zekry²

¹Université de Lyon; Institut des Nanotechnologies de Lyon INL-UMR5270,
CNRS, INSA de Lyon, Villeurbanne, F-69621, France

²Faculty of Engineering-Ain Shams University, Cairo, Egypt

Contact author:

Mohamed Abouelatta-Ebrahim

Address: Université de Lyon; Institut des Nanotechnologies de Lyon INL-UMR5270,
CNRS, INSA de Lyon, Villeurbanne, F-69621, France

Phone: (+33) (0)6 45 00 25 49

Fax : (+33) (0)4 72 43 60 81

E-mail: m.abouelatta@ieee.org

m.abouelatta@eng.asu.edu.eg

Affiliation of authors:

Mohamed Abouelatta-Ebrahim and Christian Gontrand

INSA Lyon - Institut des Nanotechnologies de Lyon
UMR CNRS 5270
Bât. Blaise Pascal, 6^{ème} étage
7, Avenue Jean Capelle
France - 69621 Villeurbanne Cedex

E-mail: m.abouelatta@eng.asu.edu.eg
Christian.Gontrand@insa-lyon.fr

Abdelhalim Zekry

Ain Shams University
Faculty of Engineering
Electronics Engineering Department
1, AlSarayat Street, Abbassia
11517, Cairo, Egypt

E-mail: aaazekry@hotmail.com

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Mohamed Abouelatta-Ebrahim^{1,2}, Christian Gontrand¹ and Abdelhalim Zekry²

¹Université de Lyon; Institut des Nanotechnologies de Lyon INL-UMR5270,
CNRS, INSA de Lyon, Villeurbanne, F-69621, France

²Faculty of Engineering-Ain Shams University, Cairo, Egypt
Phone : (+33) (0)6 45 00 25 49, Fax : (+33) (0)4 72 43 60 81

E-mail: m.abouelatta@eng.asu.edu.eg

Abstract

In this paper, an nLDMOS and a pLDMOS are developed by slight modifications of the base process steps of 0.35 μ m BiCMOS technology. Extra two masks are used for the formation of the body region and the drift region with slightly added thermal budget and without resorting to high-tilt implants. The specific ON-resistance ($R_{ON,SP}$) and the OFF-state breakdown voltage(BV) are 1.5 m Ω .cm² and 60V, for the nLDMOS and 3.0 m Ω .cm² and 160V, for the pLDMOS, so the devices can typically be operated around 42V supply voltage, which is suitable for the new automotive applications. An isolation mechanism, between the power devices is suggested using a deep trench filled with silicon dioxide and undoped polysilicon. The polysilicon has a nearly perfect conformal deposition, that is, both step coverage and bottom coverage are 100%. A simple subcircuit model is built using a two module approach, one for the intrinsic MOS area and the other for the drift region. The Spice model parameters of the intrinsic MOS part are extracted using a system that links the ICCAP extraction tool with the results of the ISE-TCAD tools. The simulation results using the Spice model are compared to the results provided by ISE-TCAD tools, and the accuracy at room temperature is less than 5% for the whole voltage domain. An interface circuit, to convert 0/3.3 V to 0/42 V, suitable for automotive applications, is proposed.

Keywords—cLDMOS; nLDMOS; pLDMOS; Deep Trench Isolation (DTI); 0.35 μ m BiCMOS; REduced SURface Field (RESURF); Smart power integrated circuit (SPIC; Automotive applications; Smart power; Breakdown voltage; Specific ON-resistance.

I. INTRODUCTION

Future 42V battery automotive applications, has driven the need for the smart power integrated circuit market in this voltage range. Smart power integrated circuit (SPIC) has high voltage devices integrated with low voltage circuitry on a single chip. Due to the reduction of external lines, components and inter-chip connections, SPIC can substantially decrease the system weight, size, and cost and makes the system more reliable [1-3].

One of the most popular high voltage structures that can be used to implement the SPIC is the Lateral DMOS (LDMOS). This structure is usually integrated with the standard components either with a dedicated process or BiCMOS/CMOS compatible schemes. The BiCMOS/CMOS compatible method is a more popular approach to implement the SPICs since it is simpler and more cost effective than a dedicated process.

Advancements were made enabling LDMOS power transistor to exhibit low ON-state resistance and high breakdown capability concurrently through a reduced surface field (RESURF) technology [4-8]. However, this RESURF technology can not be used in a BiCMOS process providing CMOS, vertical NPN transistor and power LDMOS transistor at the same time [9-13]. This is because vertical NPN transistor and RESURF LDMOS transistor require different epitaxial thicknesses according to their breakdown voltages. Hence, we had to use non- RESURF LDMOS transistor whose ON-state resistance is higher than RESURF LDMOS in a BiCMOS process. In this paper, we suggest a new RESURF-nLDMOS structure whose breakdown voltage is independent of epi thickness, and a pLDMOS structure implemented into the same epi thickness of the optimized nLDMOS. We apply the proposed cLDMOS structure to BiCMOS process that provides 3.3V CMOS.

The trench based processes have been integrated previously in CMOS architectures to suppress inter-well parasitics and CMOS thyristor latchup. This isolation scheme is used nowadays to reduce the isolation distance between power devices as well as between the power devices and low voltage circuitry and hence to reduce the total chip area drastically compared to technologies with a standard junction isolation scheme [14].

The modeling of the LDMOS structures came into play as these devices were integrated in standard technologies [15-18]. A simple subcircuit model for the entire device is built using a two module approach, one for the intrinsic MOS area and the other for the drift region. The intrinsic MOS area acts as a low voltage symmetrical device; hence it can be described by a Spice model. The model parameters are extracted using a system that links the ICCAP extraction tool with the results of the ISE-TCAD tools.

This paper is organized as follows: A quantitative description of the RESURF principle is presented in section II. Section III is devoted to the proposed devices structures, and the optimization of the device/process parameters is presented in sections IV and V. Section VI describes the ON-state characteristics. In section VII, the HV deep trench isolation technique is suggested and section VIII introduces the modeling of the devices. Section IX introduces an interface circuit and the last section presents our conclusions.

II. REDUCED SURFACE FIELD (RESURF) PRINCIPLE

The RESURF concept gives the best trade-off between the breakdown voltage and the ON-resistance of lateral devices. The technique provides the ability to form high-voltage lateral devices using an inherently low-voltage IC technology. RESURF-based technologies allowed for a more efficient interface between low-voltage/ low-power logic/analog signals and high-voltage/high-power output devices. As shown in fig. 1, the RESURF structure is constructed by a lateral P⁺/ N-epitaxial diode and a vertical P-substrate/ N-epitaxial diode.

The success of RESURF principle requires an optimization of key device/process parameters (see fig. 1): epi-layer doping concentration N_{epi} , epi-layer thickness T_{epi} , substrate doping concentration P_{sub} , and device structural geometry. The concept relies on reducing the lateral (surface) electric field of the P⁺/ N-epi diode, which represents the structure's weakest point for breakdown (most susceptible junction to high electric field) therefore enabling higher voltages to be applied .

A. Analysis of the RESURF principle

At any given applied reverse voltage V_{app} , the basic lateral RESURF structure shown in fig. 1 can be considered as a composite of two planar diodes.

Fig. 2 illustrates the depletion region/charge distribution when the lateral and vertical diodes are merged together. Notice the depletion charge/region shared by the two junctions. The charge (per unit vertical area) supported by this region is given by:

$$\Delta Q_{lat}(V_{app}) = q N_{epi} X_{lat} \eta \quad (1)$$

Where, $\eta(V_{app}) = X_{ver}(V_{app}) / T_{epi} \geq 0$

As a result of this charge contribution from the vertical diode, the “effective” charge supported by the lateral diode Q_{lateff} is lessened and is given by:

$$\begin{aligned} Q_{lateff}(V_{app}) &= Q_{lat}(V_{app}) - \Delta Q_{lat}(V_{app}) \\ &= [1 - \eta] Q_{lat}(V_{app}) \end{aligned} \quad (2)$$

The equivalent “effective” lateral field due to Q_{lateff} is given by:

$$\begin{aligned}
E_{lateff}(V_{app}) &= [1 - \eta] E_{lat}(V_{app}) \\
&= 2V_{app} \frac{[1 - \eta]}{X_{lat}(V_{app})} \\
&= \frac{2V_{app}}{X_{lateff}(V_{app})} \\
&= \frac{q N_{epieff} X_{lateff}(V_{app})}{\epsilon_s}
\end{aligned} \tag{3}$$

Where,

$$X_{lateff}(V_{app}) = \frac{X_{lat}(V_{app})}{[1 - \eta]} \tag{4}$$

$$N_{epieff}(V_{app}) = N_{epi} [1 - \eta]^2 \tag{5}$$

The equations (3-5) completely demonstrate the RESURF mechanism, and quantitatively show the field reshaping/reduction effects. With the presence of the vertical P-sub/N-epi diode and the interaction of its space-charge region with the lateral space-charge region, the lateral depletion width spans a larger distance X_{lateff} compared to the case without the presence of the vertical diode. Accordingly, the lateral electric field at the P⁺/N-epi junction E_{lateff} gets much reduced, therefore enabling higher voltages to be applied (see fig. 3).

From equations (3-5), η (through its dependence on N_{epi} , P_{sub} , and T_{epi}) is a measure of the RESURF'ing efficiency and is critical for sensitivity analysis calculations.

B. Optimal RESURF'ing condition ($\eta = 1$).

In this situation, the epi-layer is fully depleted by the vertical junction (see fig. 4). As a result, $E_{lateff} \rightarrow 0$, $N_{epieff} \rightarrow 0$, $BV_{lat} \rightarrow \infty$, and $BV_{resurf} \rightarrow BV_{ver}$.

Since the breakdown of the structure is defined entirely by the vertical junction, this situation defines the optimal RESURF condition for operation.

Actually, once the epi-region is fully depleted, it behaves as a very low-doped (very high-resistivity) layer which for simplicity can be approximated by an intrinsic layer.

Because of the low doping intrinsic behaviour of the epi-layer, BV_{lat} is now limited only by the drift length L_{Drift} and is given by:

$$BV_{lat} = E_{clat} \times L_{Drift} \tag{6}$$

III. LDMOS STRUCTURES

A. The nLDMOS Transistor

The structure of the proposed nLDMOS is shown in fig. 5a. The same standard 0.35 μm BiCMOS technological steps are used with two extra masks. One mask for the Pwell formation and the other for low thermal budget LB-Pwell (body-region) using the smallest possible thermal budget to not affect the characteristics of the low voltage CMOS parts. In this structure, the effective channel length L_{CH} is defined by the difference in the lateral diffusions of the P-body region and the N^+ source region. L_{Drift} and T_{Drift} are the length and the thickness of the drift region, respectively. L_S and T_{pwell} are the space length and the thickness of the Pwell region, respectively.

The modifications to the standard process are as follows as shown in fig. 5b:

After the buried layer alignment is finished, an N- epitaxial layer is deposited (EPITAXY1), then, the Pwell is implanted with dose= $3E13 \text{ cm}^{-2}$ and implantation energy = 240 keV. A short drive-in is performed (25min) at 1150 $^{\circ}\text{C}$.

A second N-epitaxial layer is deposited (EPITAXY2), then the whole structure is derived-in for (35min) at 1150 $^{\circ}\text{C}$. The summation of the drive-in times for all the processes (buried layer+ epitaxial layers+ Pwell) is the same as the time taken to drive-in the buried layer and the CMOS retrograde wells in the standard process. So, no extra thermal budget is needed until now.

After the LOCOS, a high energy LB-Pwell is implanted to form the body region of the nLDMOS transistor. A very short drive-in time is taken (8min) at 1150 $^{\circ}\text{C}$, to not alter the low voltage devices characteristics.

Using these process steps and the DIOS process simulator, the 2D cross-section of the device with the doping concentration distribution is shown in fig. 5c.

B. The pLDMOS Transistor

The structure of the pLDMOS is shown in fig. 6a. In this structure, two extra masks are used, one for the P_{Drift} formation and the other for Nbody region using small thermal budget.

The modifications to the standard process are as follows as shown in fig. 6b:

After the alignment of the buried layer, the deposition of the two steps N- epitaxial layer, and the fabrication of the CMOS retrograde wells, then the P_{Drift} is implanted with dose= $8E12 \text{ cm}^{-2}$ and implantation energy = 200 keV. A short drive-in is performed (10min) at 1150 °C.

After the LOCOS, a high energy Nwell is implanted to form the body region of the pLDMOS transistor. A short drive-in time is taken (10min) at 1150 °C, to not alter the low voltage devices characteristics.

Using these process steps and the DIOS process simulator, the 2D cross-section of the device with the doping concentration distribution is shown in fig. 6c.

IV. NLD MOS PARAMETERIC ANALYSIS

There are many parameters that should be optimized to achieve the required characteristics. The drift region thickness T_{Drift} , and length L_{Drift} had to be optimized to reduce the specific ON-resistance and the surface electric field by using the RESURF principle. The Pwell spacing L_S , thickness T_{Pwell} , and doping concentration P_{well} are optimized to achieve the best trade off among the electrical parameters of the device. These parameters are optimized by using the DESSIS device simulator.

A. Impact of Drift Thickness (T_{Drift})

It is noticed from fig. 7 that the breakdown voltage is slightly changed with the drift thickness, which confirms that the breakdown is not a function of T_{Drift} . The breakdown voltage depends only on the Pwell/N-buried metallurgical junction properties. This result is on contrary to the conventional RESURF LDMOSFETs, which have breakdown voltages function of the drift region thicknesses. This dependency limits the integration of these devices with low voltage CMOS devices that use thin epi-layers as in the BiCMOS technology. Also, It is clear that $R_{ON,SP}$ is inversely proportional to T_{Drift} .

The drift region thickness affects the distribution of the surface electric field as shown in fig. 8. According to the RESURF principle, the surface electric field distribution is a function of the drift dose, hence the drift thickness must be optimized to get best trade-off between the specific ON-resistance and surface electric field. Obviously, the minimum and more flat surface electric field is achieved at $T_{Drift} = T_{Drift,opt} = 1.1 \mu\text{m}$.

It is clear from fig. 9 that the potential lines are crowded in the Pwell/N-buried junction, far from the device surface. This minimizes the hot carrier effect and improves the ruggedness of the device and consequently, increases the corresponding safe operating area.

B. Impact of Pwell Spacing Length (L_S)

The maximum breakdown voltage is achieved in case of absence of the Pwell spacing (i.e. $L_S = 0.0$) as shown in fig. 10. In this case the avalanche breakdown occurs at the drain side due to punch-through phenomenon and the breakdown voltage is a function of the drift region thickness, the drain-junction curvature, and the Pwell/N-buried metallurgical junction properties.

For $L_S > 0.0 \mu\text{m}$, the breakdown voltage almost constant. The specific ON-resistance slightly decreases with increasing the spacing length; this is due to increasing the effective cross-section area of the drain current path. The surface electric field distributions for $L_S = 0.0$ and $L_S = 1.65 \mu\text{m}$ are shown in fig. 11. It is noticed that the electric field increases sharply at the drain side in case of absence of the Pwell spacing.

C. Impact of Drift Length (L_{Drift})

In fig. 12, the breakdown voltage and the specific ON-resistance are drawn as a function of the drift length (L_{Drift}). The breakdown voltage slightly decreases with increasing the drift length. This slight decrease is due to changing the Pwell/N-buried metallurgical junction properties with changing the device drift length. Also, it is clear from the figure that, increasing the drift length increases the specific ON-resistance.

D. Impact of Pwell Doping Concentration (P_{well})

The breakdown voltage and the specific ON-resistance of the nLDMOS structure for different Pwell doping concentrations P_{well} are shown in fig. 13. The BV is decreased with increasing P_{well} , as the breakdown voltage is inversely proportional to the doping concentration. $R_{ON,SP}$ is not independent on P_{well} , as it depends mainly on the drift region properties.

V. PLDMOS PARAMETERIC ANALYSIS

A. Impact of Drift Thickness (T_{Drift})

The impact of the drift thickness is illustrated in fig. 14. It is obvious that the breakdown voltage and the specific ON-resistance is a strong function of the drift thickness. The breakdown voltage obeys the RESURF principle and it has the maximum value at the drift thickness that gives the optimum drift dose.

The drift region thickness affects the distribution of the surface electric field as shown in fig. 15. According to the RESURF principle, the surface electric field distribution is a function of the drift dose, so, the drift thickness must be optimized to obtain the best trade-off among the breakdown voltage, the specific ON-resistance and the surface electric field.

It is obvious that at $T_{Drift} = 0.65\mu\text{m}$, the optimum RESURF'ing condition is achieved, above this value, the drift dose is increased and the maximum surface electric field is at the gate side (under RESURF'ing condition). The potential distribution of the LDMOS at breakdown optimum case is shown in fig. 16.

B. Impact of Drift Length (L_{Drift})

In fig. 17, the breakdown voltage and specific ON-resistance are drawn as a function of the drift length (L_{Drift}). The breakdown voltage is decreased with decreasing the drift length due to punch-through effect according the RESURF principle and the specific ON-resistance is decreased with the increase in the drift length.

C. Impact of Pdrift Doping Concentration (P_{Drift})

The breakdown voltages (BV) and the specific ON-resistances ($R_{ON,SP}$) of the pLDMOS structure for different P_{Drift} are shown in fig. 18. The breakdown voltage increases with increasing the drift doping concentration until $P_{Drift} = 6.0\text{E}+16 \text{ cm}^{-3}$, then it rests constant until $P_{Drift} = 9.0\text{E}+16 \text{ cm}^{-3}$. The optimum RESURF'ing condition that gives the maximum breakdown voltage is achieved for $6.0\text{E}+16 \text{ cm}^{-3} > P_{Drift} > 6.0\text{E}+16 \text{ cm}^{-3}$. It is also clear from the figure that, the specific ON-resistances ($R_{ON,SP}$) decreases with increasing the doping concentration.

VI. THE ON-STATE CHARACTERISTICS

A. The nLDMOS Transistor Characteristics

The $I_{DS}-V_{DS}$ characteristics have a parabolic dependence of V_{GS} and with maximum drain current of $0.42 \text{ mA}/\mu\text{m}$ at $V_{GS} = 3.3\text{V}$. The threshold voltage for the proposed device is about 0.6V , which is matched with the threshold voltage of the low voltage nMOSFET.

B. The pLDMOS Transistor Characteristics

The $I_{DS}-V_{DS}$ characteristics have a parabolic dependence on V_{GS} and with maximum drain current of $0.135 \text{ mA}/\mu\text{m}$ at $V_{GS} = -3.3\text{V}$. The threshold voltage for the proposed device is about -0.55V .

VII. HV DEEP TRENCH ISOLATION

In fig. 19, a cross-section of an nLDMOS and pLDMOS devices isolated with deep trench isolation (DTI) are shown, which constructs a complementary LDMOS (cLDMOS). A high quality thermal oxide liner is grown along the side-walls of the deep trench. A polysilicon stress-relief layer is deposited so that it fills the deep trench and is recessed below the silicon surface. The polysilicon has a nearly perfect conformal deposition, that is, both step coverage and bottom coverage are 100%.

A. OFF-state Performance

Leakage current levels of nLDMOS and pLDMOS are very low with deep trench isolation and are not different from junction leakage without deep trench, indicating that there is no additional leakage due to deep trench presence as illustrated in fig. 20a and 20b. The deep trench oxide thickness is sufficient to sustain a breakdown voltage from N-epi to substrate of more than 300V, which is greater than the OFF-state breakdown voltage of both devices.

As shown in fig. 20 the leakage currents for nLDMOS and pLDMOS are in the order of $1.0\text{E-}14$ A and $1.0\text{E-}19$ A, respectively. These values of leakage currents are very small compared to the values of the drain currents.

B. ON-state Performance

The ON-state characteristics are not changed with the use of the deep trench isolation. The ON-state characteristics of both nLDMOS and pLDMOS at $|V_{GS}| = 3$ V, are shown in fig. 21a and 21b.

VIII. LDMOS MODELING

The model for the entire device is built using a two modules approach, one for the intrinsic MOS area and the other for the drift region.

A. The Drift Resistance R_{Drift}

An analytical expression for the drift resistance is given by:

$$R_{drift} = \left[\frac{L_{dr}}{q\mu_n N_{dr} W Z_{dr}} + \frac{(V_D - V_K)}{2qN_{dr} W Z_{dr} v_{sat}} \right] / (1 + \theta_{acc} V_G) \quad (7)$$

Where, L_{dr} and Z_{dr} are the length and the width of the quasi-neutral drift region, respectively, and N_{dr} is the drift region doping concentration. W is the device width and v_{sat} is the saturation velocity. θ_{acc} is a fitting parameter that defines the transverse-field dependence in the accumulation region.

R_{Drift} is plotted at $V_{GS} = 2$ V, as a function of V_{DS} and V_K in fig. 22. As V_{GS} increases, the accumulation resistance decreases and hence the total drift resistance decreases. As the drift resistance is the dominant part of the device ON-resistance, so an average value for R_{ON} can be estimated from fig. 22, which is the value of R_{drift} for nLDMOS at $V_{DS} \rightarrow 0$, ($R_{ON} \approx 21$ k Ω at $V_{GS} = 2$ V).

B. Implementation of the Model into Spice

Approximate subcircuit model of nLDMOS is illustrated in fig. 23 with LEVEL 3 MOS Spice model is used to implement the intrinsic MOS part of LDMOS. ICCAP extraction tool is used to extract the Spice model parameters by using the results of the TCAD simulations as the input to these

tools (as measured data). Then the value of the Spice parameter RD is modified to take the effect of the drift resistance into consideration.

The pLDMOS can also be described by similar subcircuit model. The simulation results using the Spice model are compared to the results provided by ISE-TCAD tools, and the accuracy at room temperature is less than 5% for the whole voltage domain as shown in fig. 24 and 25.

IX. AN INTERFACE CIRCUIT

The aim of the interface circuit is the conversion of 0/3.3 V low logic voltage to 0/42 V high level voltage. We must check that the voltage across each transistor must be smaller than its breakdown voltage.

The circuit schematic is shown in fig. 26. M9 and M10 constitute our proposed cLDMOS. Transistors M3 to M8 constitute level shift circuit, causes V_G of M9 to be $(V_{DDH}-V_{DDL})/V_{DDH}$ but V_G of M10 is $0/V_{DDL}$. M1 and M2 is a CMOS inverter. The input and output waveforms are shown in fig. 27.

X. CONCLUSION

In this paper, we suggest a RESURF cLDMOS structure and apply this structure to the 0.35 μ m BiCMOS process that provides 3.3V CMOS. $R_{ON,SP}$ and BV are 1.5 m Ω .cm² and 60V, for the nLDMOS and 3.0 m Ω .cm² and 160V, for the pLDMOS. The devices can typically be operated around 42V supply voltage, which is suitable for the future automotive applications. An isolation mechanism, between the power devices is suggested using a deep trench filled with silicon dioxide and undoped polysilicon. The polysilicon has a nearly perfect conformal deposition, that is, both step coverage and bottom coverage are 100%. Also, a simple subcircuit model for the entire device is built using a low voltage intrinsic MOSFET and a voltage dependent resistor. The Spice model parameters of the intrinsic MOS part are extracted using a system that links the ICCAP extraction tool with the results of the ISE-TCAD tools and the Spice parameter RD is modified to account the drift region effect. An interface circuit to convert the low logic levels to high voltage levels is proposed.

REFERENCES

- [1] B. Murari, F. Bertotti, G. A. Vignola, "Smart Power ICs," Berlin, Springer, 1996.
- [2] B.J. Baliga, "The future of power semiconductor device technology," *Proceedings of the IEEE*, vol. 89, no. 6, pp. 822 – 832, 2001.
- [3] B. J. Baliga, "Fundamentals Of Power Semiconductor Devices", Springer Verlag, Dec. 2008.
- [4] Z. Sun, W. Sun, L. Shi, "A review of safe operation area," *Micro. J.*, vol.37, pp.661-667, 2006.
- [5] P. Moens, G.bosch, "Characterization of Total Safe Operating Area of Lateral DMOS Transistors," *IEEE Trans. Dev. and Mat. Reliability*, vol. 6, no. 3, pp. 349–357, Sep. 2006.
- [6] M. Imam, M. Quddus, J. Adams, and Z. Hossain, "Efficacy of Charge Sharing in Reshaping the Surface Electric Field in High-Voltage Lateral RESURF Devices," *IEEE Trans. Elec. Dev.*, vol. 51, no.1, pp. 141–148, Jan. 2004.
- [7] A. Parpia and C. A. T. Salama, "Optimization of RESURF LDMOS Transistors: an Analytical Approach," *IEEE Trans. Elec. Dev.*, vol. 37, no. 3, pp. 789-796, 1990.
- [8] S.Y. Han, H.W. Kim, S.K. Chung, "Surface field distribution and breakdown voltage of RESURF LDMOSFETs," *Micro. J.*, vol.31, no.8, 2000.
- [9] T.Terashima, F.Yamamoto, K.Hatasako, S.Hine, "120 V BiC DMOS process for the latest automotive and display applications," *IEEE Proc. ISPSD*, pp. 93 – 96, 2002.
- [10] T.H. Kwon, Y.S. Jeoung, S.K. Lee, Y.C. Choi, et al., "Newly designed isolated RESURF LDMOS transistor for 60 V BCD process provides 20 V vertical NPN transistor," *Proc. Dev. Research Conf. DRC*, pp. 67- 68, 2002.
- [11] V. Parthasarathy, R.Zhu, M.L.Ger, V.Khemka, A.Bose, et al., "A 0.35 μm CMOS based smart power technology for 7V-50V applications," *IEEE Proc. ISPSD*, pp.317-320,2000.
- [12] T.R.Efland, "Integration of power devices in advanced mixed signal analog BiCMOS technology," *Micro. J.*, vol.32, no. 5-6, pp.409-418, 2001.
- [13] P.M. Santos, V. Costa, MC Gomes, B. Borges, M. Lança, "High-voltage LDMOS transistors fully compatible with a deep-submicron 0.35 μm CMOS process," *Micro. J.*, vol. 38, no. 1, pp. 35-40, 2007.
- [14] F. De Pestel, P. Coppens, H. De Vleeschouwer, et al., " Deep Trench Isolation for a 50V 0.35 μm Based Smart Power Technology", *IEEE Proc. ESSDERC*, pp. 191 – 194, 2003.
- [15] R. Kraus, H. Mattausch, "Status and Trends of Power Semiconductor Device Models for Circuit Simulation," *IEEE Trans. Power Electronics*, vol. 13, no. 3, May 1998.
- [16] C.W.Tang, K.Y.Tong, "A compact large signal model of LDMOS," *Solid-State Electronics*, vol.46, no.12, pp. 2111-2115, 2002. http://www.ingentaconnect.com/content/els/00381101/2002/00000046/00000012/art00238 - aff_1
- [17] L. Starzak, M. Zubert, A. Napieralski, "The new approach to the power semiconductor devices modelling," *Proc. MSM*, vol.1, pp.640 – 644, 2002.
- [18] P. Moens, D. Bolognesi, L. Delobel, D. Villanueva, et al., "Future trends in intelligent interface technologies for 42 V battery automotive applications," *IEEE Proc. ESSDERC*, pp. 287-290, 2002.

FIGURE CAPTIONS

- Fig.1 Cross-section of a lateral RESURF structure
- Fig.2 The resulting space-charge sharing when the lateral and vertical diodes are merged together
- Fig.3 Illustration of the lateral electric field reshaping for the structure in figure 1 The electric field reduction due to the lower N_{epieff} value
- Fig.4 $\eta = 1$, optimal RESURF'ing condition
- Fig.5a The structure of nLDMOS
- Fig.5b The process steps of nLDMOS in 0.35 μm BiCMOS technology
- Fig.5c 2D cross-section of nLDMOS
- Fig.6a The structure of pLDMOS
- Fig.6b The process steps of pLDMOS in 0.35 μm BiCMOS technology
- Fig.6c 2D cross-section of pLDMOS
- Fig.7 BV and $R_{ON,SP}$ for different T_{Drift} at $L_{Drift}=7.5\mu\text{m}$, $T_{Pwell}=1.7\mu\text{m}$, $L_S=1.65\mu\text{m}$
- Fig.8 Electric field distribution at breakdown for various drift thicknesses at $L_{Drift}=7.5\mu\text{m}$, $T_{Pwell}=1.7\mu\text{m}$, $L_S=1.65\mu\text{m}$
- Fig.9 Potential distribution at the breakdown for $T_{Drift} = 1.1\mu\text{m}$, at $L_{Drift} = 7.5\mu\text{m}$, $T_{Pwell}=1.7\mu\text{m}$, $L_S=1.65\mu\text{m}$
- Fig.10 BV and $R_{ON,SP}$ for different L_S at $L_{Drift}=7.5\mu\text{m}$, $T_{Pwell}=1.7\mu\text{m}$, $T_{Drift}=1.1\mu\text{m}$
- Fig.11 Electric field distribution at breakdown for various L_S at $L_{Drift}=7.5\mu\text{m}$, $T_{Pwell}=1.7\mu\text{m}$, $T_{Drift}=1.1\mu\text{m}$
- Fig.12 BV and $R_{ON,SP}$ for different L_{Drift} at $L_S=1.65\mu\text{m}$, $T_{Pwell}=1.7\mu\text{m}$, $T_{Drift}=1.1\mu\text{m}$
- Fig.13 BV and $R_{ON,SP}$ for different P_{well} at $L_S=1.65\mu\text{m}$, $L_{Drift}=7.5\mu\text{m}$, $T_{Drift}=1.1\mu\text{m}$
- Fig.14 BV and $R_{ON,SP}$ for different T_{Drift} at $L_{Drift}=7.5\mu\text{m}$
- Fig.15 Electric field distribution at breakdown for various drift thicknesses at $L_{Drift}=7.5\mu\text{m}$
- Fig.16 Potential distribution at the breakdown for $T_{Drift}=0.65\mu\text{m}$ at $L_{Drift}=7.5\mu\text{m}$
- Fig.17 BV and $R_{ON,SP}$ for different L_{Drift} at $T_{Drift}=0.65\mu\text{m}$
- Fig.18 BV and $R_{ON,SP}$ for different P_{Drift} at $T_{Drift}=1.1\mu\text{m}$, and $L_{Drift}=7.5\mu\text{m}$
- Fig.19 The structure of cLDMOS with deep trench isolation
- Fig.20 The drain and bulk currents for (a) nLDMOS, and (b) pLDMOS, without trench isolation (dashed curves), and with trench isolation (solid curves)
- Fig.21 The drain currents for (a) nLDMOS, and (b) pLDMOS, at $|V_{GS}| = 3\text{ V}$, without trench isolation (dashed curve), and with trench isolation (solid curve)

Fig.22 R_{drift} as a function of V_{DS} and V_K at $V_{GS}=2V$

Fig.23 Approximate subcircuit model of nLDMOS

Fig.24 Comparison of the TCAD simulation (Black solid curves) and the PSpice model simulation (Red dashed curves) for nLDMOS

Fig.25 Comparison of the TCAD simulation (Black solid curves) and the PSpice model simulation (Red dashed curves) for pLDMOS

Fig.26 The circuit schematic of the interface circuit

Fig.27 The input and output waveforms of the interface circuit

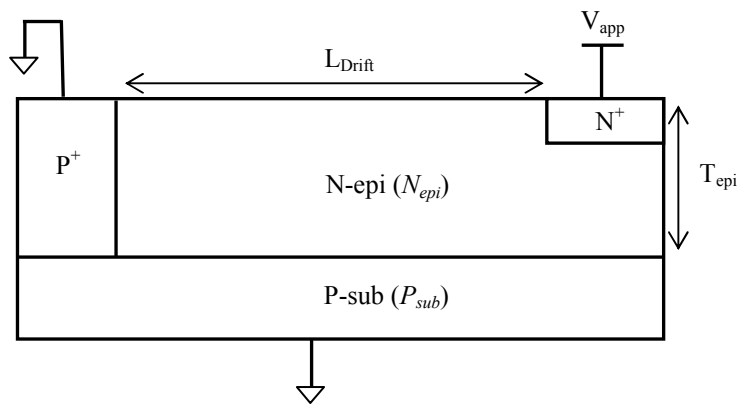


Fig. 1

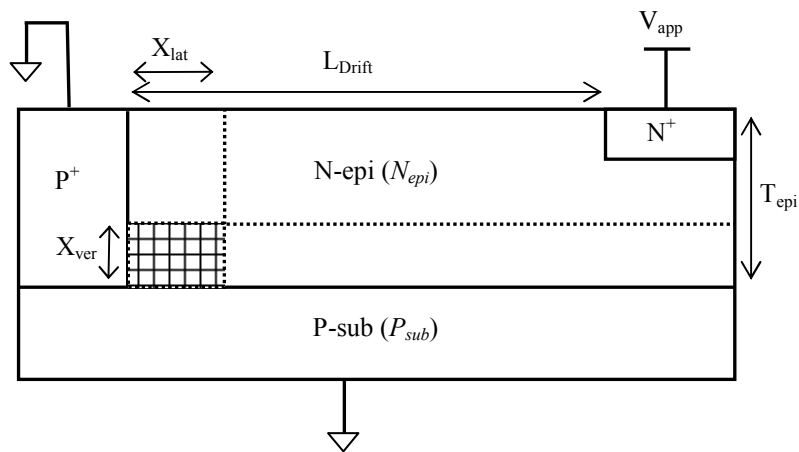


Fig. 2

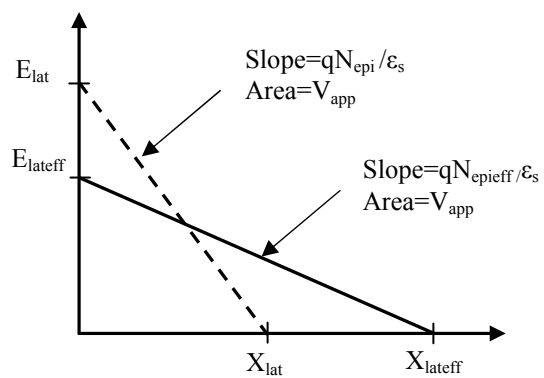


Fig. 3

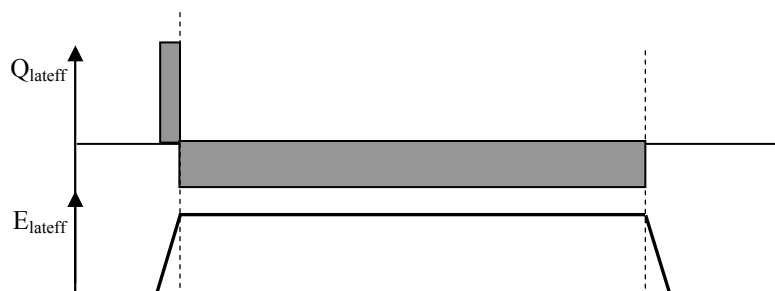


Fig. 4

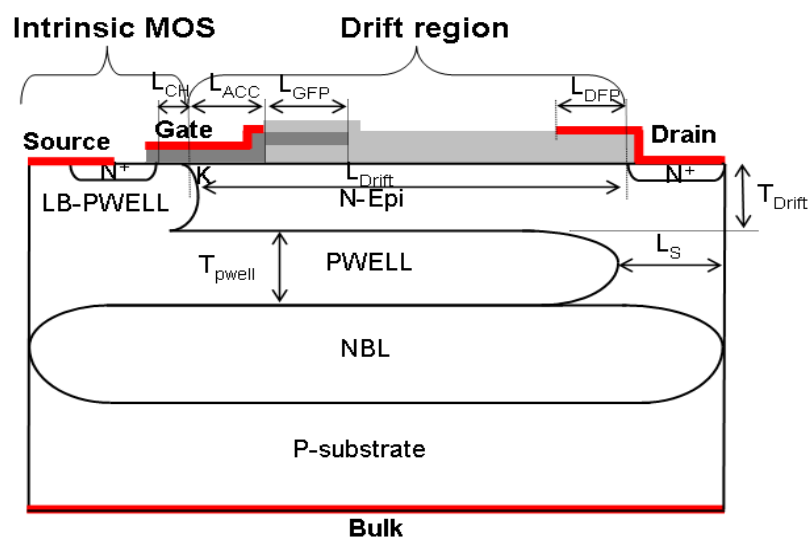


Fig. 5a

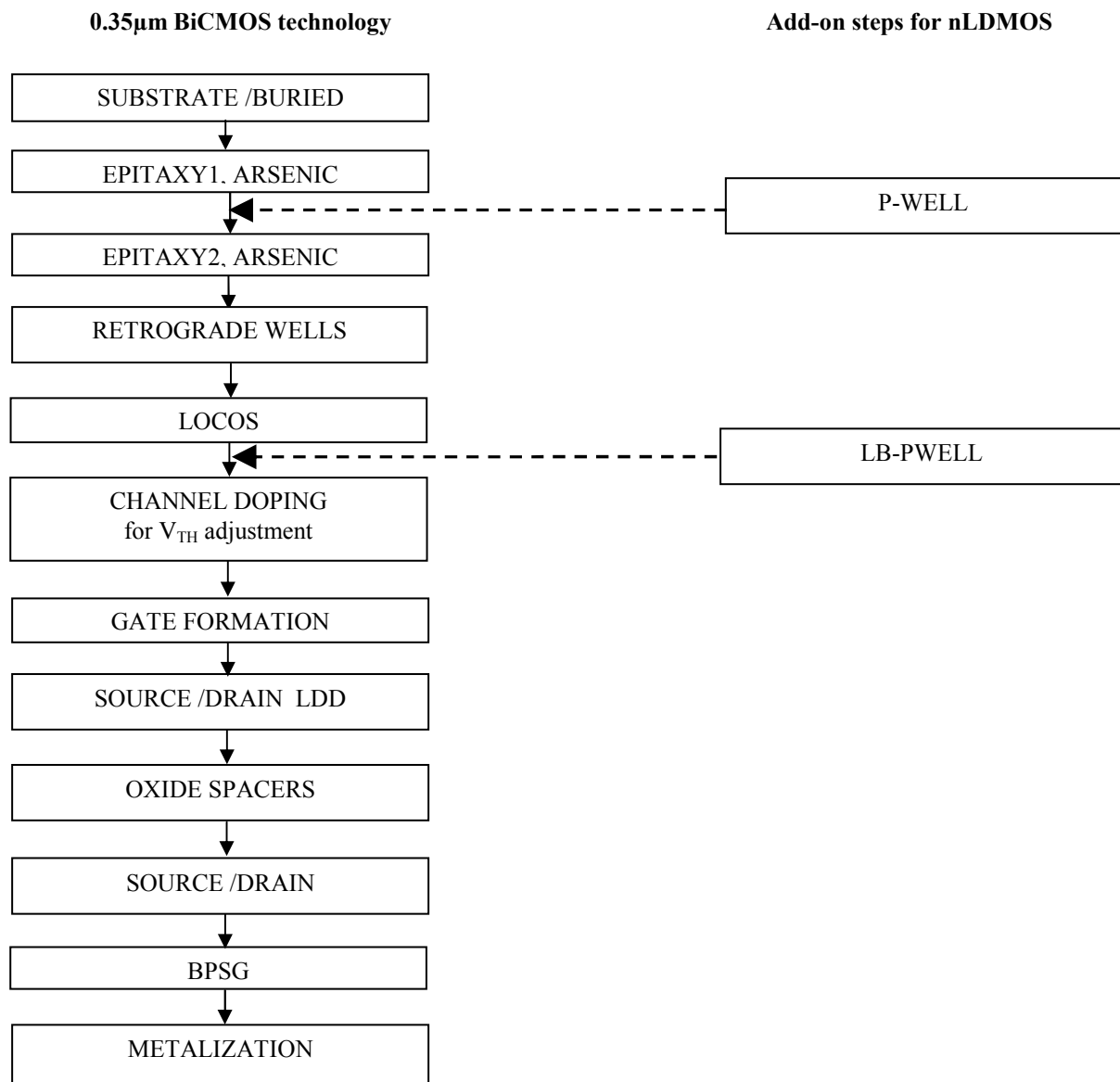


Fig. 5b

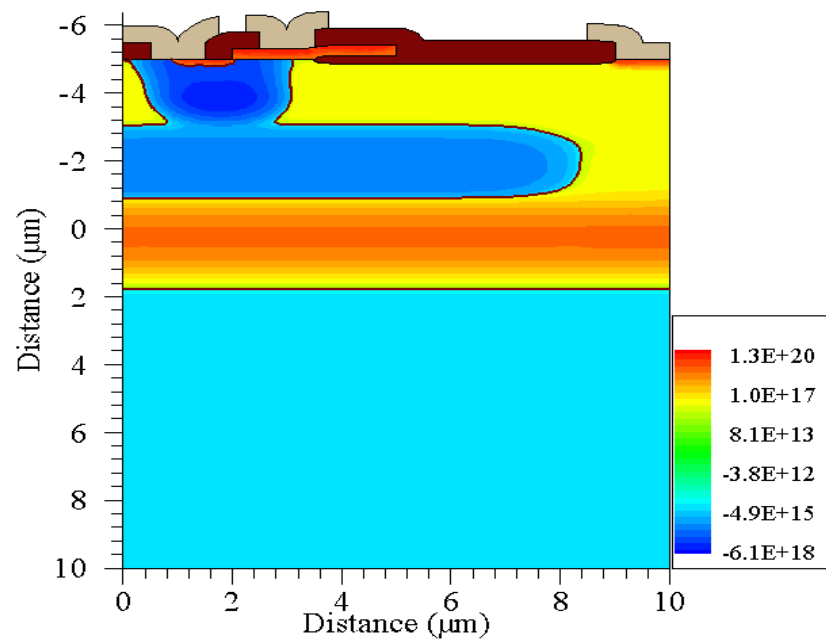


Fig. 5c

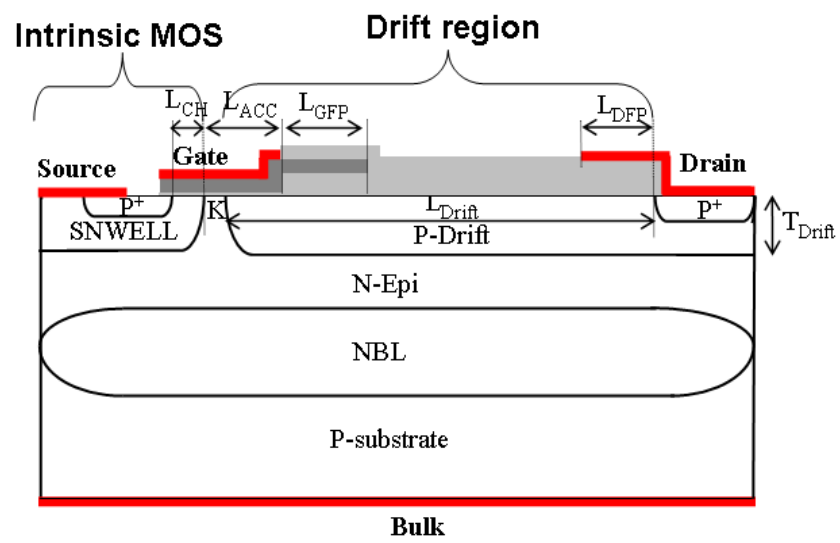


Fig. 6a

0.35μm BiCMOS technology

Add-on steps for pLDMOS

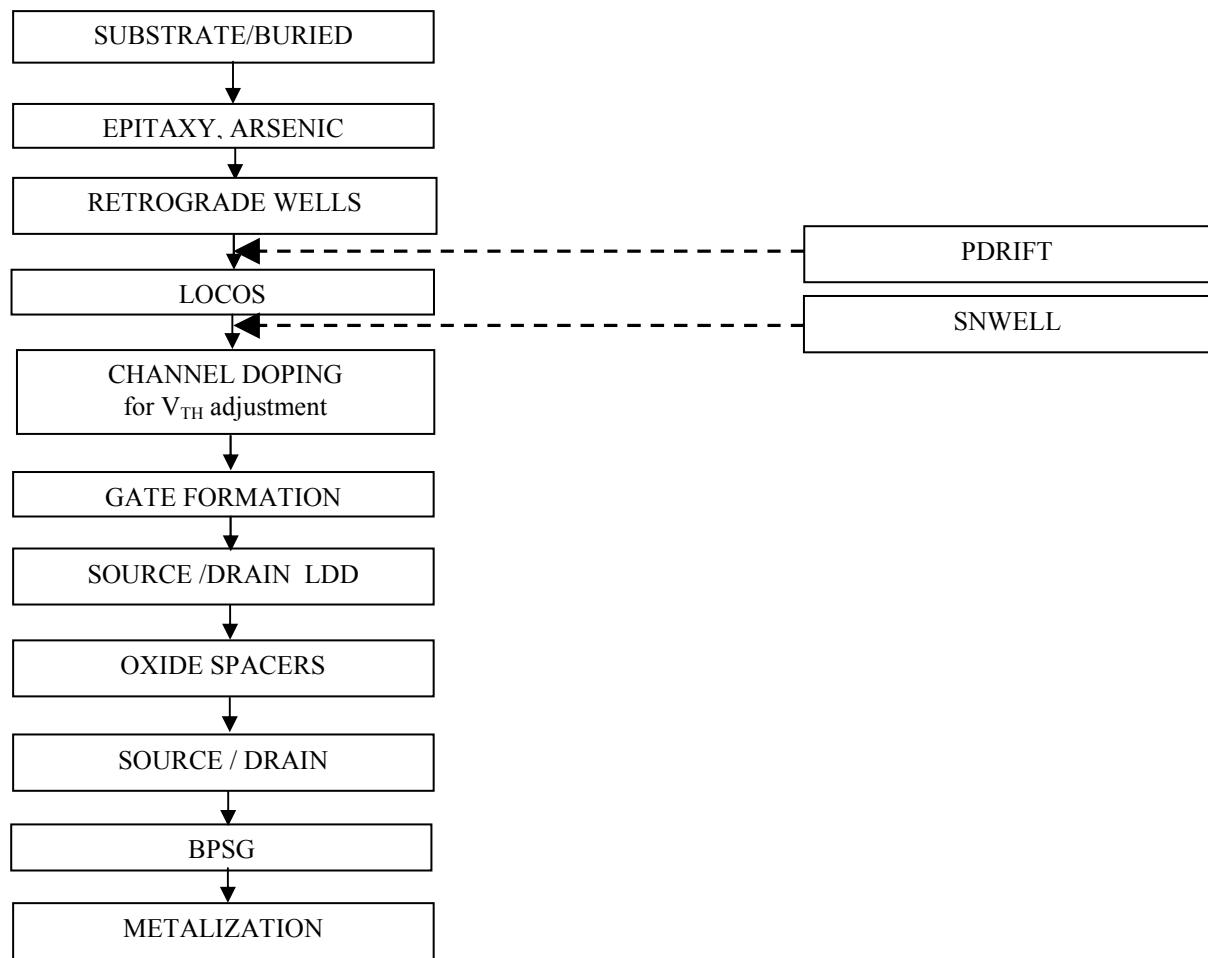


Fig. 6b

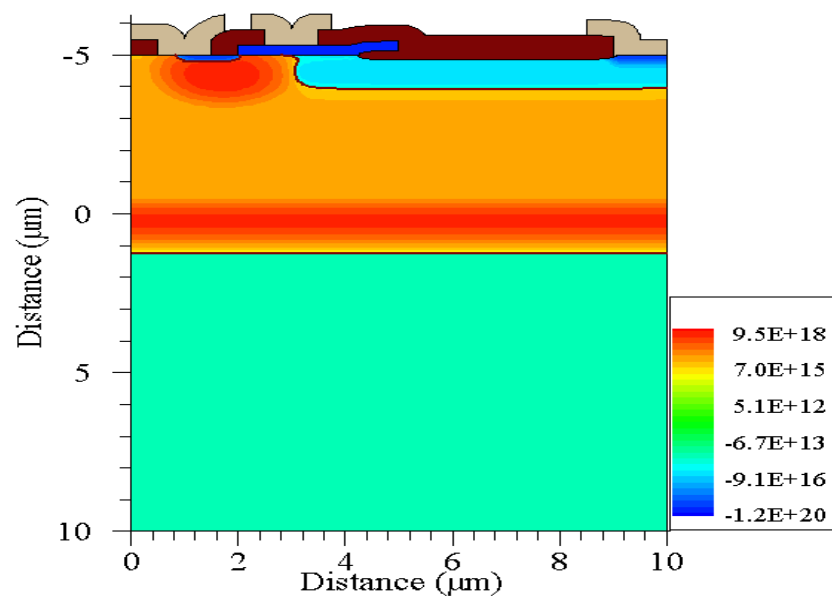


Fig. 6c

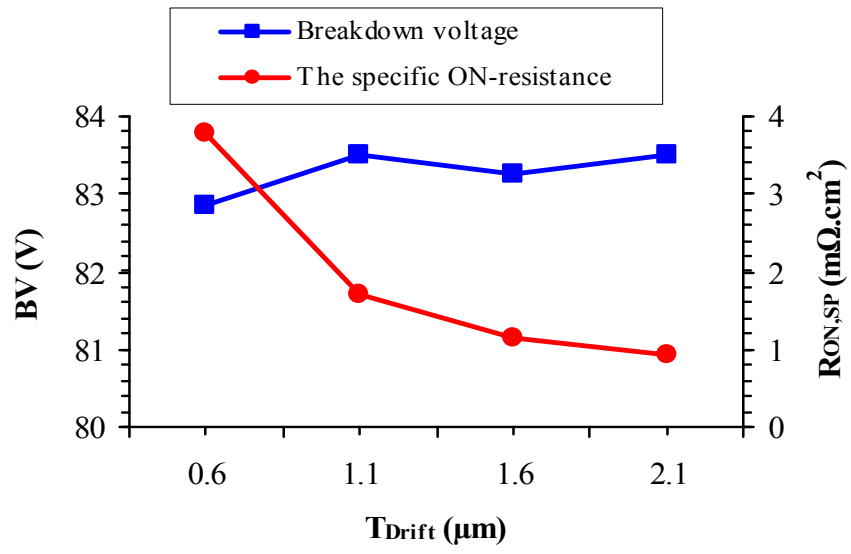


Fig. 7

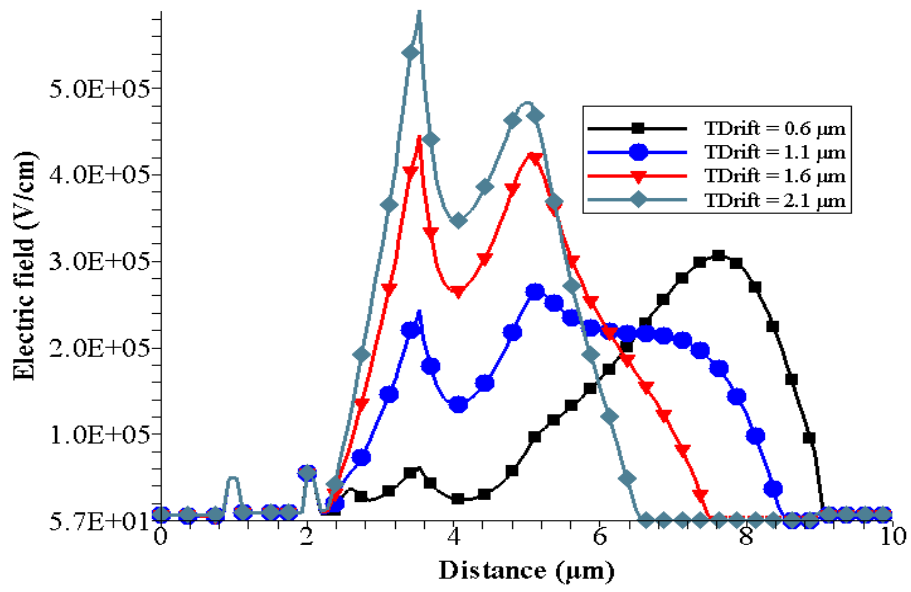


Fig. 8

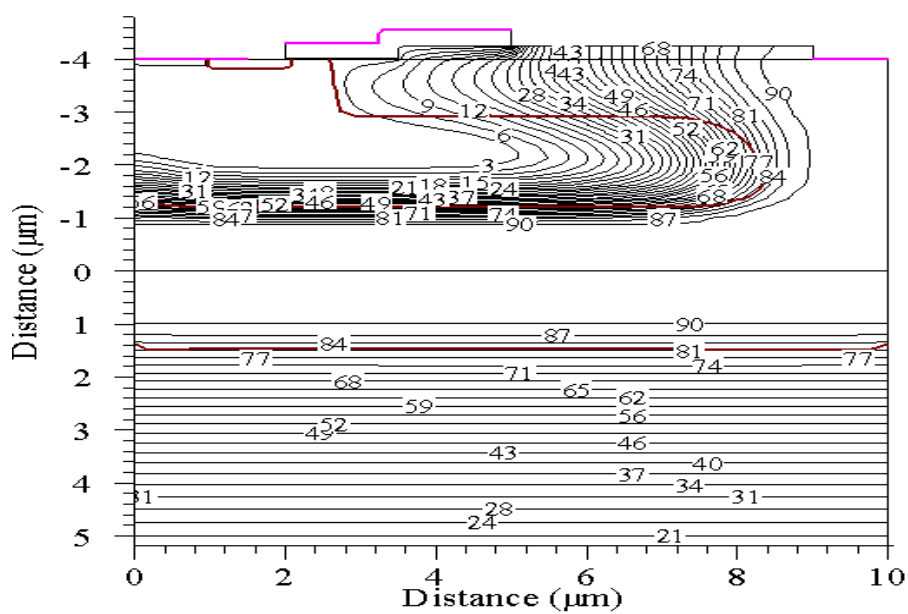


Fig. 9

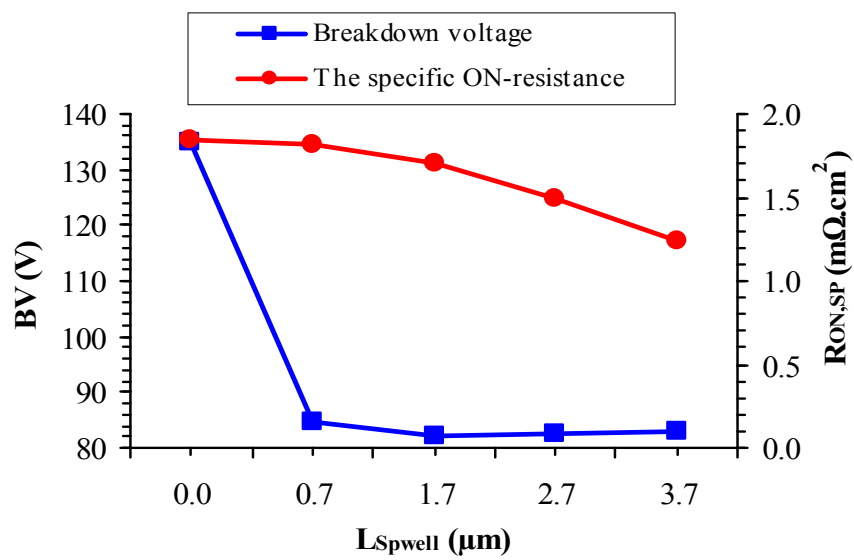


Fig. 10

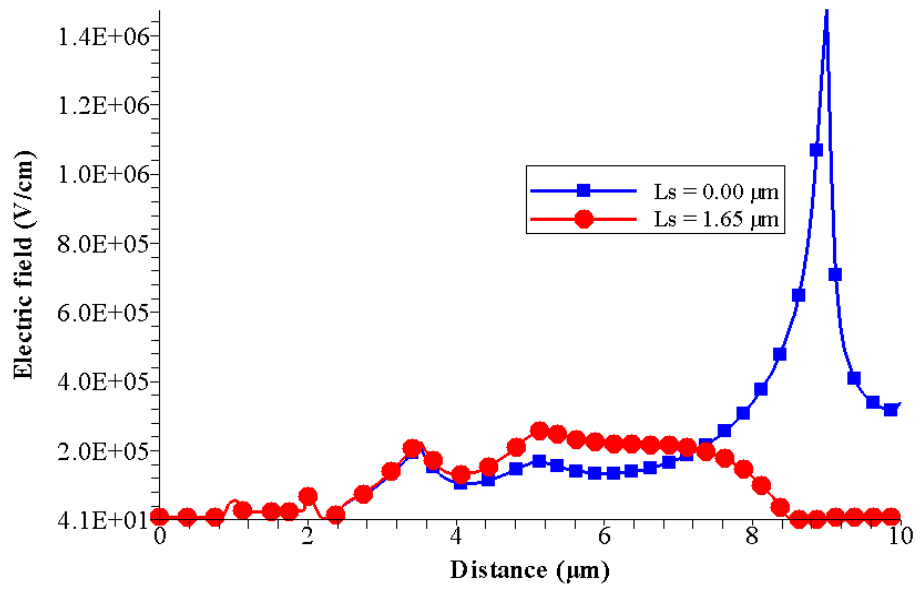


Fig. 11

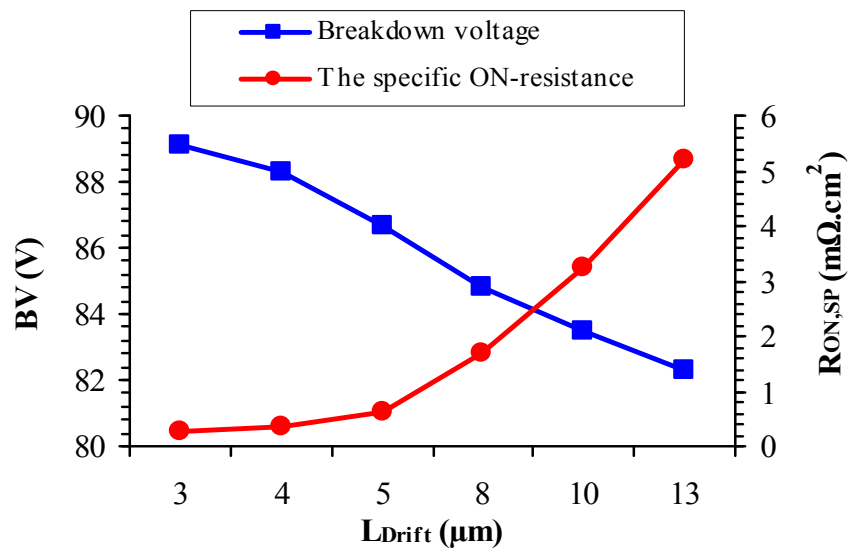


Fig. 12

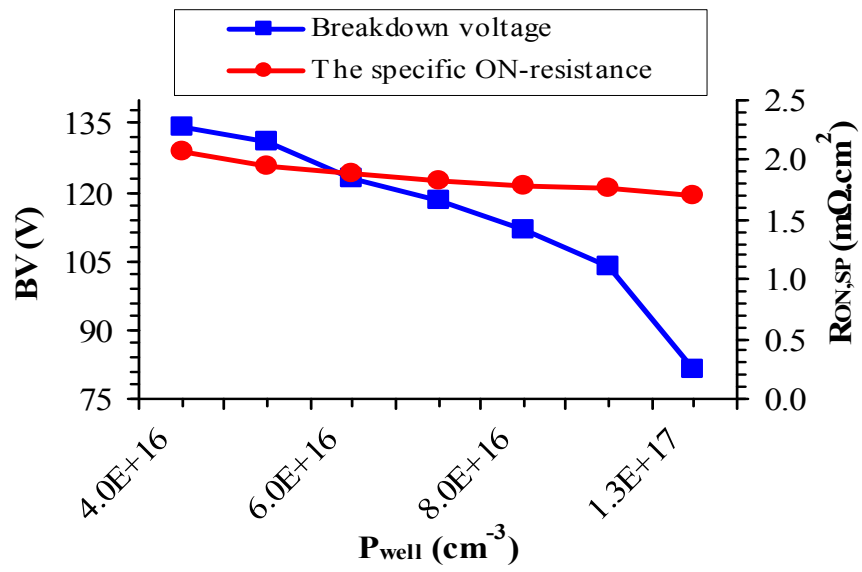


Fig. 13

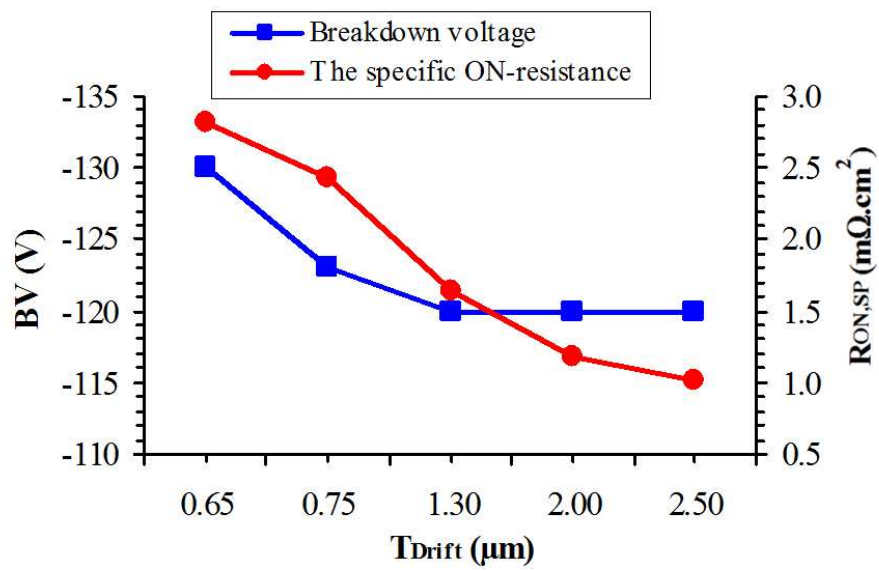


Fig. 14

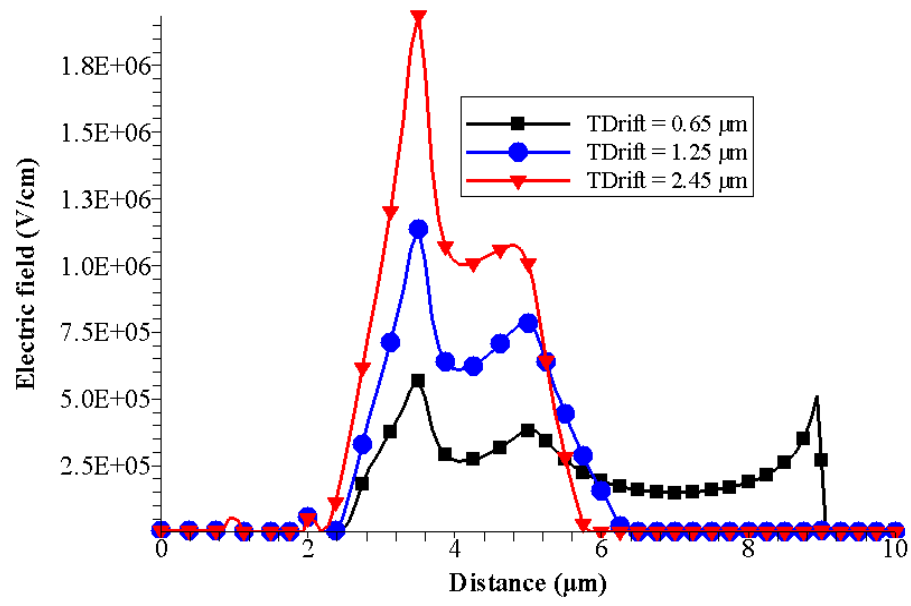


Fig. 15

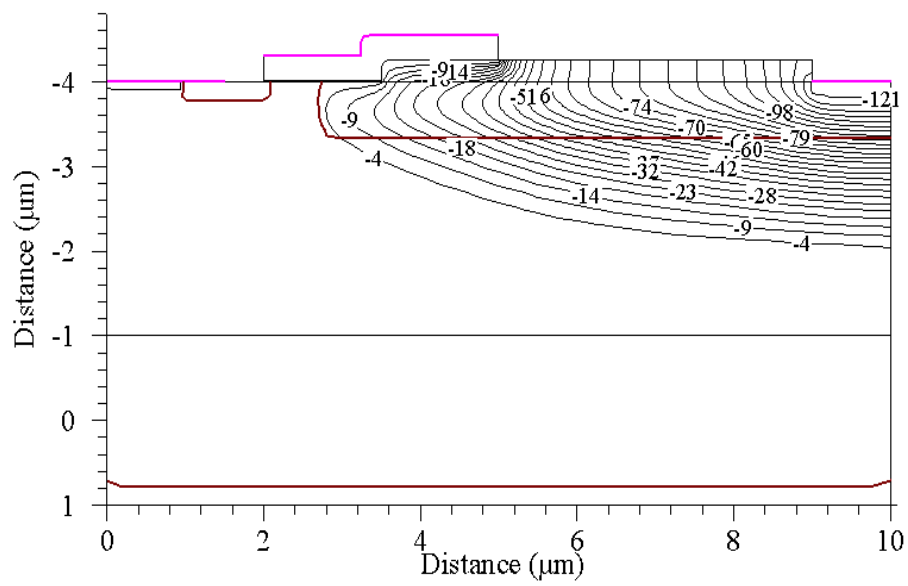


Fig. 16

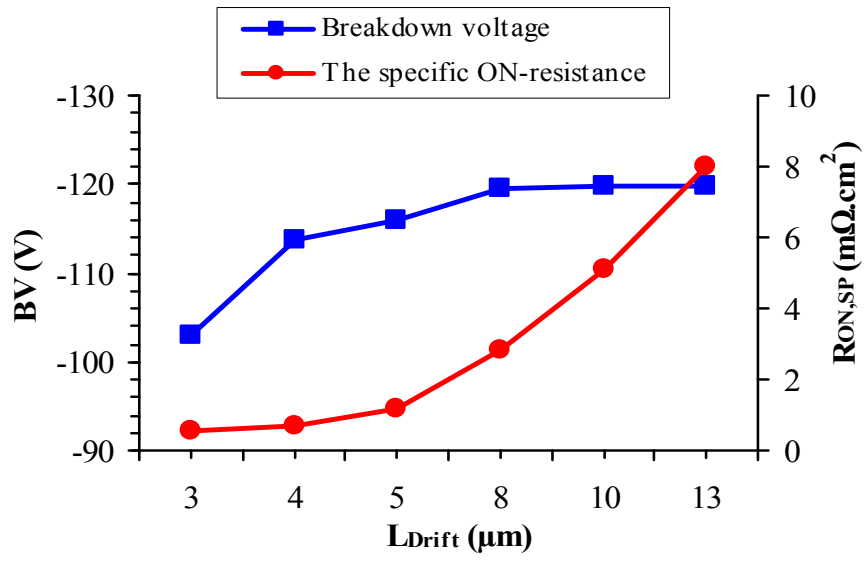


Fig. 17

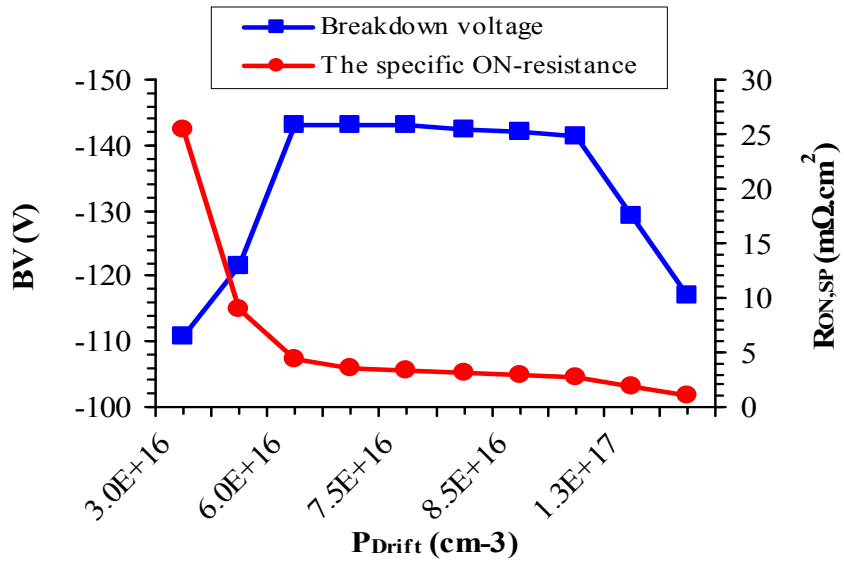


Fig. 18

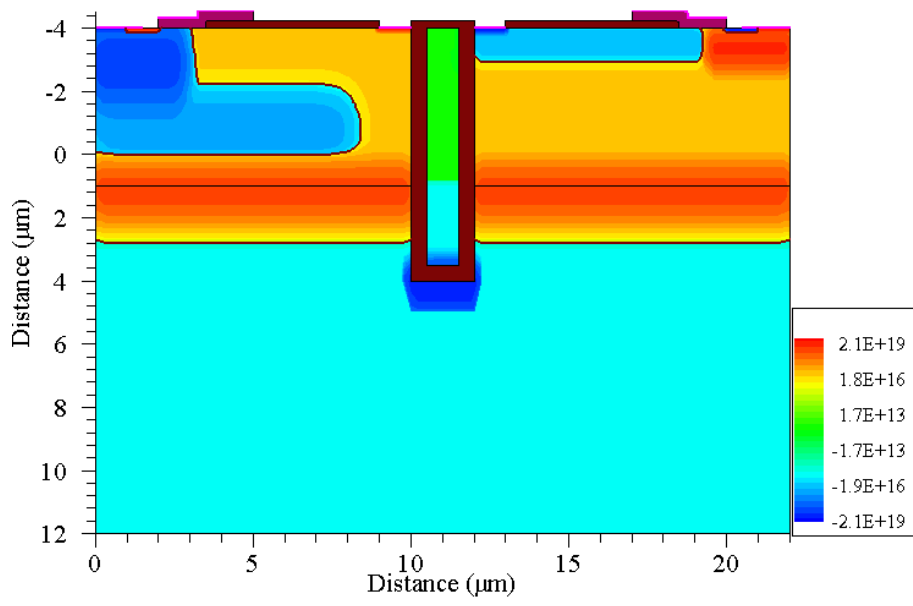


Fig. 19

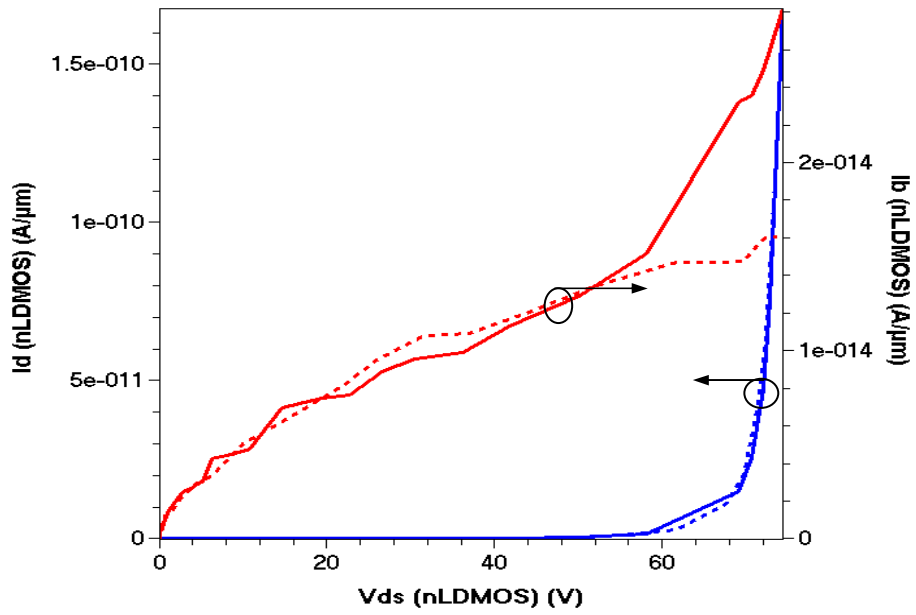


Fig. 20a

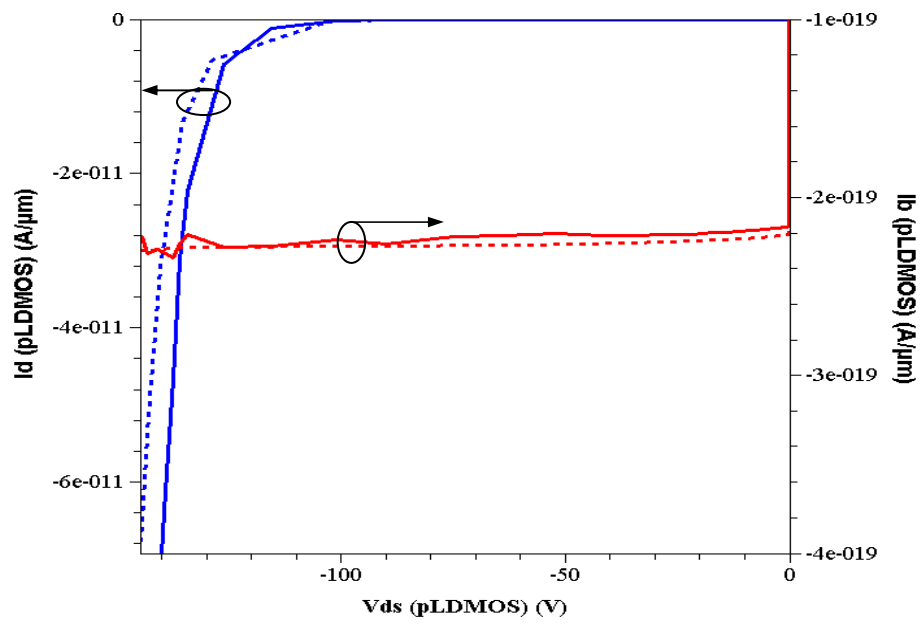


Fig. 20b

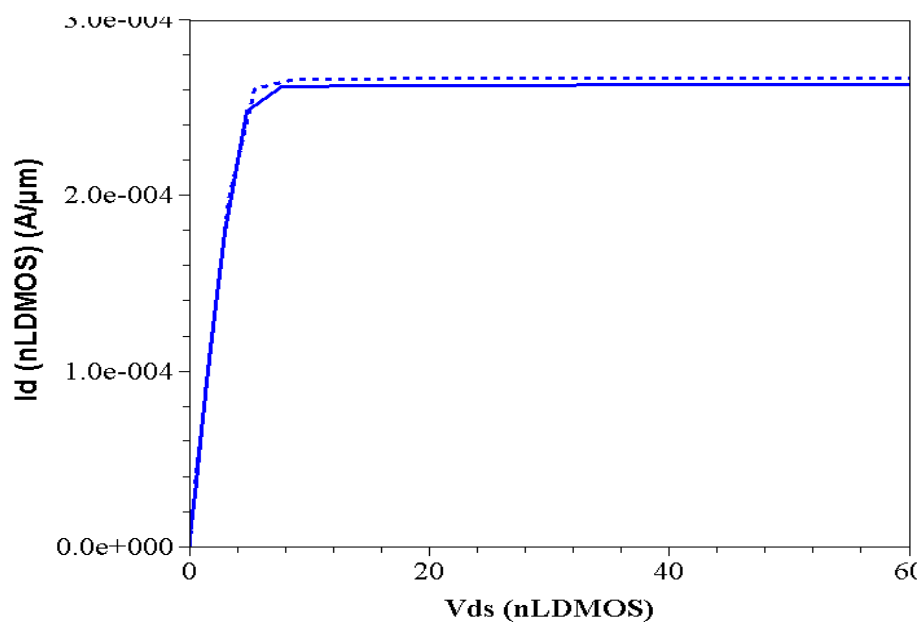


Fig. 21a

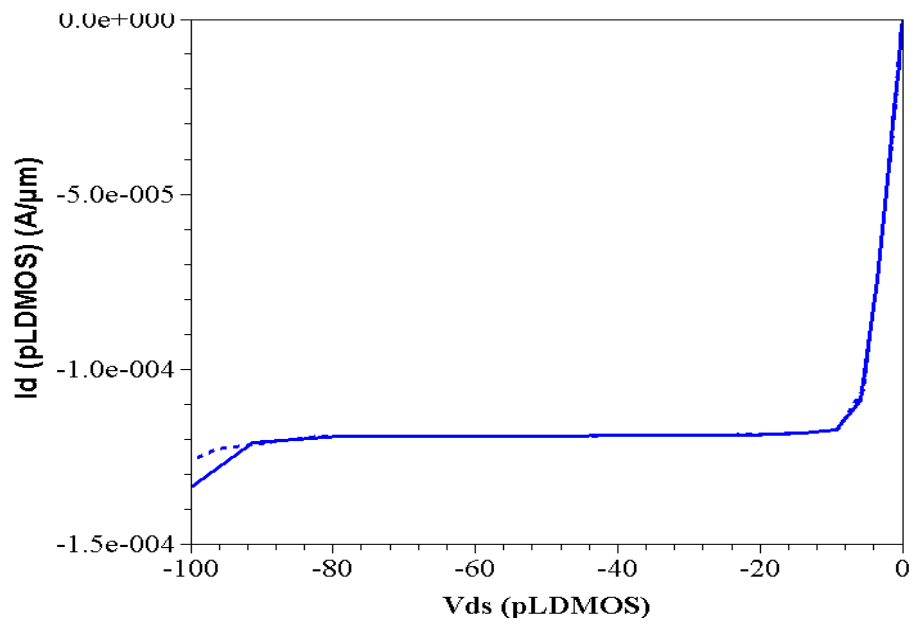


Fig. 21b

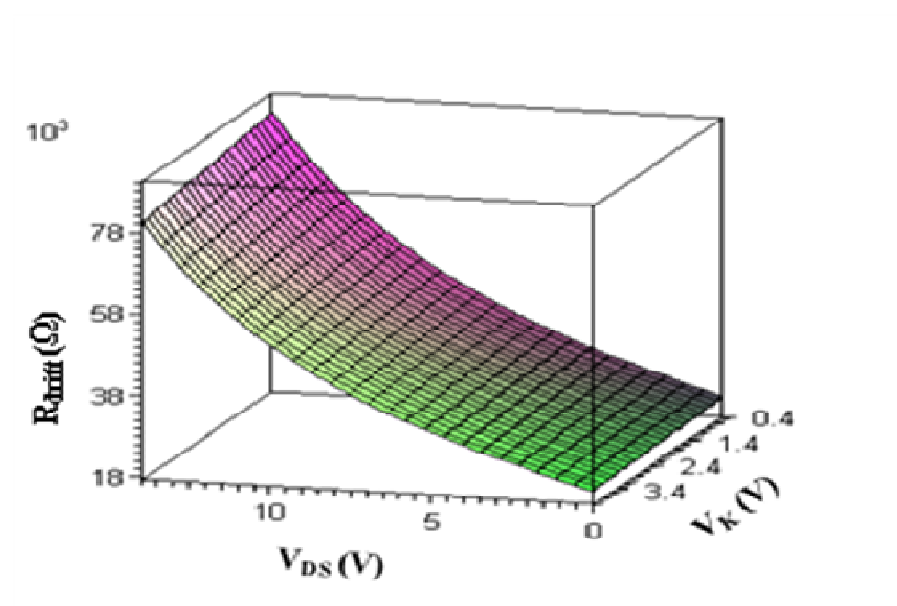


Fig. 22

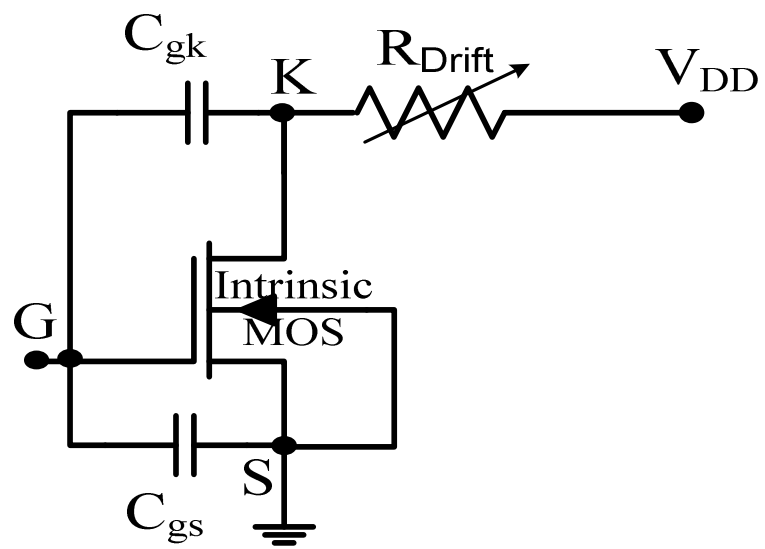


Fig. 23

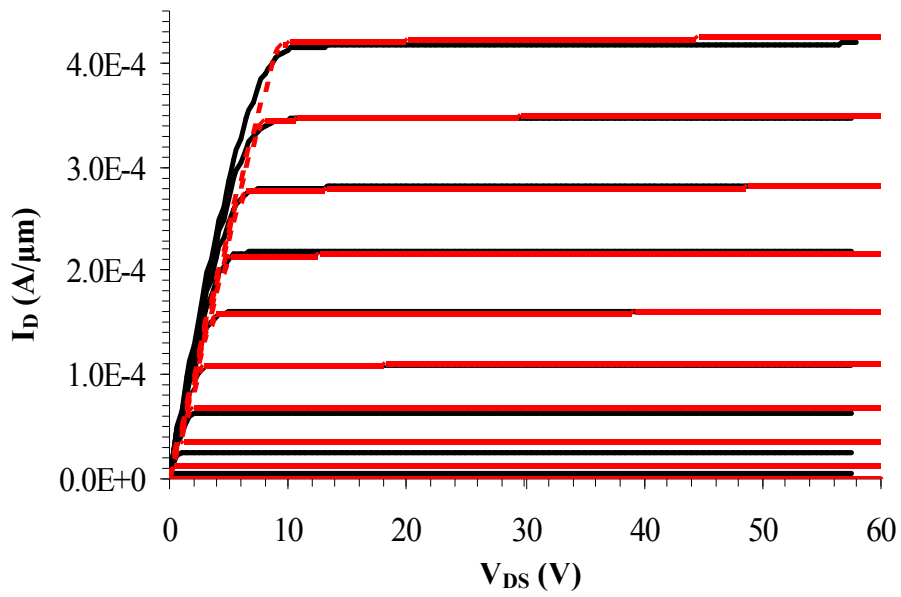


Fig. 24

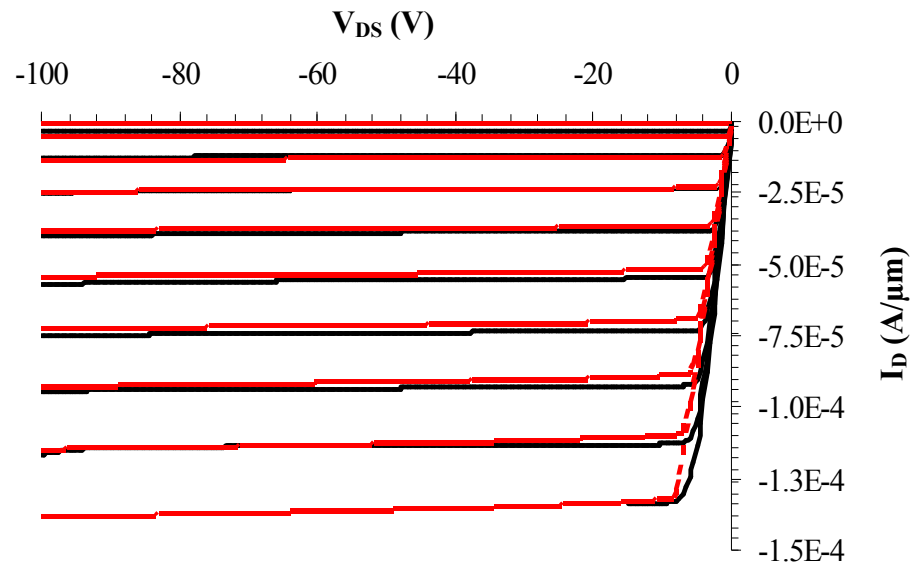


Fig. 25

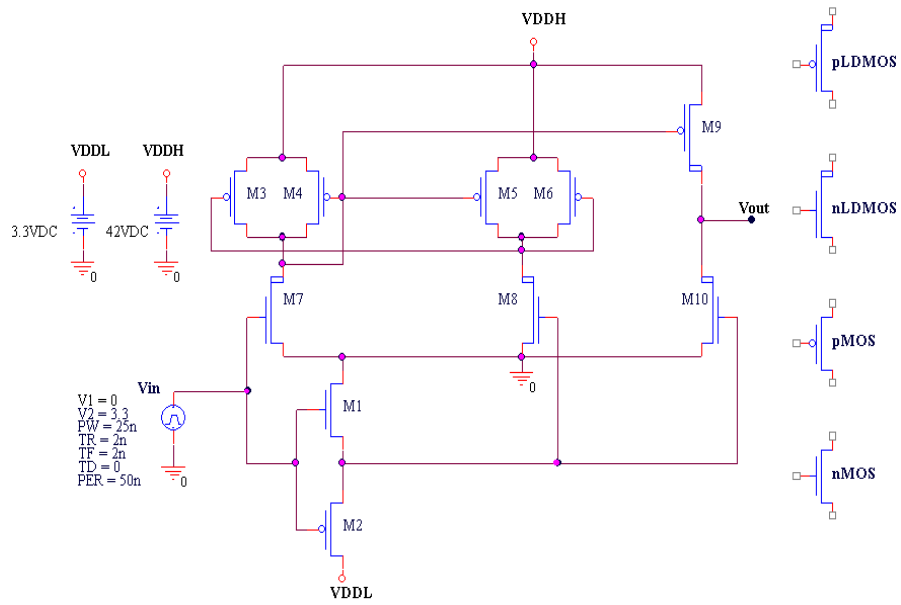


Fig. 26

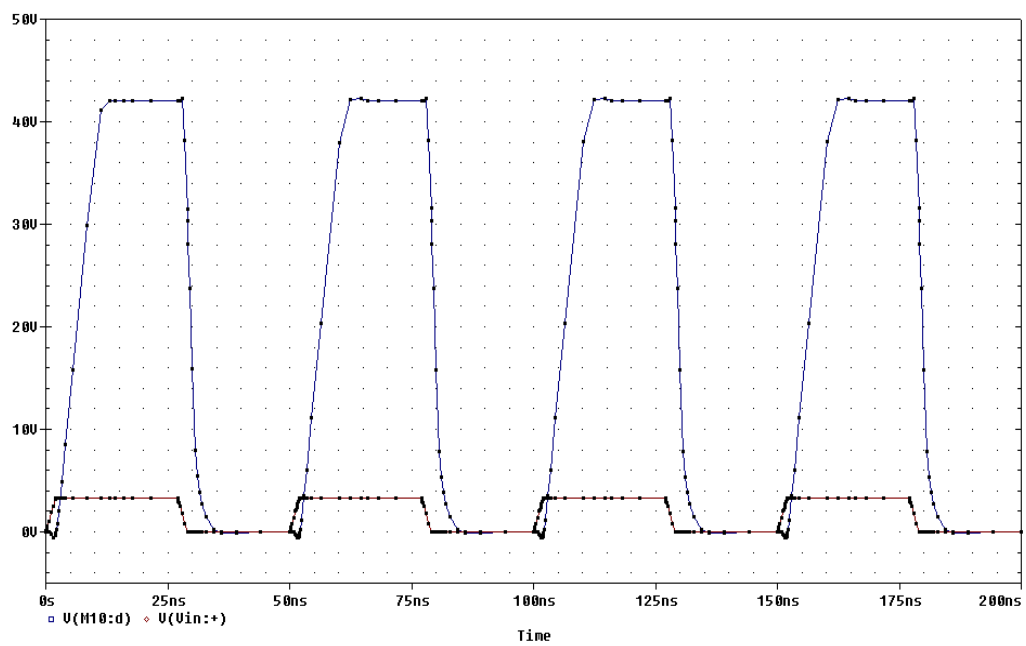


Fig. 27