



**HAL**  
open science

## **Automatic Stress Effects Computation Based On A Layout Generation Tool For Analog IC**

Stéphanie Youssef, Damien Dupuis, Ramy Iskander, Marie-Minerve Louërat

### ► **To cite this version:**

Stéphanie Youssef, Damien Dupuis, Ramy Iskander, Marie-Minerve Louërat. Automatic Stress Effects Computation Based On A Layout Generation Tool For Analog IC. 2010 IEEE International Behavioral Modeling and Simulation Conference (BMAS 2010), Sep 2010, San Jose, CA, United States. pp.7-12, <10.1109/BMAS.2010.6156590>. <hal-00749921>

**HAL Id: hal-00749921**

**<https://hal.science/hal-00749921v1>**

Submitted on 8 Nov 2012

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

# Automatic Stress Effects Computation Based On A Layout Generation Tool For Analog IC

Stéphanie YOUSSEF, Damien DUPUIS, Ramy ISKANDER and Marie-Minerve LOUËRAT  
LIP6 Laboratory, Université Pierre et Marie-Curie, Paris, France  
Email: stephanie.youssef@lip6.fr

**Abstract**— This paper studies the matching and the stress effect problems that appear in deep submicron CMOS technologies. These effects significantly affect the electrical behavior of CMOS transistors. We propose a method to compute stress effect parameters resulting from different layout styles such as interdigitated and symmetrical styles. We apply this method to a transistor device and a differential pair device. We also quantify the errors due to transistor folding and stress effects in 65nm CMOS technology for different device layouts. The results show the effectiveness of the proposed method.

**Keywords:** Compact modeling, analog IP, Reuse, Migration, Layout Generation, Stress effects

## I. INTRODUCTION

Traditionally, the design of an analog circuit is an iterative process. Given a set of specifications, the circuit is first

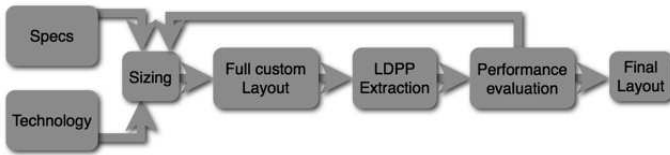


Fig. 1. Traditional design flow.

sized, then a full custom layout is performed, followed by an extraction of layout-dependent parasitics parameters (LDPP). Finally, the performance are evaluated using post layout simulation. The complete design flow is shown in Fig. 1. If the circuit does not meet the required specifications, the designer has to go through another iteration and modify the sizing, the full custom layout or both. The designer may iterate manually through several loops till satisfactory performance are achieved. Not only the number of iterations can be huge, but also each step of one design iteration is carried out on a different tool. This manual design flow is laborious, time consuming and subject to human error.

To speed up the design, layout-oriented design methodologies have been proposed in [1], [2], [3], [4] and [5]. [2] shows the advantage of providing a two ways communication between the sizing and layout generation as shown in Fig. 2. The idea is that the sizing tool provides the electrical parameters of the transistor such as the width (W), length (L), number of fingers (NF), etc... to the layout generation tool. Once the layout is generated, the layout tool sends back the layout-dependent parasitics parameters such as the drain and

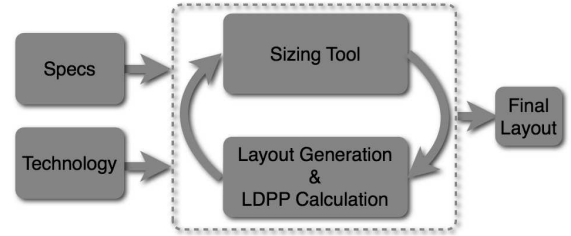


Fig. 2. Applied design flow.

source areas and perimeters, the stress effect parameters, etc... to re-evaluate the performance. This internal loop is repeated several times, with minimal designer intervention, till the target specifications are achieved. The final layout is then realized. Our layout generation tool allows the generation of parametrized and shaped layouts, with different analog dedicated layout styles [6]. Therefore this methodology minimizes the design time and possible errors. This approach has been implemented into our framework CHAMS which is dedicated to analog synthesis and technology migration for mixed signal circuits in nanometric technologies.

Section II defines the problem. Section III describes the layout generation tool environment. Section IV treats the stress effects for the MOS transistor. Section V shows the stress impact on a transistor. Section VI compares the stress effects for a differential pair laid out using different styles. Section VII presents the stress impact on a differential pair. Finally section VIII concludes the paper.

## II. PROBLEM DEFINITION

The evolution of CMOS from micro to nano technologies is driven by the need of less area, less power consumption and high speed integrated circuits providing better performance. With the migration to deep-sub-micron (DSM) technologies, two important constraints related to the layout of the circuit have to be taken into consideration :

a) *The problem of analog device matching:* Due to circuit aspect ratio, large transistors' widths have to be handled with dedicated layout styles. Transistor folding technique is commonly used to reduce parasitic capacitances and gate resistance [7], [8] allowing more accurate geometries and providing better electrical performance. Interdigitated and symmetrical

styles are usually used to equally distribute the gradient along the device.

*b) The Shallow Trench Isolation (STI):* The DSM technologies use Shallow Trench Isolation (STI) for its accurate dimension control when compared to LOCOS isolation [9]. STI is implemented in the form of trenches etched into the wafer and filled with silicon dioxide to isolate the active area of the transistors. Although STI provides some degree of latch-up protection, this isolation technique induces mechanical stress on the transistor and hence degrades its performance [10]. As shown in [11], this mechanical stress is highly dependent on the layout style being used. To reduce the impact of mechanical stress, the layout must be designed so that all the transistors of the device are affected in the same way.

In the subsequent sections, we study the influence of the mismatch and the stress effects on the performance of the devices (transistor and differential pair), as well as the suitable layout style for each of them considering matching and stress effects.

### III. LAYOUT GENERATION TOOL ENVIRONMENT

Our layout generation tool is based on Python language. This choice was motivated by the fact that Python is an easy to learn, object-oriented, portable and interpreted language. This allows the designer to write concise and simple code to describe complex layouts.

#### A. Stack object

As previously mentioned, folding technique is commonly used in analog circuits. Since this structure is essential, we have defined a 'Stack' object in our layout generation tool. To create the layout of a complete stack, the designer of parametrized analog devices (folded transistors, differential pair and current mirror) simply calls `createStack()` method with well specified input parameters.

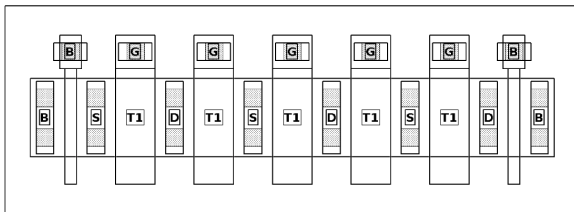


Fig. 3. Layout stack example  $W = 2.0\mu\text{m}$ ,  $L = 0.2\mu\text{m}$ ,  $NFs = 7$ ,  $Type = NMOS$  and  $NB_{dummies} = 1$ .

The input parameters of the `createStack()` method are :

- **Type:** The type of the transistor NMOS or PMOS.
- **W:** The overall width of the transistor.
- **L:** The length of each finger (except dummies).
- **NFs:** The number of stack's fingers (including dummies).
- **NB<sub>dummies</sub>:** The number of dummies at each stack ends.

Fig. 3 presents an example of a generated stack layout. The routing is not shown for clarity. The labels "T1" on the fingers

represent the transistor to which the fingers belong. Once a stack object has been created, it can be queried for useful layout distances as shown in Fig. 4. The distances provided

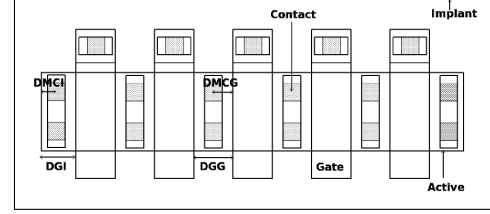


Fig. 4. Useful distances provided by the Stack object.

by the stack are :

- **DMCI:** Distance from the middle diffusion contact till the isolation edge.
- **DMCG:** Distance from the middle diffusion contact till the gate edge.
- **DGG:** Distance between two successive gates. This is equal to  $2 \times DMCG$ .
- **DGI:** Distance from the edge of the end gate to the isolation edge. This is equal to  $DMCI + DMCG$ .

Each distance has a method to query it in the stack object.

#### B. Extension Functions

For each device, described in Python, we define two methods. The first one computes the area and perimeter of the drain and source zones. The second one computes stress effect parameters introduced in BSIM4 [12] to model nanometric DSM effects. We propose a dedicated Python API to offer the possibility to describe technology independent layouts. The generated layout passes design rule checking.

### IV. THE STRESS EFFECTS FOR A TRANSISTOR

In the BSIM4 model [12] the stress effect parameters are  $SA$ ,  $SB$ ,  $SD$  as shown in Fig. 5.

- **SA:** Distance from the first left gate edge at the left end of the stack till the isolation edge at the left end of the stack. This is computed using

$$SA = DGI + NB_{dummies} \times (L_{dummy} + DGG) \quad (1)$$

where  $NB_{dummies}$  is the number of dummies and  $L_{dummy}$  is the dummy transistor length.

- **SB:** Distance from the first right gate edge at the right end of the stack till the isolation edge at the right end of the stack. This is computed using

$$SB = DGI + NB_{dummies} \times (L_{dummy} + DGG) \quad (2)$$

where  $NB_{dummies}$  is the number of dummies and  $L_{dummy}$  is the dummy transistor length.

- **SD:** Distance between two successive gates. This is set equal to  $DGG$ .

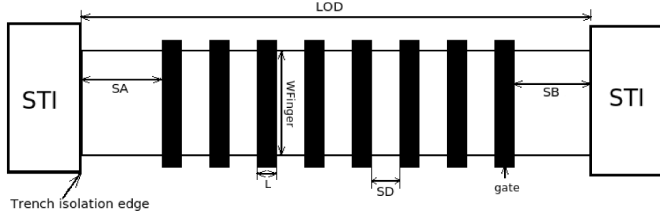


Fig. 5. The stress effect parameters for the transistor.

For the transistor that has multiple fingers  $NF$ , the BSIM4 model [12] calculates the effective values  $SA_{eff}$  and  $SB_{eff}$  for SA and SB respectively using:

$$Inv_{SA} = \sum_{i=0}^{(NF-1)} \frac{1}{SA + 0.5 \cdot L_{drawn} + i \cdot (SD + L_{drawn})} \quad (3)$$

$$Inv_{SB} = \sum_{i=0}^{(NF-1)} \frac{1}{SB + 0.5L_{drawn} + i \cdot (SD + L_{drawn})} \quad (4)$$

$$SA_{eff} = \frac{1}{Inv_{SA}} \quad (5)$$

$$SB_{eff} = \frac{1}{Inv_{SB}} \quad (6)$$

The stress effects affect model parameters such as the effective mobility  $\mu_{eff}$ , the velocity saturation  $V_{sat}$  and the threshold voltage  $V_{th}$  [13], [14], [15]. To reflect the influence of  $SA_{eff}$  and  $SB_{eff}$ , we define the parameter " $\alpha$ " that depends on both:

$$\alpha = \frac{1}{\frac{1}{2SA_{eff}} + \frac{1}{2SB_{eff}}} \quad (7)$$

In Fig. 6, we plot  $1/\alpha$  versus  $NF$  for NMOS transistor in 65nm technology with  $W = 6\mu m$  and  $L = 0.15\mu m$ . We notice how

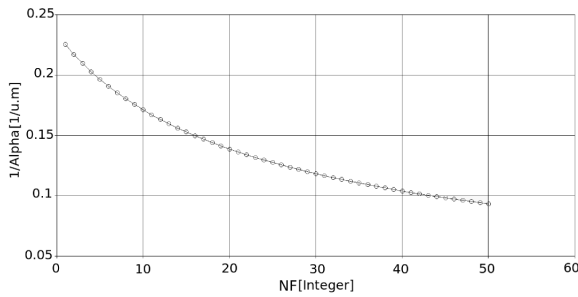


Fig. 6. The stress effect parameter  $1/\alpha$  versus  $NF$ .

stress effects decrease by increasing  $NF$ .

## V. RESULTS FOR A TRANSISTOR

### A. Stress effect errors

After the generation of the layout, the extension function `ComputeStressEffect()` is called to compute the stress effect parameters. The parameter values were verified for correctness against a commercial extraction tool. These values

are then used to back-annotate a spice netlist for simulation. We compute the percentage of the normalized current error in a specific case  $IDS$  compared to a reference current  $IDS_{Ref}$ :

$$Error = 100 \times \left| \frac{IDS - IDS_{Ref}}{IDS_{Ref}} \right| \quad (8)$$

Let us consider an NMOS transistor in 65nm technology with  $W = 6\mu m$  and  $L = 0.15\mu m$ . We choose  $NF = 1$  since it corresponds to the maximum stress effects. Fig. 7 shows the drain current  $IDS$  versus  $VGS$  in two different cases:

- With stress effect where  $NF = 1$ ,  $SA_{eff}$  and  $SB_{eff}$  are minimal.
- Without stress effect  $NF = 1$ ,  $SA_{eff} = \infty$  and  $SB_{eff} = \infty$ .

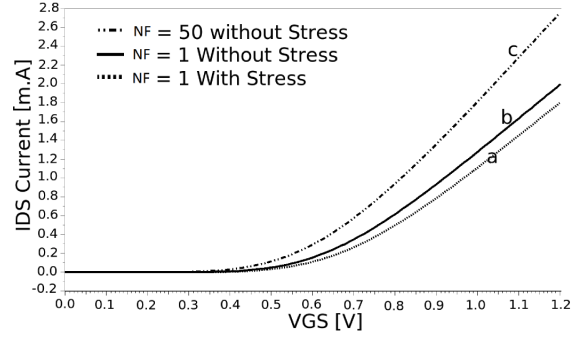


Fig. 7. Stress and Folding effect on Current for NMOS transistor.

The simulation results in Fig. 7 show that the stress effects decrease  $IDS$ . The calculation of the percentage of the nor-

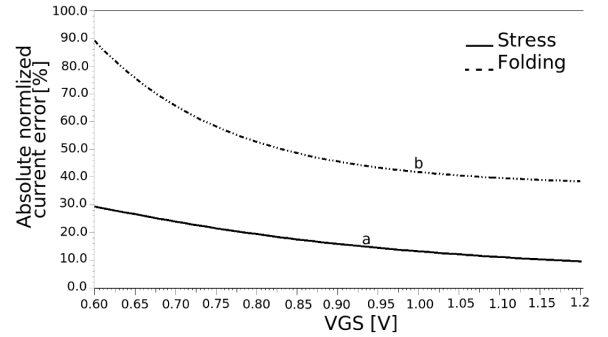


Fig. 8. Absolute normalized current error for stress and folding effect for NMOS transistor.

malized drain current error is shown in Fig.8 case (a).

### B. Folding effect errors

A folded transistor with  $NF = 50$  is compared to a single finger transistor having the same total width. The simulation results are shown in Fig. 7. It is clear that transistor folding increases the drain current due to the inverse narrow width effects [16]. Fig. 8 case (b) shows the percentage of the normalized drain current error for  $NF = 50$ . We conclude that stress effects and transistor folding highly affect the drain current and should be considered simultaneously.

### C. Reducing stress effect

The mechanical stress effect can be reduced by increasing the number of fingers and/or adding dummies at each side of the stack.

- **Increasing the number of fingers  $NF$**  : The drain current of a  $6\mu\text{m}/0.15\mu\text{m}$  NMOS transistor is simulated versus VGS for different values of  $NF$ . The drain current is compared to a reference current of a similar transistor without stress effect. Fig. 9 shows the percentage of the normalized current error versus VGS. The maximum number of fingers chosen in this simulation is 20. Clearly, the normalized current error decreases significantly when increasing the number of fingers.

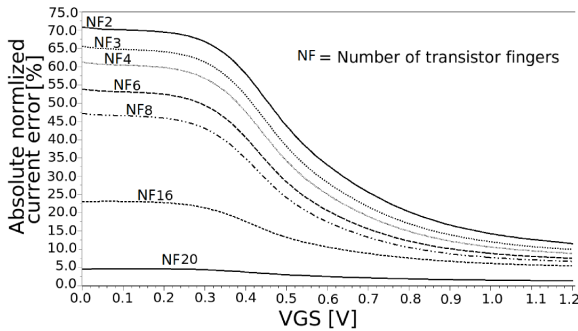


Fig. 9. The effect of the variation of number of number of fingers on the stress effect.

- **Adding transistor dummies at each side of the Stack** : On the other hand, adding transistor dummies at each side of the stack makes the transistor fingers less prone to stress effects. A simulation for the drain current versus VGS is performed for an NMOS transistor with  $NF = 8$ , while varying the number of dummies at each side. The current is compared to a reference current of a similar transistor without stress effects and without dummies. Fig. 10 shows the percentage of the normalized current error versus VGS. The figure shows that the stress effects

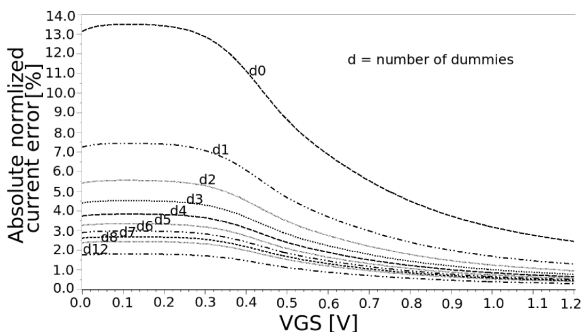


Fig. 10. The effect of the variation of number of dummies on the stress effect.

decrease with increased number of dummies at each side. It should be noted that adding a single dummy at each side ( $d1$  curve) has a significant reduction in the normalized current error when compared to a transistor

with no dummies ( $d0$  curve). By further increasing the number of dummies at each side, the improvement in stress effects induced errors becomes less significant. A trade-off between the total area of the device and its performance is introduced: increasing the number of dummies improves the transistor immunity to stress effects but increases the overall area of the design.

The above results are for NMOS transistor. As reported in literature [17], [18] the stress effects increase the PMOS current and enhances its mobility. To compensate the current increase due to stress effects and folding, it is desirable to reduce the PMOS number of fingers [19], [20].

### VI. THE STRESS EFFECTS FOR A DIFFERENTIAL PAIR

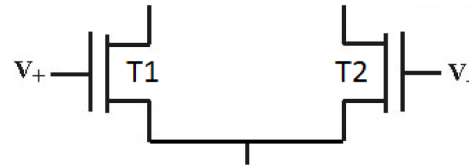


Fig. 11. Differential Pair Schematic View.

When considering the effects of mechanical stress on differential pair, the analysis differs significantly from that of a standalone transistor. For the case of a standalone transistor, all the fingers belong to the same device. On the other hand, a differential pair requires the matching of two different transistors. The calculation of the stress effects parameters becomes more complicated as it deals with matched fingers from different transistors. In this case, the calculation of stress parameters for a differential pair depends on the layout style chosen for the differential pair. Fig. 11 shows a differential pair consisting of transistors T1 and T2. In the following, we discuss the stress effects calculations for the layout styles: *symmetrical* and *interdigitation*.

#### A. Symmetrical style

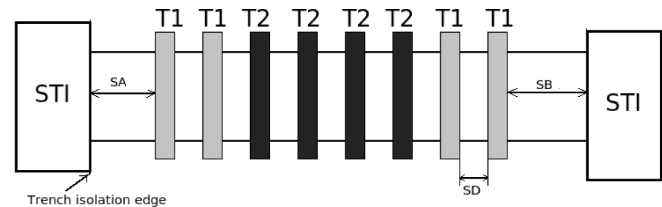


Fig. 12. The stress effect parameters for the symmetrical style.

The stress effect parameters for differential pair can be calculated using the equations (3)-(4) of the transistor device applied to each transistor (T1 and T2) separately. The main difference is that the calculations of one transistor change according to the position its fingers. For example, when considering the first device, the summation is carried out on the range from 0 to  $NFs-1$  instead of  $NF-1$ . The presence of

the fingers of the other transistor alternating to the calculated transistor's fingers creates what we called holes. This requires the introduction of a new parameter  $\delta$  in the formula. The parameter  $\delta$  takes the value of 1 when pointing to a finger of the transistor considered, and the value of 0 when pointing to a finger of the other transistors.

$$Inv_{SA,T1} = \sum_{i=0}^{(NFs-1)} \frac{\delta i}{SA + 0.5 \cdot L_{drawn} + i \cdot (SD + L_{drawn})} \quad (9)$$

$$Inv_{SB,T1} = \sum_{i=0}^{(NFs-1)} \frac{\delta i}{SB + 0.5L_{drawn} + i \cdot (SD + L_{drawn})} \quad (10)$$

$SA_{eff}$ ,  $SB_{eff}$  and  $\alpha$  are calculated in the same manner as the case of the transistor device.

### B. Interdigitated style

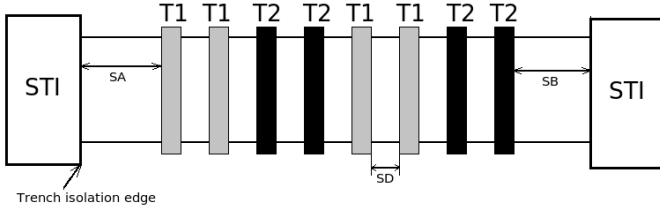


Fig. 13. The stress effect parameters for the interdigitated style.

The same equations of symmetrical styles are used for the interdigitated style. Since the placement is different, the values taken by  $\delta_i$  differ.

## VII. RESULTS FOR A DIFFERENTIAL PAIR

We evaluate the stress effects for both transistors T1 and T2 of the differential pair. Each transistor has  $W = 6.0\mu\text{m}$ ,  $L = 0.06\mu\text{m}$  and  $NF=4$  in 65nm technology. In the following subsections, we study the influence of stress effects on the biasing current for different layout styles.

### A. Symmetrical style

In old technologies for long channel devices, the symmetrical style in Fig. 14 was preferred since it eliminates the linear gradient effects along the substrate. The linear gradient could produce significant mismatch as the devices had a large area.

Fig. 15 shows the absolute normalized error in the drain current for each of both transistors T1 and T2 of the differential pair with symmetrical layout. The error in T1 current is more than twice that of T2. This is expected as T1 transistor has its fingers nearer to the STI than transistor T2 and thus T1 is more prone to the stress effects than T2.

To interpret the above results, we compare the variation of  $1/\alpha$  versus NF. In the new nanometric technologies, the transistors have a smaller area and the stress effects have become more important. Fig. 16 clearly illustrates how the transistors are affected differently by the mechanical stress of the STI

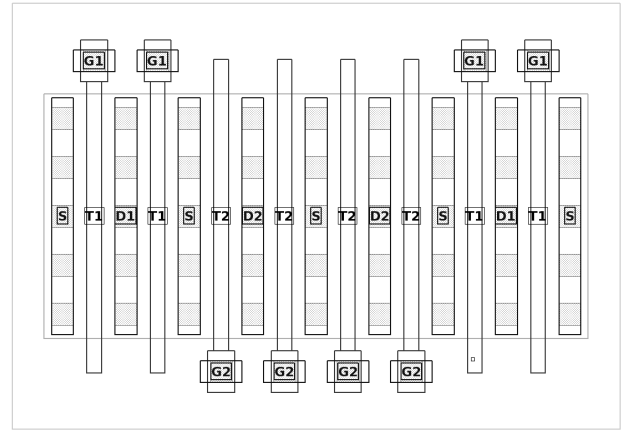


Fig. 14. Layout generation of the Symmetrical style.

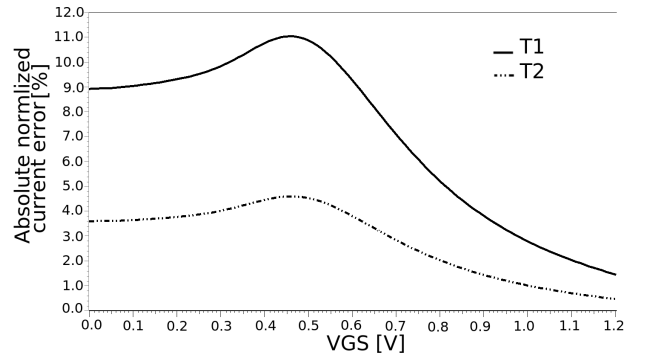


Fig. 15. The stress effect parameters for the symmetrical style.

inducing a significant mismatch between the differential pair devices.

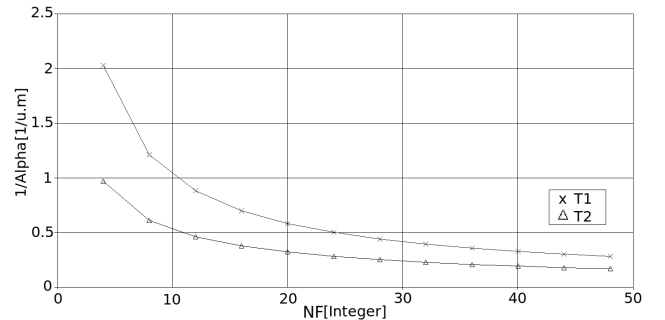


Fig. 16. The stress effect  $1/\alpha$  parameter versus NF of the Symmetrical style.

### B. Interdigitated style

The interdigitated style for the differential pair is shown in Fig. 17 .

Fig. 18 shows the absolute normalized error in the drain current for both transistors T1 and T2 of the differential pair with interdigitated layout. The error is identical for both transistors since they are evenly affected by the same stress effects.

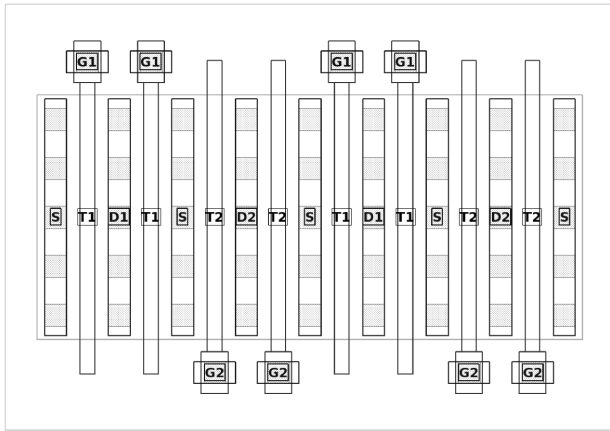


Fig. 17. Layout generation of the interdigitated style.

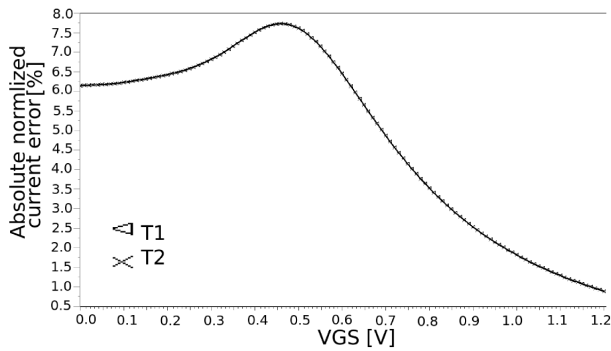


Fig. 18. The stress effect for the interdigitated style.

Fig.19 shows that both transistors shows identical  $1/\alpha$  versus NF curves. This clearly reflects the perfect matching of the two transistors.

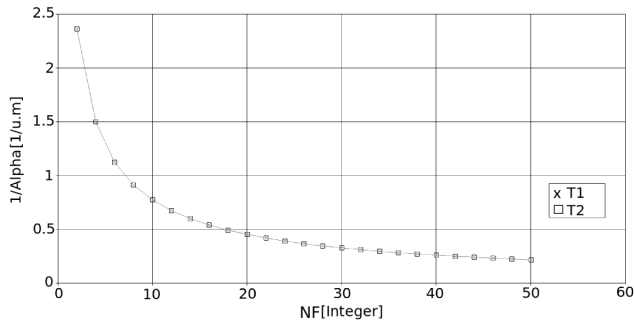


Fig. 19. The stress effect  $1/\alpha$  parameter versus NF of the interdigitated style.

We conclude that the interdigitated layout style is much preferred to eliminate the stress effects, which are more significant in nanometric technologies.

## VIII. CONCLUSION

In this paper we have presented a method that allows simple and concise description for complex devices in nanometric technologies. It allows direct and accurate quantification of

stress effects and folding for different layout styles. The designer is therefore able to compare between layout styles and choose the suitable device layout for his circuit. We have examined the stress effects for a transistor and a differential pair. We showed that layout styles preferred for old technologies may not be beneficial for new nanometric technologies.

## REFERENCES

- [1] M. Dessouky *et al.* A layout approach for electrical and physical design integration of high-performance analog circuits. In *Proc. of the 1st International Symposium on Quality of Electronic Design*, page 291, San Jose, USA, 2000.
- [2] M. Dessouky *et al.* Layout-oriented synthesis of high performance analog circuits. In *Proc. Design, Automation and Test in Europe*, pages 53–57, Paris, France, March 2000.
- [3] R. Castro-Lopez *et al.* An Integrated Layout-Synthesis Approach for Analog ICs. *IEEE Trans. on Computer Aided Design*, 27(7):1179–1189, July 2008.
- [4] M. Ranjan *et al.* Fast, layout-inclusive analog circuit synthesis using pre-compiled parasitic-aware symbolic performance models. In *Proc. Design, Automation and Test in Europe Conf.*, pages 604–609, Paris, France, February 2004.
- [5] V. Joshi *et al.* Stress aware layout optimization. In *Proc. Int. Symp. on Physical design*, pages 168–174, Portland, Oregon, April 2008.
- [6] R. Jacob Baker. *CMOS: circuit design, layout, and simulation*. John Wiley and Sons, 2008.
- [7] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, 2000.
- [8] Ravindranath Naiknaware *et al.* Automated hierarchical CMOS analog circuit stack generation with intramodule connectivity and matching considerations. *J. Solid-State Circuits*, 34(3):304–317, March 1999.
- [9] D. Andriukaitis *et al.* LOCOS CMOS process simulation. In *Conf. Information Technology Interfaces*, pages 489–494, Catvat, Croatia, June 2006.
- [10] W.L. Goh *et al.* Latchup characterization of 0.18-micron sti cobalt silicided test structures. *Microelectronics Journal*, 32(9):725–731, September 2001.
- [11] W.L. Goh *et al.* A comprehensive geometrical and biasing analysis for latchup in 0.18- $\mu\text{m}$   $c_{o}si_2$  STI CMOS structure. *Solid-State Electronics J.*, 48:2109–2114, 2004.
- [12] W. Liu. *MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4*. Wiley Interscience, 2001.
- [13] L. Yang *et al.* Simulation of layout-dependent STI stress and its impact on circuit performance. In *Int. Conf. on Simulation of Semiconductor Processes and Devices*, pages 281–284, San Diego, USA, September 2009.
- [14] H. Tsuno *et al.* Advanced analysis and modeling of MOSFET characteristic fluctuation caused by layout variation. In *VLSI Technology Symposium*, pages 204–205, Kyoto, Japan, June 2007.
- [15] V. Moroz *et al.* The impact of layout on stress-enhanced transistor performance. In *Int. Conf. on Simulation of Semiconductor Processes and Devices*, pages 143–146, Tokyo, Japan, September 2005.
- [16] C. Pacha *et al.* Impact of sti-induced stress inverse narrow width effect and statistical vth variations on leakage currents in 120 nm cmos. In *European Solid-State Device Research Conf.*, pages 397–400, Leuven, Belgium, September 2004.
- [17] C.-C. Wang *et al.* Compact modeling of stress effects in scaled CMOS. In *Int. Conf. on Simulation of Semiconductor Processes and Devices*, pages 131–134, San Diego, USA, September 2009.
- [18] P.G. Drennan *et al.* Implications of proximity effects for analog design. In *Custom Integrated Circuits Conf.*, pages 169–176, San Diego, USA, September 2006.
- [19] J. Xue *et al.* Layout-dependent sti stress analysis and stress-aware rff/analog circuit design optimization. In *Proc. of Int. Conf. on Computer-Aided Design*, pages 521–528, San Jose, USA, November 2009.
- [20] A. B. Kahng *et al.* Exploiting sti stress for performance. In *Proc. of Int. Conf. on Computer-Aided Design*, pages 83–90, San Jose, USA, November 2007.