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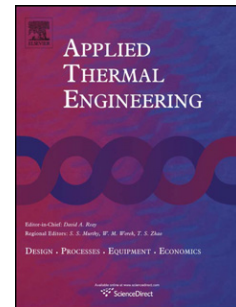


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Low-cost and versatile thermal test chip for power assemblies assessment and thermometric calibration purposes

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Abstract. Chips specifically designed for thermal tests such as the assessment of packages, are of main interest in Microelectronics. Nevertheless, these test dies are required in relatively low quantities and their price is a limiting factor. This work describes a low-cost thermal test chip, specifically developed for the needs of power electronics. It is based on a poly-silicon heating resistor and a decoupled Pt temperature sensing resistor on the top, allowing to dissipate more than 60 W (170 W/cm²) and reaching temperatures up to 200°C. Its simple structure allows an easy simulation and modeling. These features have been taken in profit for packaging materials assessment, calibration of temperature measurement apparatus and methods, and validation of thermal models and simulations.

Keywords: thermal test chip, thermometric calibration, thermal model validation, packaging, power electronics.

1. Introduction

Test chips have been widely used to analyze the interactions and degradation mechanisms between integrated circuits (ICs) and their packages [1, 2]. In this framework, thermal test chips (TTC) have been extensively used as a powerful thermal validation tool in the field of thermal management for a long time [3, 4]. Basically, TTCs are chips with embedded heat sources and temperature sensors for the evaluation of thermal resistance, thermal impedance and package thermal design qualification [5] [6]. Their basic principle of operation consists in biasing the

heating element to dissipate a well known power waveform and, simultaneously, measuring the associated temperature increment. Beside, TTCs have also been employed for in-chip thermal coupling (thermal cross-talk) analysis [7] and thermometry calibration purposes [8].

In the last years, the importance of TTCs has increased as a response to the high power densities dissipated in sophisticated ICs and packages. For example, reference [9] describes a thermal tester developed around a TTC working in the 100-200 W/cm² range, for the thermal assessment of packaging solutions for digital processors. The literature reports also several TTC designs with different topologies of heat sources and temperature sensors, including different interconnection possibilities (bumps or wire-bonding) and variable chip-size using chip-array combinations [10]. Nevertheless, most of the reported TTCs have been conceived to reproduce the behavior of low power ICs. This represents a limitation when the objective is the assessment of packaging technologies developed for power electronics applications, since power devices dissipate power densities orders of magnitude higher than ICs, show different contact pads configurations, etc. Examples of devices oriented to pure power electronics applications are the test dies P432 and H029 from ST-Microelectronics, implementing bipolar and VDMOS transistors respectively [11]. Concerning their DC thermal performances, the P432 and H029 allow dissipating a maximum power of 40 W and 300 W, respectively. However, the fabrication process is the same used for functional power transistors, resulting in a relatively high cost.

Another option for high power package assessment consists in using functional semiconductor power devices, which are easily available. After a heating phase, the device temperature is indirectly estimated using a temperature sensitive parameter (TSP) with the device adequately biased [12]. This approach presents several drawbacks. First, the heating and the temperature sensing circuits are electrically coupled, requiring the combination of measurement and high power circuitries. Second, as the thermal tests are divided in heating and measurement phases, it is not possible to monitor continuously the die temperature evolution at any heating time instant. Finally, the relationship between dissipated power and temperature increase is not always linear for high dissipated powers, mainly in specific devices with small geometries such as RF transistors [13]. All these limitations are overcome using TTCs because the heating and temperature sensing elements are naturally decoupled.

This paper proposes a new design concept for TTCs oriented to the assessment of power electronics packages and modules. It reproduces the thermal behavior of typical vertical power devices (IGBTs, MOSFETs, fast recovery diodes, etc.). In addition, the design of the proposed TTC follows the JEDEC JESD 51-4 [14] guidelines and can be used in other frameworks than power electronics. The first section of the paper describes the basic design concepts, structure

and fabrication process of the device. The second section analyses the electrical and thermal behavior of the test chip, in view of its utilization in practical thermal experiments. Finally, some application examples corresponding to three different research fields, demonstrate the usefulness and versatility of the proposed device: the assessment of power substrates, the validation of thermal models and simulations and the calibration of thermometry techniques oriented to device-level temperature measurement.

2. Thermal Test Chip structure and fabrication

2.1. Basic design concepts

The proposed TTC was designed to reproduce the thermal behavior of the most employed vertical power devices, such as fast recovery diodes (FRD), power MOSFETs or Insulated Gate Bipolar Transistors (IGBT). In the most common discrete components and power modules based on these families of devices, the heat is mainly generated in the top zone of the die and the heat flux dissipation path is established towards the chip backside. Even when the dissipation heat sources are relatively small, like the cells of the MOS controlled devices, the heat flux towards the backside spreads laterally and at a given depth from the top, the heat flux is uniform and the isothermal surfaces are parallel. This behavior is determined by the relatively high thermal conductivity of Silicon, around 148 W/m.K at room temperature. Thus, the TTC could be based on uniformly distributed heat sources on its top, capable of dissipating several tens or even hundreds of Watts. These power sources could be simple resistors, active bipolar transistors or MOSFET devices. Although active devices provide higher degrees of freedom in order to dissipate a given power during thermal experiments, their manufacture involves relatively critical and expensive technology steps, such as implantations, diffusions or gate oxide growth. In the present work, we propose to integrate a distributed resistor on the top of a Silicon die, the best technical solution being the parallel connection of deposited poly-Silicon strips. On the other hand, two main options arise for an easy chip temperature measurement: implementation of resistance temperature detectors (RTD) or diodes [15]. Both kinds of temperature sensors show different advantages. For instance, temperature sensing diodes can be implemented in a very small area while RTDs show a higher linearity. Nevertheless, the present work aimed at developing a low cost TTC, and therefore, the implementation of an RTD sensor was decided. The RTD was based on a Platinum deposition, avoiding the implantation and diffusion steps required to fabricate a rectifier junction. As it is well known Platinum is a good choice to implement a temperature sensor because the resulting RTD shows a good linearity, sensitivity, stability and wide operation temperature range.

Concerning the chip size, typical power devices are comprised between a few square millimeters and more than 150 mm². The final selected dimensions have been 6 mm × 6 mm, which are representative of medium power IGBTs, FRDs and power MOSFETs. Figure 1 presents a top view picture of the fabricated TTC soldered on a ceramic substrate. The paralleled Aluminum wire-bonds (25 µm diameter) at both sides connect the lateral Aluminum heating resistor (R_H) pads to the power terminals of the assembly, giving a high current bias capability. Connected to the four central pads are also visible the wire-bonds providing external Kelvin measurement capability for the temperature sensing resistor (R_S). It can be observed how the poly-Silicon strips of the R_H surround the R_S zone. This layout allows an outline of the heating source covering a 98 % of the chip area inside the bonding pads.

Figure 1

2.2. Fabrication steps and structure

The TTC has been developed on standard 525 µm thick Silicon CMOS substrates of both, P- and N-type. Figure 2 shows a schematic cross section of its basic structure. The fabrication process starts with the growth of a 35 nm SiO₂ layer, followed by an additional 1 µm local oxidation under the areas that will be taken up by the connection pads. The thin oxide layer provides an appropriate insulation mechanism between both resistors, R_H and R_S . After that, a 350 nm poly-Silicon layer is deposited on the top of the thin oxide and the R_H stripes are defined by photolithography and dry-etching. The R_H layout consists basically in 130 parallel poly-Silicon tracks, 20 µm wide and spaced 17.2 µm between them. Then, a 1.3 µm interlevel oxide is deposited to protect the poly-Silicon. This SiO₂ layer is opened (dry etching) in the central part of the chip, where the RTD will be defined, and in the lateral areas where the Aluminum pads will contact the poly-Silicon strips. A new deposition, photolithography and wet etching steps, allow the definition of the 2 µm thick Aluminum pads corresponding to the R_H terminals. Next, the definition of R_S in the central part of the chip starts with the deposition of a 20 nm Titanium layer to improve the adherence of the subsequent 150 nm thick Platinum layer. This layer is patterned by lift-off and its layout consists basically on a folded track, taking a total area of 700 µm × 700 µm. The resistance value can be accurately measured using the 4-wire (Kelvin) technique through the corresponding 120 µm × 120 µm Platinum pads. The fabrication of the TTC finishes with the top passivation layer (500 nm SiO₂ and 700 nm Si₃N₄) and the backside metallization with a Ti/Ni/Au multilayer. The left side of Figure 2 represents the edge zone of the die, with the Aluminum pads of the R_H terminals and the poly-Silicon strips, while the right side shows the centre of the chip including the Platinum sense resistor.

Figure 2**3. Thermal Test Chip Performances****3.1. Temperature Sensor and Heating Source Characterization**

Figure 3 plots the temperature versus R_S value measured for 20 different dies in the 25°C up to 135°C range. As it can be observed, the R_S dispersion at ambient temperature for this population is between 630 Ω and 775 Ω , but the slopes of the curves (which represent in fact the R_S sensitivity with temperature) show a lower variation. This means that for applications not requiring very high accuracy, the calibration of R_S can be simplified measuring only its value at ambient temperature and assuming the mean slope value measured for a significant number of devices. For example, for the 20 devices measured in Figure 3, the mean slope value is 0.95 °C/ Ω and the standard deviation is 0.04 °C/ Ω . The mentioned slopes have been determined from the linear fits (first order polynomial fit) obtained for each TTC. The correlation factors are in the range of 0.9999 for data between 20°C and 135°C and temperature steps of 5°C (24 experimental points).

Figure 3

When the TTC operates at standard temperatures, the best option to increase its accuracy is to calibrate the R_S response in the temperature range of interest [15]. Nevertheless, the proposed device can also be used at higher temperatures, up to 200°C. In this extended operation range, the nonlinearities of the temperature versus R_S curve become relevant and the first order fitting shows considerable errors, mainly at low and high temperatures. This can be seen in Figure 4, where the error between the true temperature and the calculated one is represented for first, second and third order polynomial fits of the calibration data. These curves correspond to a particular TTC but the same behavior can be extended to all devices. Figure 4 shows also that the second order fitting gives an error lower than 0.5°C between 20°C and 175°C and, in any case, the error is always lower than 1°C for all the measurement range. It is also interesting to observe that a higher fitting order, order 3 in Figure 4, does not reduce the calibration error.

Figure 4

Another relevant aspect concerns the R_H dependence on the temperature. In order to easily fix predictable power dissipation values, it is interesting to have a low R_H variation with

temperature or, at least, to easily predict this relationship. In this sense, Figure 5 shows the R_H dependence on the temperature up to 125°C for a given TTC. As it can be derived from the linear fit associated with this data, the poly-silicon R_H sensitivity is approximately 0.05 $\Omega/^\circ\text{C}$.

Figure 5

Although the proposed TTC was mainly designed for steady state analysis, in some applications it has also been used in transient operation. For these applications it has to be taken into account that the dynamic response of the temperature sensing circuit is limited by a parasitic capacitance (50 pF - 100 pF) between R_H and R_S .

3.2. Thermal characteristics of the TTC

In typical power electronics applications, the main heat transfer mechanism from the device to the environment corresponds to conduction from the top zone of the die towards a heat-sink across the different materials' stack constituted by the semiconductor, die-attach and packaging layers. For the proposed TTC, although the heat is generated by individual poly-silicon strips distributed on the surface of the die, the heat-spreading inside the Si bulk allows considering an equivalent homogeneous distributed heat source on the top surface. This fact is demonstrated by the Flotherm [16] thermal 3D simulations shown in Figure 6. Figure 6 a) shows the temperature distribution along the X axis at different depths inside a 525 μm thick silicon slab, when a given constant power density of 151 W/cm^2 is dissipated by the top-side strips. These strips have the same lateral size and pitch distribution than the ones of the proposed TTC. Lateral symmetry and constant temperature (20°C) in the backside of the silicon slab are assumed. As it can be observed, at 38 μm from the top ($Y=487 \mu\text{m}$) the temperature distribution is practically constant (24.91°C) and the effect of the individual strips is not appreciable.

Figure 6 a) and b)

The simulations corresponding to Figure 6 b) have been performed under the same conditions than those of Figure 6 a), but the heat source has been replaced by a homogeneous poly-silicon layer. Consequently, the internal temperature distribution corresponds to constant isothermal surfaces at each depth and, at 38 μm the temperature value is again 24.91°C. Thus, it can be assumed that approximately 40 μm below R_H the heat flux is homogeneous, being the isothermal lines parallel to the chip backside surface. This fact allows an easy description and modeling of the thermal phenomena inside the TTC, as will be shown further on.

The main deviation from this simple behavior is induced by the $700\text{ }\mu\text{m} \times 700\text{ }\mu\text{m}$ central area taken by R_S and by the Aluminum pads at the chip edges. In these zones, any heat dissipation is produced and consequently, the temperature of the Silicon is slightly lower than in its surrounding area. These temperature differences have been quantified by simulation using Flotherm for a fixed temperature of 20°C at the TTC backside and free air convection around the device. The heat source on the top of the TTC has been modeled as a square homogeneous dissipating surface, taking the same area than that of the poly-Silicon strips ($5.6\text{ mm} \times 5.6\text{ mm}$ in total), with a central $700\text{ }\mu\text{m} \times 700\text{ }\mu\text{m}$ hole. Figure 7 a) shows the temperature profile along the X axis at different depths (Y) when crossing the center chip zone. On the top surface, the temperature difference between the chip center and the maximum reached value is 2.9°C for 50 W constant dissipation. As it can be observed, this effect persists inside the silicon slab below R_S . In turn, Figure 7 b) shows the same temperature distributions along X, but relatively far away from the central part of the TTC. A practically constant temperature plateau can be observed, while the temperature decreases a few degrees when approaching the chip edge. This phenomenon occurs at different depths.

Figure 7 a) and b)

Another thermal issue to be considered is the influence of the thin SiO_2 layer responsible of the electrical isolation between R_S and R_H . On the one hand, the thermal resistance of a SiO_2 parallelepiped of $6\text{ mm} \times 6\text{ mm} \times 35\text{ nm}$ is $7.5 \times 10^{-4}\text{ K/W}$, considering a thermal conductivity for this material of 1.3 W/m.K . Namely, for a dissipated power of 50 W , the temperature difference between both oxide surfaces is 0.04°C . Consequently, the thermal influence of this layer on the dissipation phenomena can be neglected for all practical operation conditions. On the other hand, R_S is also placed over the thin oxide layer. This means, in principle, a difference between the temperature of the Silicon surface and that of R_S because both surfaces are in thermal contact by a 0.05 K/W thermal resistance ($700\text{ }\mu\text{m} \times 700\text{ }\mu\text{m} \times 35\text{ nm}$ SiO_2 parallelepiped). Nevertheless, at this point there is not a significant heat flux because the heat flows from the poly-silicon strips towards the TTC backside and, consequently, the temperature value detected by R_S can be considered the same one of the silicon surface.

4. Application Examples

This section shows the versatility of the proposed TTC in three different research and engineering fields: Thermal characterization of power assemblies and substrates, thermal modeling validation, and thermometry calibration purposes. The most relevant aspects of the TTC related with each application are discussed here and details about each particular application can be found in the provided references.

4.1. Thermal characterization of power assemblies and substrates

A precise knowledge of the characteristics of power substrates is crucial to undertake an accurate power-module thermal design. Two main kinds of substrates are used in typical power electronics assemblies: Direct Copper Bonded (DCB) substrates and Insulated Metal Substrates (IMS), though for low-power applications Printed Circuit Board (PCB) substrates are sometimes also used. DCB ceramic substrates are the preferred ones for high power applications. They consist basically in a Copper-ceramic-Copper sandwich structure. Alumina (Al_2O_3) and Aluminum Nitride (AlN) ceramic layers are the most used and they show very good thermal performances. Insulated Metal Substrates represent an interesting alternative for medium power and low cost applications. Although their thermal properties are worse than those of the DCB substrates, they are less expensive, more robust and machineable. IMSs are based on a thick Aluminum base-plate clad with a Cu foil on the other side, using a polymer-ceramic composite bonding layer. This layer is made of an organic resin (for example epoxy), with ceramic fillers in order to increase the thermal conductivity. There is a trade-off between the performances (thermal, mechanical and electrical) of the IMS substrates and their cost, depending on the different technological solutions and materials selected for the fabrication of the dielectric layer. The prediction of the thermal parameters of this kind of composites is very difficult and strongly dependent on each particular composition and fabrication process. Thus, in situ thermal characterization is mandatory.

A quantitative study of the static thermal behavior of five power substrates (a PCB, three IMS and a DCB), was performed using a thermal test vehicle based on two TTCs soldered onto the substrates under test [17]. The analysis was performed using continuous and pulsed (power pulses of 2.5 s) power values up to 40 W on the TTCs (110 W/cm^2), obtaining the same results. From the temperature measurements, the self-heating of the active device and the thermal coupling effects between active and inactive chips are studied. Figure 8 shows the plots of temperature increment (taken the reference at the substrate backside) versus dissipated power for the active TTC. In this figure, a linear relationship is observed between temperature and power and the slope of these curves gives the chip-to-backside thermal resistance (R_{TH}). This

value is basically related with the thickness and thermal conductivity of the different materials making up the substrate stack. For the IMS case, the predominant parameter in R_{TH} is the thermal conductivity of the dielectric layer. The IMS power dissipation capability is placed between that of FR4 PCB and alumina DCB substrates. In particular, the lower cost IMS shows half R_{TH} value than FR4, while the more performing (and expensive) IMS shows five times lower R_{TH} value than FR4. On the other hand, the R_{TH} of this IMS is only three times higher than that of the ceramic DCB.

The comparative analysis of the five substrates has been performed under true operation conditions. Although functional power devices will present different R_{TH} values than those obtained with the TTC, the relative values between different substrates will be practically the same. Thus, using the TTC, the quantitative thermal comparison between different substrate technologies can be performed with standard instrumentation, avoiding the complexity of junction temperature measurement of functional devices.

Figure 8

The method for the power substrate assessment discussed above, provides valuable information. However, it is sometimes more interesting to get the thermal conductivity (K_{TH}) values of particular materials in order to design a given assembly or module by thermal simulation. In this sense, a parameter identification method based on the proposed TTC has been also developed [18]. The method is based on a thermal test assembly implemented by soldering and connecting the TTC on the substrate under test. In a previous characterization step, the chip-to-backside thermal resistance of the test assembly is measured. In a second step, the thermal conductivity of the critical substrate layers (the dielectric ones) is identified minimizing the difference between the experimental and the simulated thermal resistances of the assembly. Consequently, a numerical 3D model of the test assembly must be previously defined, using in our case the Flotherm CFD simulation software. The method has been applied to a DCB substrate with a nominal thermal conductivity value for the alumina layer of 24 W/m.K, although the identified K_{TH} value was 11.5 W/m.K. The curves of Figure 9 show the simulated vertical temperature profile at the center of the DCB assembly, from the bottom of the solution domain ($Y = 0 \mu m$) up to the ambient air above the TTC ($Y = 2500 \mu m$). As it can be observed, when the heat flux flows through each layer, a temperature increase appears, the slope of the temperature profile being inversely proportional to the thermal conductivity of the layer material. The temperature increase observed in Figure 9 also confirms that, from the thermal point of view, the Al_2O_3 layer is the critical element of the DCB substrate, accounting for almost the 80% of the total substrate

temperature rise. The dashed curve of Figure 9 has been obtained with the nominal thermal conductivity value of the Al_2O_3 (24 W/m.K). For a dissipated power of 10 W, the maximum chip temperature reaches 24.2°C (temperature increment from the backside of 4.2°C). When using the identified K_{TH} value of 11.5 W/m.K to perform the same simulation, the temperature distribution is represented by the solid line and the maximum TTC temperature becomes 27.4°C (temperature increment of 7.4°C). As the thermal resistance between the chip and the baseplate can be computed as the ratio between the temperature increment and the dissipated power, it is clear that the R_{TH} deviation induced by the wrong Al_2O_3 thermal conductivity value reaches 55%.

Figure 9

The proposed identification method allows obtaining the K_{TH} value of critical materials under exactly the same operation conditions used in power module applications. It is worth pointing out that the in-situ identified values are more accurate than the nominal ones, avoiding the influence of different measurement equipment, dispersion among fabrication lots, etc. A similar approach has also been applied for the determination of the specific heat, exciting the material samples with power pulses [19].

4.2. Thermal modeling validation

Thermal simulation is the main thermal design tool used to predict temperature distributions of complex power electronics assemblies such as hybrid or power modules. Nevertheless, the validation of the simulation results remains a complex problem, mainly in dynamic operation, due to the difficulty in measuring semiconductor device temperatures and the determination of boundary conditions. Reference [20] proposes a methodology for the accurate validation of 3D thermal simulations of power modules based on a test vehicle with two TTCs soldered on an IMS substrate (see Figure 10 a). The TTCs are excited by a single power pulse while the temperature evolution at the top of the chips and at the substrate backside is acquired. Figure 10 b) presents the measured temperature increment waveforms (solid lines) of both TTCs when the active device is excited with a 2.5 s power pulse of 50 W (138 W/cm²). It is interesting to observe in the dissipated power curve that this variable is practically constant and only an initial and small decrease is observed in the first milliseconds due to the R_{H} self heating expected from figure 5. In parallel, thermal simulations of the test vehicle and its environment have been performed using Flotherm (dots in Figure 10 b). As the device temperature waveform can be

accurately measured during all the phases of the experiment (heating, steady-state and cooling) and the TTC structure is perfectly known, major efforts may be addressed to the optimization of other aspects of the simulation process. In this particular case, the first aspect that has been analyzed concerns the parameters of critical materials. The density and the specific heat of the dielectric layer of the IMS substrate are very difficult to determine from the manufacturer's information and they have been adjusted to best fit the simulation with the experimental results during the transients considering the rest of parameters known from materials data-sheets. Another element of the set-up which is usually difficult to characterize is the thermal interface material (TIM) layer between the IMS backside and the heat-sink. In the present case, a thin layer of silicone-based grease was applied. Its contribution to the total thermal resistance of the assembly has been determined during the quasi steady-state phase of the temperature waveforms. Apart from the issues related with the set-up itself, other relevant aspects concerning the boundary conditions and the simulation model were addressed. For instance, the influence of the natural air convection was analyzed, because the computation time can be considerably reduced if this effect can be neglected. In this sense, a simulation grid optimization was also dealt with to obtain accurate results spending a reasonable computation time.

The dots of Figure 10 b) show the simulation results when all mentioned aspects are considered. Very good agreement between experimental and simulation results is obtained, including the thermal coupling effect, when the inactive TTC is heated by the active device. The important point is that all the conclusions derived during the simulation optimization process (parameter values, TIM layer effects, boundary conditions, grid size, etc.) can be directly applied to functional power modules based on the same substrates, where direct dynamic temperature measurements are difficult to obtain at device level.

Figure 10 a) and b)

Numerical simulation methods are part of the most accurate approaches to couple electrical, thermal and mechanical effects. However, the simulation cost limits their usage and compact models are then required for efficient electro-thermal simulation, their validation being one of the relevant aspects to complete the modeling task. For this application, the TTC is also very useful because it allows the assessment of compact thermal modeling methods working under different operation conditions and regimes (steady-state, step response, sinusoidal regime, etc.), giving access to the temperature waveforms at any time instant. In particular, the Diffusive Representation approach has been validated for compact thermal modeling using the proposed thermal test vehicle shown in Figure 10 b) [21]. The Diffusive Representation allows a systematic and efficient way to build compact thermal models using the state-space formalism.

The application of the proposed method was tackled in two phases. In a first phase, the test vehicle is excited to obtain identification data. In a second phase, other experiments are carried out under different excitation conditions (different power pulse amplitudes and durations) in order to analyze the predictions of the identified model. In addition, as two TTCs are assembled in the test vehicle, the multi-input/multi-output modeling capabilities of the Diffusive Representation are also demonstrated, considering the model inputs as the dissipated powers and the model outputs as the TTCs temperature increments. As the complete temperature waveforms are available when using the TTC (not only the cooling phase as it is often the case when using functional power devices), the accuracy and robustness of the model can be analyzed during all transient and steady-state conditions through the influence of model parameters and model order on the error between computation and experiment.

4.3. Thermometric calibrations

The TTC has also been used to calibrate thermometric set-ups developed for performing internal infrared laser deflection (IIRLD) [22] and interferometry-based measurements [23]. This application is grounded on the fact that simple analytical expressions can describe the TTC internal temperature profiles. These simple expressions can be inferred regardless of the analysis domain (time or frequency) in which the measurements are performed. As long as the measurements are performed at the plateau region shown in Figure 7 b) for short excitation times (time domain) [24] or high frequencies (frequency domain) [25], the TTC behaves like a semi-infinite vertical slab with a constant heat flux injected onto its top-side ($Y = 0$) [26, 27]. Under these conditions, the transient evolution of the temperature rise profile within the TTC at a given depth Y ($\Delta T(t, Y)$) may be described in the time domain as [27]:

$$\Delta T(t, Y) = -2 \frac{P}{A K_{TH}} \left\{ \sqrt{\frac{D_{\alpha} t}{\pi}} \exp\left(\frac{-Y^2}{4D_{\alpha} t}\right) - \frac{Y}{2} \operatorname{erfc}\left(\frac{Y}{\sqrt{4D_{\alpha} t}}\right) \right\} \quad (1)$$

where P is the dissipated power, A is the top area of the chip, K_{TH} is the thermal conductivity of Silicon (148 W/m.K at room temperature) [28] and D_{α} denotes the thermal diffusivity of Silicon. D_{α} may be derived from:

$$D_{\alpha} = \frac{K_{TH}}{\rho c} \quad (2)$$

where ρ and c are the mass density ($2.33 \times 10^3 \text{ kg/m}^3$) [28] and the specific heat capacity of Silicon (713 J/kg.K) [28], respectively. Eq. (1) applies for power pulses with a time duration well below $L^2(4 D_\alpha)^{-1}$, where L is the TTC thickness.

In the frequency domain, when the sinusoidal steady-state is reached, a given power density or heat flux $P'(t, Y=0)$ is injected into the device at an angular frequency ω_{heating} , following this periodic function:

$$P'(t, Y=0) = (P_0 / A) \cos(\omega_{\text{heating}} t) \quad (3)$$

where P_0 is the amplitude of the dissipated power. $\Delta T(t, Y)$ may be written as:

$$\Delta T(t, Y) = \frac{L_d}{\sqrt{2}} \frac{P_0}{2 A K_{TH}} \exp\left(-\frac{Y}{L_d}\right) \cos\left(\omega_{\text{heating}} t - \frac{Y}{L_d} - \frac{\pi}{4}\right) \quad (4)$$

L_d corresponds to a characteristic length expressed in terms of ω_{heating} and the diffusivity of the material (D_α):

$$L_d = \sqrt{\frac{2 D_\alpha}{\omega_{\text{heating}}}} \quad (5).$$

Eq. (4) can be used when the condition $\omega_{\text{heating}} \gg L^2(2 D_\alpha)^{-1}$ is satisfied.

In the IIR-LD thermometry, an infrared laser probe beam passes through a biased device, striking perpendicularly on its lateral walls (see the inset of Figure 11). From the measurement of the beam deflection, it is possible to deduce a longitudinal averaged value for the temperature gradient at a given depth. The beam deflection is due to the refractive index gradient (“mirage” effect) induced by the coupled contribution of temperature and free-carrier concentration gradients. As the TTC does not present any vertical current, only the thermal effects are measured. The signal corresponding to the laser vertical deflection is linearly dependent on the vertical temperature gradient. The proportionality constant is function of several parameters related with the set-up and with the semiconductor properties [24]. To derive the temperature profile, the integration of the measured temperature gradient must be carried out along the several inspection depths Y . The mathematical model given by eq. (1) corresponding to the time domain evolution of ΔT is used as a calibration reference allowing the fine adjustment of all parameters involved in the measurement chain. In particular, it is possible deriving the thermo-optical coefficient of the analyzed material. This coefficient describes the refractive index dependence on temperature of the semiconductor, and its in-situ measurement is of main

importance because considerable dispersion is found in the values reported in the literature. During the calibration process of the IIRLD measurements described in reference [24], the TTC is thermally excited with 250 μs power pulses up to 60 W (167 W/cm²). Figure 11 shows $\Delta T(t, Y)$ for three excitation times (50, 150 and 250 μs). The solid lines represent the temperature distribution predicted by the analytical model from eqs. (1) - (2) and, as it can be observed, they agree with the experimental points (dots). These calibration works were also extended to the frequency domain in Ref. [25]. When the heat sources are excited with sinusoidal waveforms (eq (3)), the IIRLD method shows significant improvements in terms of accuracy, robustness to noise, control of boundary conditions and heat flux confinement. In addition, working in the frequency domain allows direct temperature measurement, avoiding integration steps to derive the temperature from the temperature gradient measurements. Consequently, eq. (4) can be directly used to validate temperature increment experimental data.

Figure 11

On the other hand, the TTC has been used for the validation of the transmission Fabry–Pèrot interference (FPI) thermometry [23]. In this technique, the parallel opposite walls of the chip act as a Fabry–Pèrot cavity. The interferometry pattern of the transmitted radiation through the device, provide a given temperature increment between consecutive maxima due to the optical path modification of the cavity [29, 30]. This modification is mainly associated to the refractive index dependence with temperature, since thermo-mechanical expansion can be neglected. In this case, the recorded magnitude of the laser probe is its power and the extracted result is the device internal temperature profile. This thermometry is compatible and complementary with the IIRLD one. In Ref. [23], simultaneous IIRLD (laser beam deflexion) and FPI (laser beam intensity variation) measurements are performed on a TTC excited with 250 μs power pulses of 15 W, 30 W and 60 W. Again, the predictability of the internal temperature distribution has allowed an accurate validation of the FPI technique and a direct comparison with the IIRLD one. The results corresponding to 60 W power pulses are depicted in Figure 12. The temperature increase evolution inside the TTC substrate is recorded at two depths (70 μm and 90 μm from the top) during the heating phase. As it can be appreciated, the fitting between the ΔT values predicted by eq. (1) (solid lines) and the experimental data (dots) is remarkable.

Figure 12

5. Conclusions

The design, fabrication and characterization of a low-cost and versatile high power thermal test chip have been described. The proposed device thermally behaves like typical power devices, with a power generation area on the top-side and heat dissipation towards the back-side by conduction. It allows dissipating power densities up to $200\text{W}/\text{cm}^2$ using a poly-silicon heating resistor distributed on the top surface. Simultaneously, the temperature on the centre of the top surface can be accurately measured using a Platinum resistor (up to 200°C). Thus, the dissipation and temperature measurement circuits are decoupled and the thermal response of the device can be achieved with standard equipment.

The versatility of the proposed TTC has been demonstrated with some application examples of three different engineering and research fields. First, the thermal behavior of different power substrates is quantitatively evaluated. It has been demonstrated that the TTC is suitable for the evaluation of the thermal conductivity of critical power substrate layers (ceramics, composites, etc.). Second, the simple structure of the TTC allows easy thermal modeling and 3D simulation, useful for the validation of analytical models and the determination of thermal parameters of numerical simulators. Finally, the heat flux distribution inside the TTC can be accurately predicted. This feature has been used to calibrate advanced internal temperature measurement apparatus. In particular, it has been possible to calibrate an internal IR laser deflection system working in the time and the frequency domain, as well as a transmission Fabry-Pérot interference thermometry set-up. In conclusion, the proposed TTC design provides a powerful tool in the main thermal management branches: design, parameter extraction and characterization.

Acknowledgements

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Figure Captions

Figure 1 Top view of a TTC soldered on a ceramic substrate. The parallel poly-silicon strips of R_H cover the top surface and are connected at the edges with Al wire-bonds in parallel. On the center, the R_S Platinum sensing resistor is connected with 4 wire-bonds (Kelvin measurement).

Figure 2 TTC schematic cross-section (not to scale) showing the different layers of the structure. The left side represents a zone near the edge of the die and the right side represents the center area.

Figure 3 R_S calibration curves with temperature for 20 TTCs in the 20°C - 135°C range.

Figure 4 Temperature error plots for 3 different polynomial fittings between the temperature and the R_S calibration data, in the 20°C - 200°C range.

Figure 5 Temperature dependence of the poly-silicon R_H on the temperature. The dots represent experimental data and the solid line a linear fit with a correlation factor of 0.99804.

Figure 6 a) 3D thermal simulation of an infinite distribution of poly-silicon strips on top of a 525 μm thick Silicon slab, showing the internal temperature profiles at different depths. b) Simulation of a homogeneous heat source, equivalent to the poly-silicon strips. At 38 μm from the top, the temperature distribution is practically the same for both simulations.

Figure 7 Temperature distributions along X axis at different depths, a) when crossing the Silicon below the R_s zone, and b) far away from the inactive R_s zone. For both cases, the heat source (50 W) is homogeneously distributed on the top, except on the inactive areas (centre and edges). The backside temperature is fixed at 20°C.

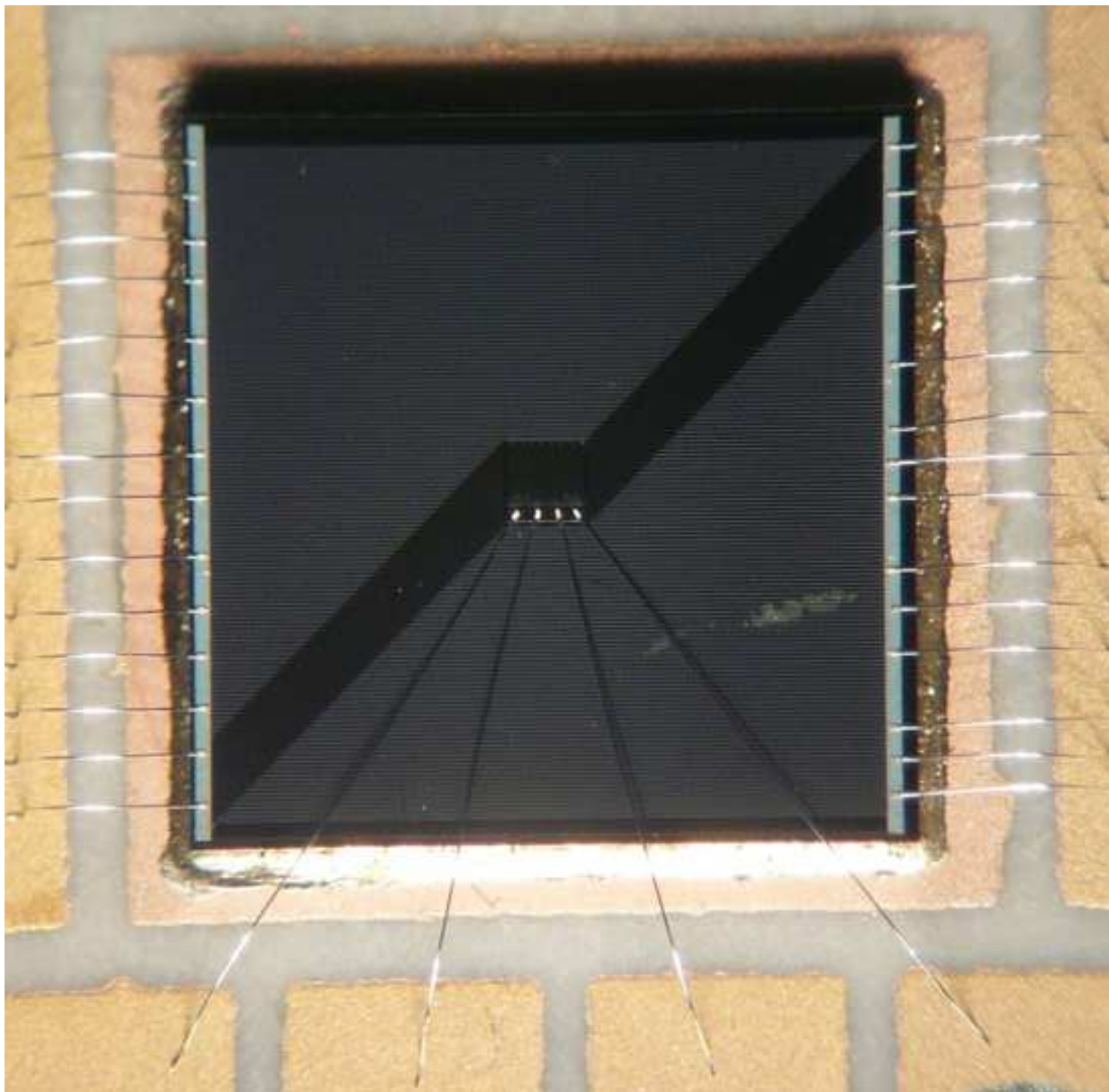
Figure 8 Active TTC temperature increment from the substrate backside (reference) versus the dissipated power for five substrates, a PCB, 3 IMS and a DCB.

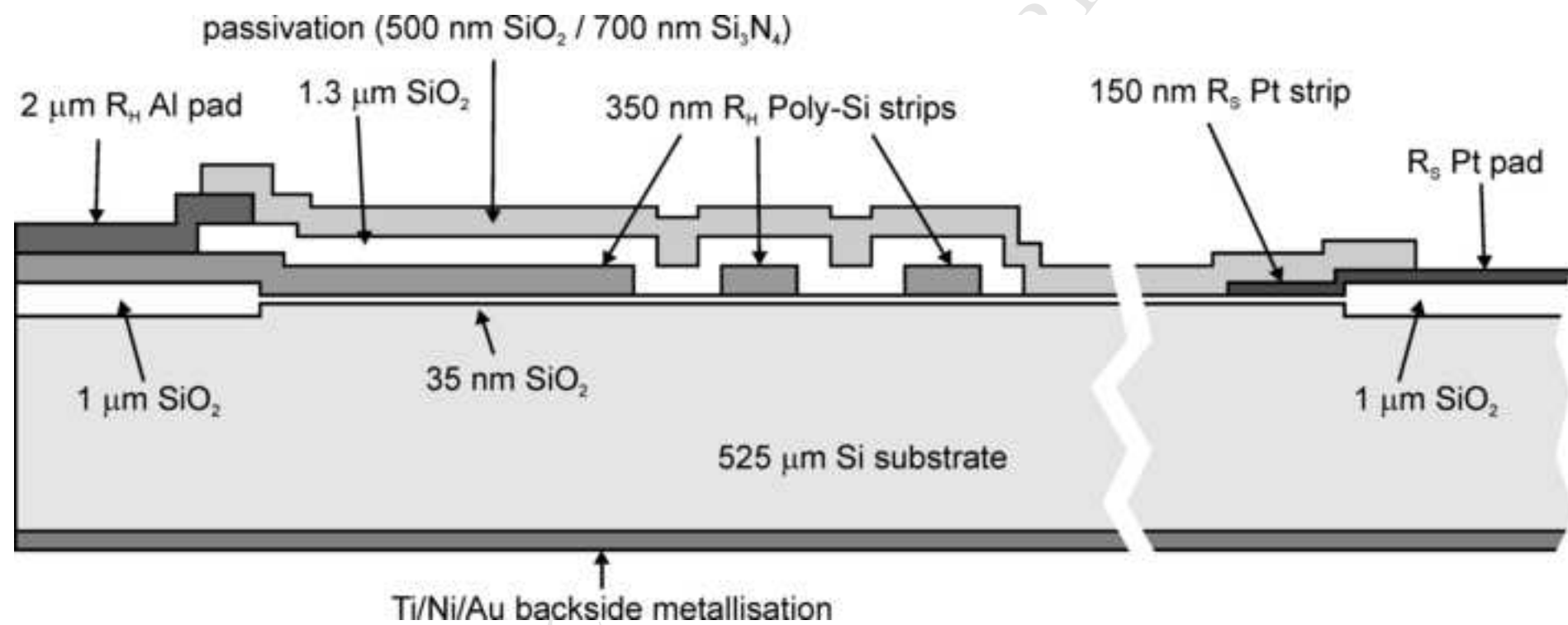
Figure 9 Simulated vertical temperature profile below the TTC center of a DCB substrate assembly, for a dissipated power of 10 W, using two different K_{TH} values for the Al_2O_3 .

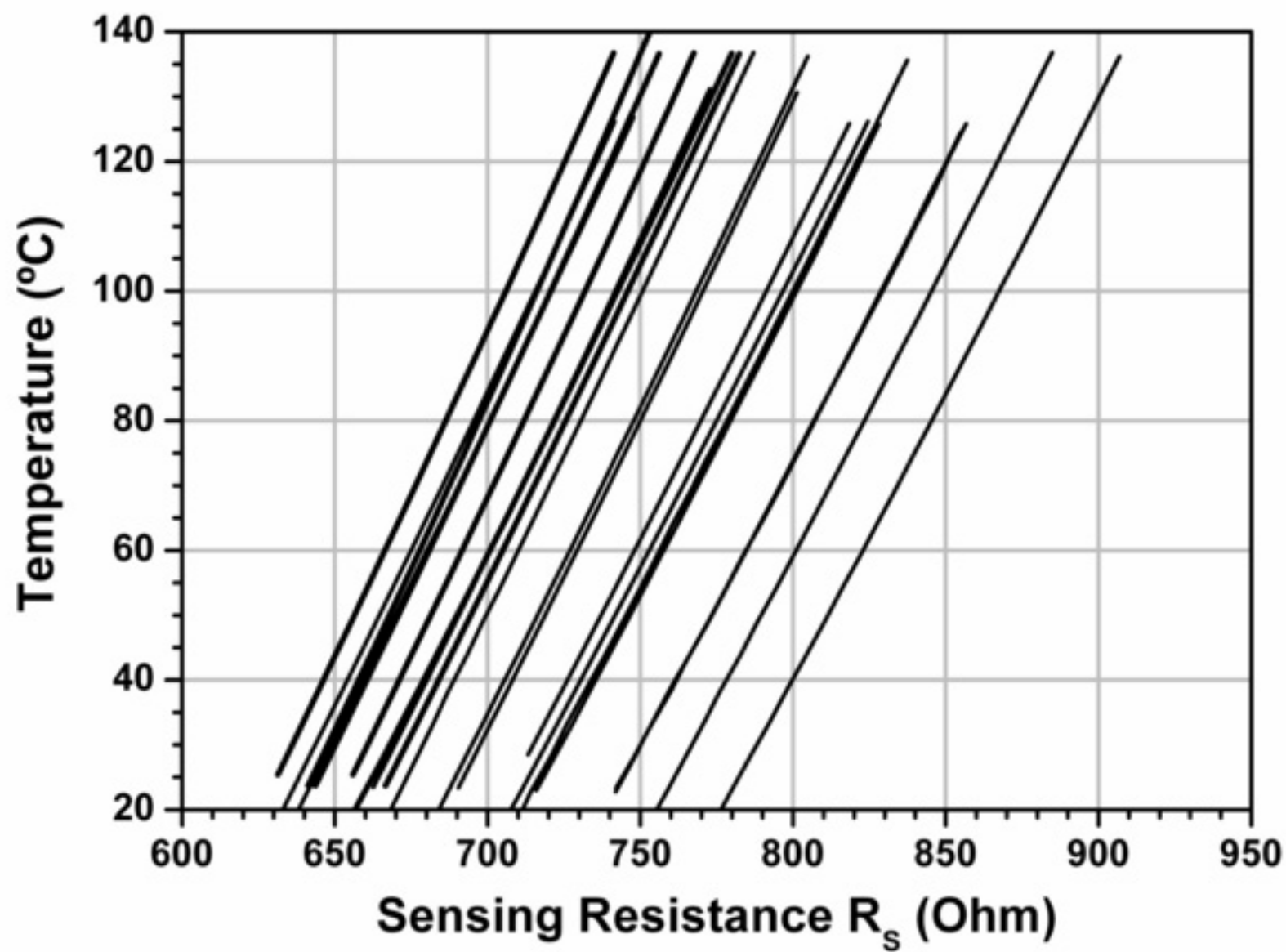
Figure 10 a) Scheme of the two TTCs test assembly for power modules simulation assessment. b) Comparison between experimental (solid lines) and simulated (dots) temperature increments for both TTCs when the active device is excited with a 2.5 s - 50 W power pulse.

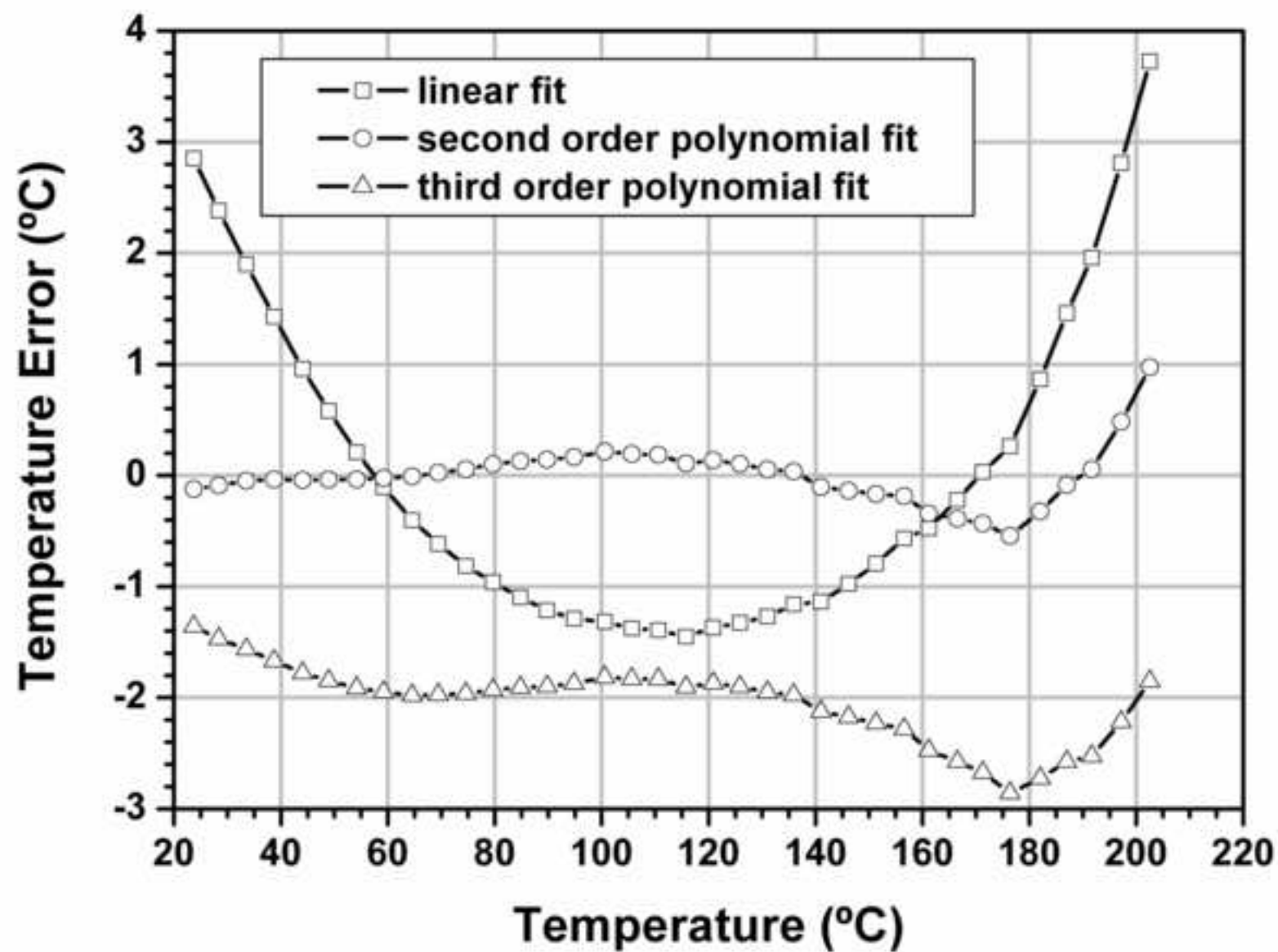
Figure 11 Temperature increment distribution along the vertical axis inside the TTC at three different excitation times (50 μ s, 150 μ s and 250 μ s). The solid lines represent the analytical model prediction and the dots, the experimental points.

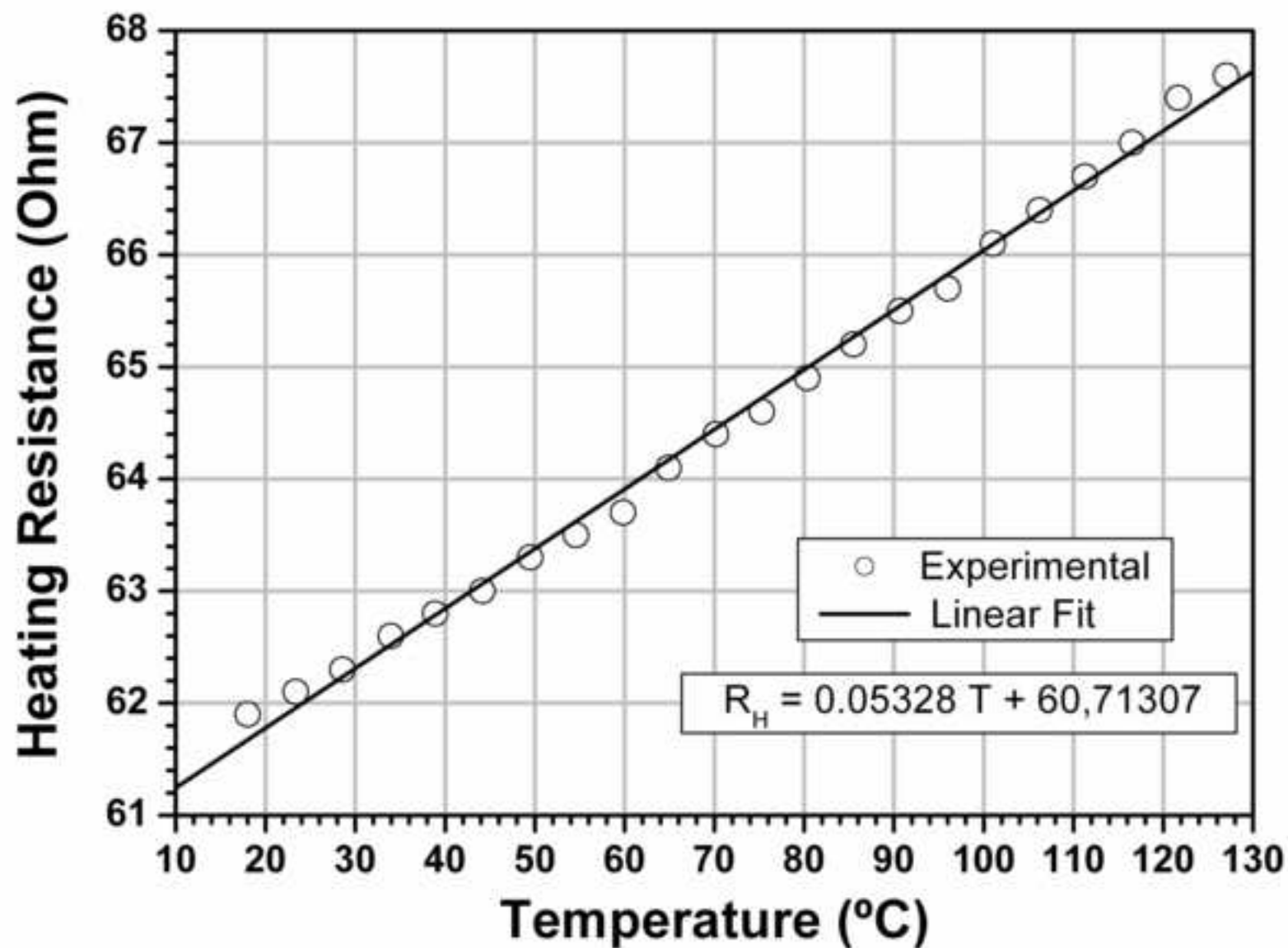
Figure 12 Comparison between theory (solid line) and measurements (dots) of the temperature evolution at two depths (solid symbols $Y=70 \mu$ m, empty symbols $Y=90 \mu$ m) during the TTC heating process ($P=60$ W), using IIR-LD (round symbols) and FPI (square symbols) thermometry.

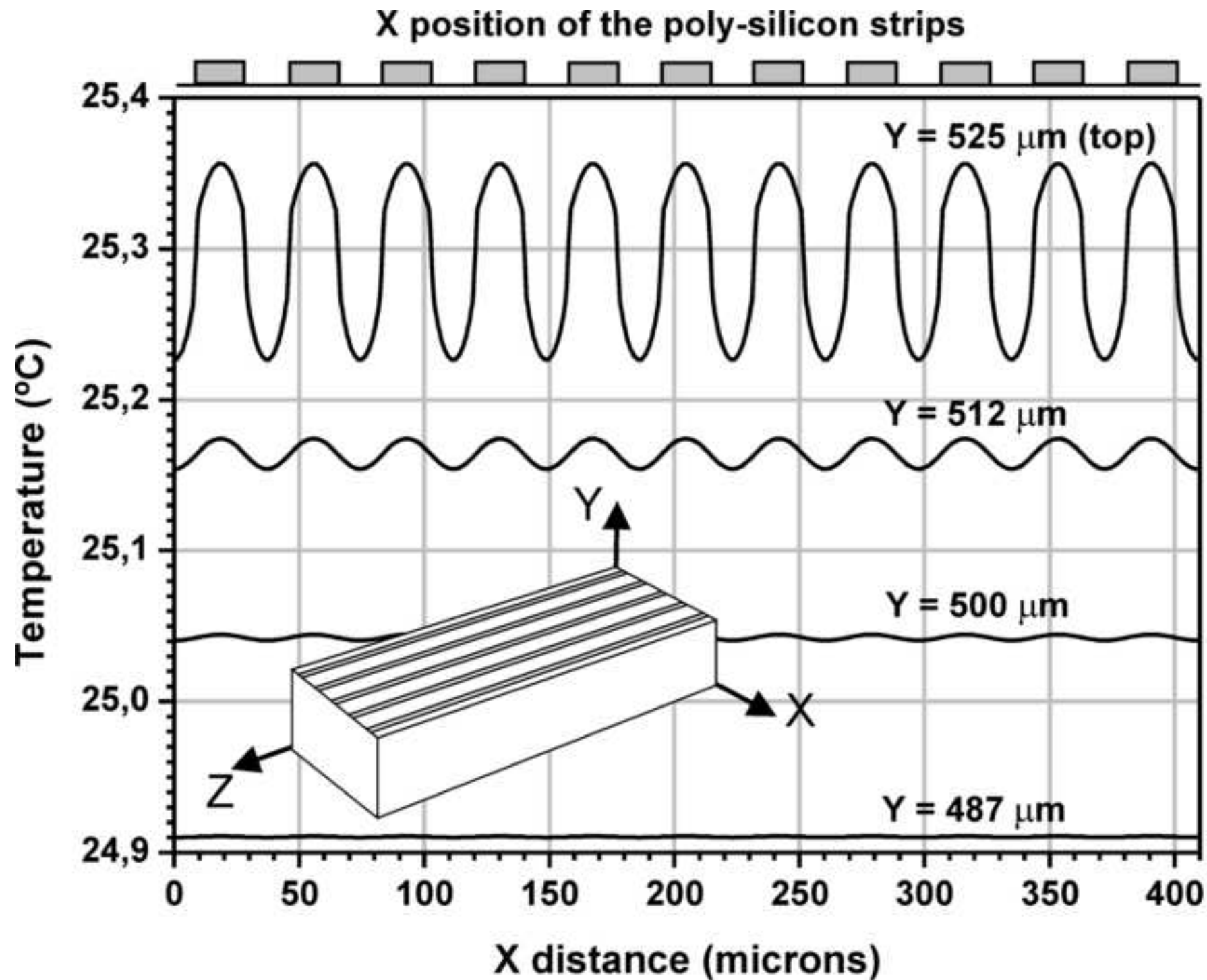












Equivalent distributed poly-silicon heat source

